75X SERIES

4-BIT SINGLE-CHIP MICROCONTROLLER

Selection Guide, Version 12

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PREFACE

Because of their excellent cost performance, 4-bit microcontrollers are used in various equipment from consumer products such as video cassette recorders, audio sets, television sets, and microwave ovens to industrial equipment such as copiers, telephones, and dashboards.

NEC has commercialized high-performance original devices as a pioneer of the industry since developing the first 4-bit microcontrollers, the mCOM-4, in Japan in 1973. Next, NEC released the 75X series, which adapts state-of-the-art architecture and advanced process technology for drastic improvement in performance.

The 75X series are epoch-making 4-bit microcontrollers having the controllability peculiar to 4-bit microcontrollers and arithmetic operation functions equivalent to those of 8-bit microcontrollers.

The Selection Guide introduces the 75X series features, product line-up, development tools, etc.

CONTENTS

1. NEC 4-BIT MICROCONTROLLERS AND 75X SERIES

NEC 4-bit microcontrollers development can be classified into four generations, as shown in Figure 1-1.

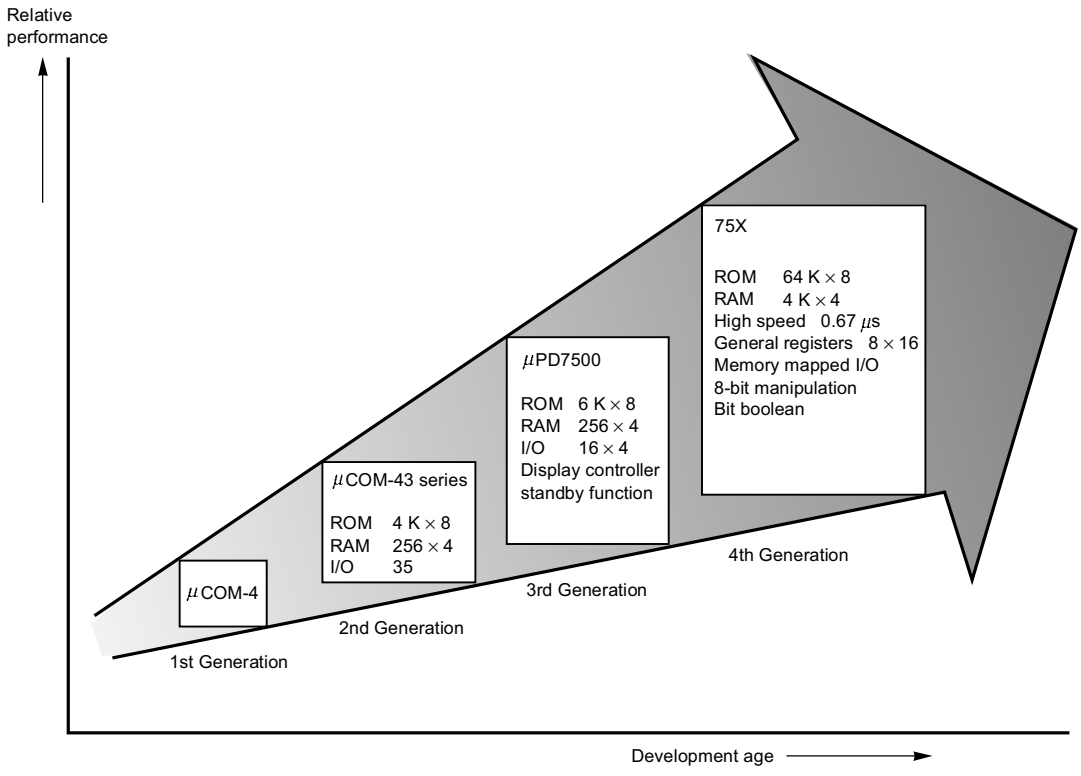
The mCOM-4 of the first generation and the mCOM-43 of the second generation proved that 4-bit microcontrollers were applicable to various devices and were LSIs indispensable to downsizing and adding value to devices.

The high performance, power saving, and on-chip peripheral hardware of 4-bit microcontrollers became indispensable for obtaining high performance, downsizing, and power saving for application devices. Next, the mPD7500 series of the third generation was released. This series has the features of high performance and low power consumption. Various peripheral hardware devices are mounted on a single chip. About 30 product types are commercialized.

However, multifunctional application equipment require faster, higher-performance 4-bit microcontrollers containing mass memory. Fortunately, LSI production technology is progressing at a remarkable rate and these requirements can be met. The 75X series has been developed by adopting a new 4-bit microcontrollers architecture that expands the mPD7500 series.

The 75X series contains all the functions of the mPD7500 series and provides full continuity from the mPD7500 series. Thus, the mPD7500 series application programs can be easily modified for the 75X series.

Figure 1-1. 4-bit Microcomputer Development



Remark The performance of the highest-performance product in each series is indicated in the box.

[MEMO]

2. 75X SERIES FEATURES

The basic features of the 75X series are as follows:

(1) Enhancement of addressing capability
    ROM : 64 K × 8 bits MAX.
    RAM : 4 K × 4 bits MAX.
(2) High-speed instruction execution (0.67 μs)
(3) Improvement of peripheral hardware expansion and expansibility
(4) Drastic improvement of instruction functions
(5) Maintenance of inheritance from the μPD7500 series

The 75X series has been especially contrived to provide these features. The hardware and software features of the 75X series are described below.

2.1 Hardware Features

(1) Program memory (ROM)

The program memory can be expanded to a maximum of 64 K × 8 bits. Products that consist of the same hardware and differ only in internal memory capacity are scheduled to be released as a series.

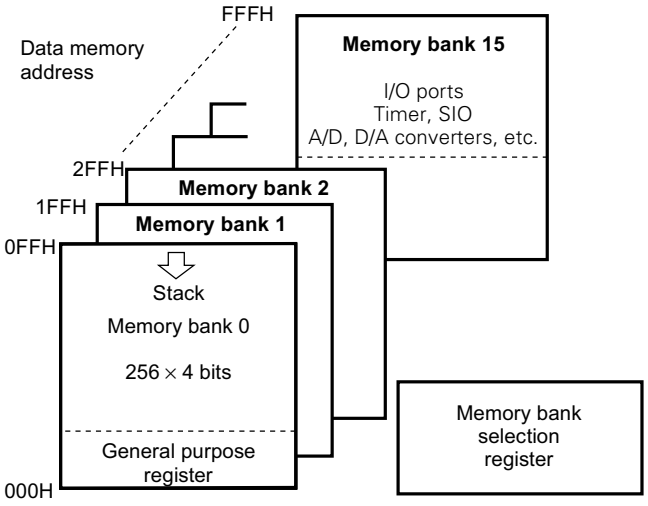
(2) Data memory (RAM)

The data memory can be expanded to a maximum of 16 banks each consisting of 256 × 4 bits. Products that consist of the same hardware and differ only in internal memory capacity are scheduled to be released as a series. The following addresses are mapped in the data memory space:

a. Static RAM
b. General-purpose registers
c. Stack area
d. I/O ports
e. Peripheral hardware such as timers, SIO, and interrupts

Figure 2-1 shows the data memory space map.

Figure 2-1. Data Memory Space Configuration

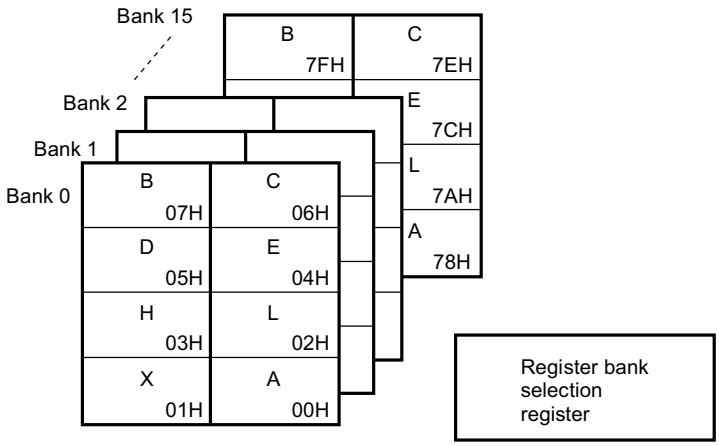


(3) General purpose registers

A maximum of 16 general purpose register banks each consisting of eight 4-bit registers X, A, B, C, D, E, H, and L can be contained. These are mapped in the data memory and can be handled by executing general purpose register handling instructions and data memory manipulating instructions. The registers can also be paired as 8-bit registers XA, BC, DE, and HL for handling.

An appropriate number of register banks are mounted on a chip according to the product type. Figure 2-2 shows the general purpose register configuration

Figure 2-2. General Purpose Register Configuration



(4) High-speed operation and low power consumption

The 75X series enables an instruction cycle 0.67 μs or less. Since the instruction cycle time can be changed under the program control, if the supply voltage lowers, operation can also be changed to low-speed operation to continue processing. The standby mode is HALT or STOP. In the HALT or STOP mode, CPU operation can be stopped by a program and restarted by an interrupt signal; intermittent operation can be performed.

Thus, the 75X series is designed to enable high-speed operation and low power consumption at the same time.

(5) Interrupt function

A maximum of seven vector tables can be specified and each can contain two interrupt sources. Thus, a maximum of 14 interrupt sources can be contained. Appropriate interrupt sources are contained for each product type.

Products that contain serveral register banks have an automatic register bank switching function for when vectored interrupts are executed. Thus the interrupt service routine does not need save or restore the registers.

The 75X series is thus designed to enhance the number of interrupt sources, interrupt responsiveness, etc.

(6) Expansibility of on-chip peripheral hardware

The 75X series adopts the memory mapped I/O system to separate the CPU part and peripheral hardware part. Thus, as many peripheral devices having various functions as required can be mounted.

2.2 Software Features

(1) Addressing mode and accumulators

Since peripheral hardware is mapped in the data memory space, instructions are described centering on the general purpose registers and data memory. As described above, the general purpose registers can be specified in 4-bit or 8-bit units. On the other hand, the data memory can be addressed in 1-bit, 4-bit, or 8-bit units.

The accumulators on which data processing centers are the CY flag (1-bit accumulator), A register (4-bit accumulator), and XA register (8-bit accumulator). Thus, programs can be described as desired according to the bit length of the data to be processed.

(2) Instruction set features

a. 4-bit handling instructions

The 75X series 4-bit handling instructions are based on the μPD7500 series instruction set. Thus, the μPD7500 series programs can be easily modified for the 75X series.

b. 8-bit handling instructions

75X series 8-bit handling instructions enable transfer, comparison, operations, increment, and decrement, and match 8-bit microcomputer instructions in data processing.

c. 1-bit handling instructions

The 75X series enables direct specification of a bit address for set, clear, or test. Thus, programs can be described simply in an easy-to-understand manner. If the carry flag is used as a 1-bit accumulator, the accumulator and specified bit can be ANDed, ORed, or exclusive-ORed (Boolean algebra operations). Complicated decision processing can also be described simply according to logical expressions. Programmer load is reduced and programs are also executed efficiently.

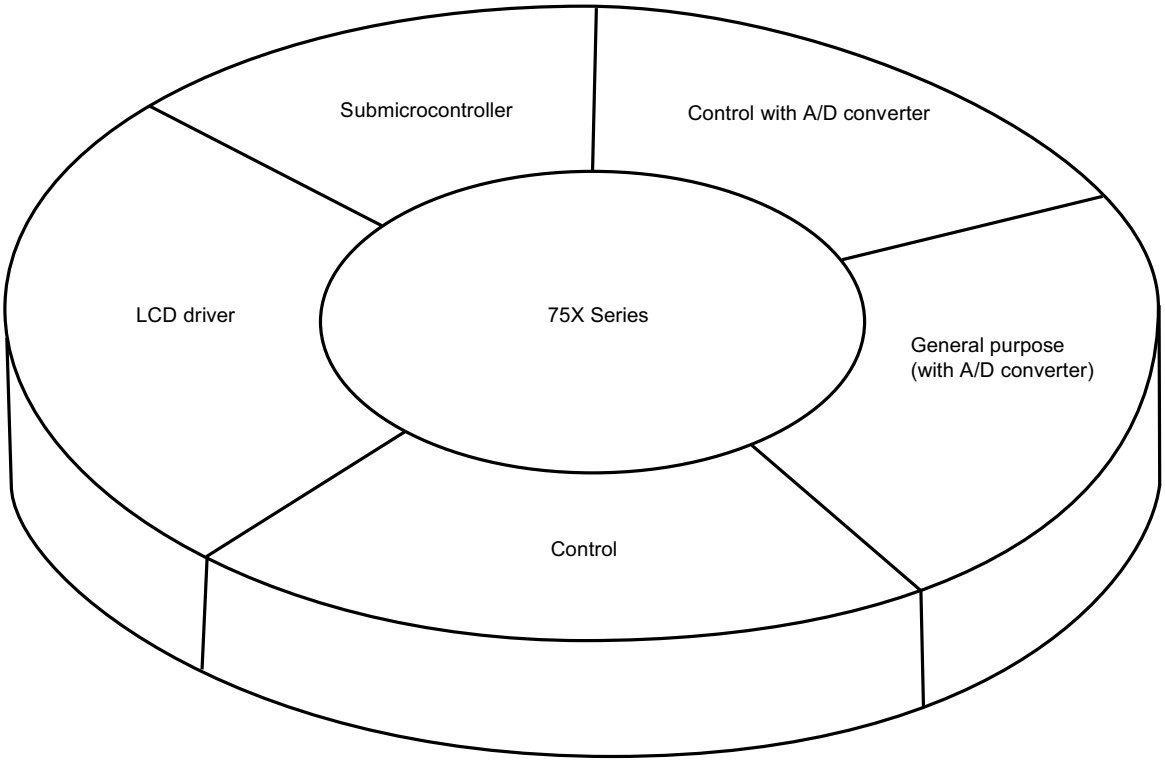
d. GETI instruction

Any 2-byte and 3-byte instructions predefined on a table are read and executed by a 1-byte GETI instruction. 48 instructions can be defined in total. The program size can be drastically reduced by making the most of the GETI instruction.

3. 75X SERIES PRODUCT DEVELOPMENT

(1) μPD750×× series (General purpose)
(2) μPD751×× series (Control)
(3) μPD753×× series (LCD driver)
(4) μPD754×× series (Submicrocontroller)
(5) μPD755×× series (Control, with on-chip A/D converter)

Figure 3-1. 75X Series Product Development



3.1 75X Series Product List

(1) μPD750×× series (General purpose)

Part number	ROM×8	RAM×4	I/O	Package	PROM version
μPD75064	4K	512	32	42-pin SDIP 44-pin QFP (10×10 mm)	μPD75P068 (8K)
μPD75066	6K				
μPD75068	8K				

(2) μPD751×× series (Control)

Part number	ROM×8	RAM×4	I/O	Package	PROM version
μPD75104	4K	320	58	64-pin SDIP 64-pin QFP (14×20 mm)	μPD75P108B (8K)
μPD75106	6K				
μPD75108	8K	512			
μPD75112	12K				μPD75P116 (16K)
μPD75116	16K				
μPD75104A	4K	320		64-pin QFP (14×14 mm)	—
μPD75108A	8K	512			
μPD75108F	8K			64-pin QFP (14×20 mm)	μPD75P108B Note (8K)
μPD75112F	12K				μPD75P116 Note (16K)
μPD75116F	16K				
μPD75116H	16K	768		64-pin QFP (12×12 mm) (14×14 mm)	μPD75P117H (24K)
μPD75117H	24K				

Note It differs from μPD751××F in some of its electrical characteristics.

(3) μPD753×× series (LCD driver)

Part number	ROM×8	RAM×4	I/O	Package	PROM version
μPD75304	4K	512	40	80-pin QFP (14×20 mm)	μPD75P308 (8K)
μPD75306	6K				
μPD75308	8K				
μPD75304B Note	4K			80-pin QFP (14×14 mm) (14×20 mm) 80-pin TQFP (12×12 mm)	μPD75P316A (14×20 mm, 16K) μPD75P316B (12×12 mm, 14×14 mm, 16K)
μPD75306B Note	6K				
μPD75308B Note	8K				

Note The μPD75304B, 75306B and 75308B are low-voltage operation version of the μPD75304, 75306 and 75308, respectively (V_{DD} = 2.0 to 6.0 V).

(4) μPD754×× series (Submicrocontroller)

Part number	ROM×8	RAM×4	I/O	Package	PROM version
μPD75402A	2K	64	22	28-pin DIP 28-pin SDIP 44-pin QFP (10×10 mm)	μPD75P402 (2K)

(5) μPD755×× series (Control, with on-chip A/D converter)

Part number	ROM×8	RAM×4	I/O	Package	PROM version
μPD75512	12K	512	64	80-pin QFP (14×20 mm)	μPD75P516 (16K)
μPD75516	16K				
μPD75517	24K	1024			μPD75P518 (32K)
μPD75518	32K				

3.2 Product Map (ROM Development)

Series	Typical product \ ROM	2K	4K	6K	8K	12K	16K	24K	32K
General purpose (μPD750××)									
with A/D	μPD75068		○	○	◎				
Control (μPD751××)	μPD75108		○	○	◎	○	◎		
lower voltage higher speed	μPD75108F				○	○	○		
μPD75108F+low-voltage	μPD75116H						○	◎	
LCD driving (μPD753××)	μPD75308		○	○	◎		Δ		
Submicrocontroller (μPD754××)	μPD75402A	◎							
Control (μPD755××) on-chip A/D	μPD75516					○	◎		
with higher speed	μPD75518							○	◎

Remark ○: Mask versions only
◎: Mask versions and PROM versions
Δ : PROM versions only

[MEMO]

4. 75X SERIES APPLICATIONS

Application / Product type	VCR			Audio					Communication				Automotive electronics		Others				
	Timer, tuner	System control	Camera	Tape deck	Tuner	Car stereo	CD player	DAT	Multifunctional telephone	Radio equipment	Cellular phone	Pager	Dash-board	Trip computer	ECR	Vending machine	Camera	Home electronics	Musical instrument
General purpose (μPD750××)	○		○	○		○	○	○	○	○	○	○				○	○	○	○
Control (μPD751××)		○	○	○		○	○	○	○	○	○	○	○	○		○	○	○	○
LCD drive (μPD753××)			○		○	○	○	○	○	○	○	○	○	○			○	○	
Submicrocontroller (μPD754××)				○		○	○	○		○	○		○	○	○	○	○	○	○
Control (on-chip A/D) (μPD755××)	○	○	○	○		○	○	○	○	○	○	○	○	○		○	○	○	○

[MEMO]

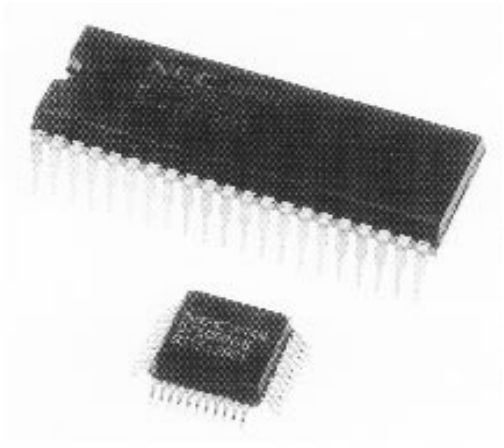
5. 75X SERIES PRODUCTS

Series	Title	Applicable product type	Page
General purpose	General purpose + A/D converter	μPD75064, 75066, 75068, 75P068	p. 15
Control	Control	μPD75104, 75106, 75108, 75112, 75116, 75104A, 75108A, 75P108B, 75P116	p. 18
	Low voltage, high speed control	μPD75108F, 75112F, 75116F	p. 21
	F product + low voltage	μPD75116H, 75117H, 75P117H	p. 25
LCD drive	LCD driving	μPD75304, 75306, 75308, 75304B, 75306B, 75308B, 75P308, 75P316A, 75P316B	p. 29
Submicrocontroller	Submicrocontroller	μPD75402A, 75P402	p. 32
Control (on-chip A/D converter)	Control (with on-chip A/D converter)	μPD75512, 75516, 75P516	p. 35
	Control (with on-chip A/D converter) + high speed	μPD75517, 75518, 75P518	p. 38

5.1 General Purpose Series (μPD750××)

5.1.1 General purpose with A/D converter

Applicable products: μPD75064, 75066, 75068, 75P068



This series provides high general purpose microcontrollers, each of which contains input/output ports, serial interface, timers, watch timer, interrupt function, watch subclock oscillator, A/D converter, etc. These microcontrollers provide all standard microcontroller functions, and thus can be used as standard microcontrollers in every field.

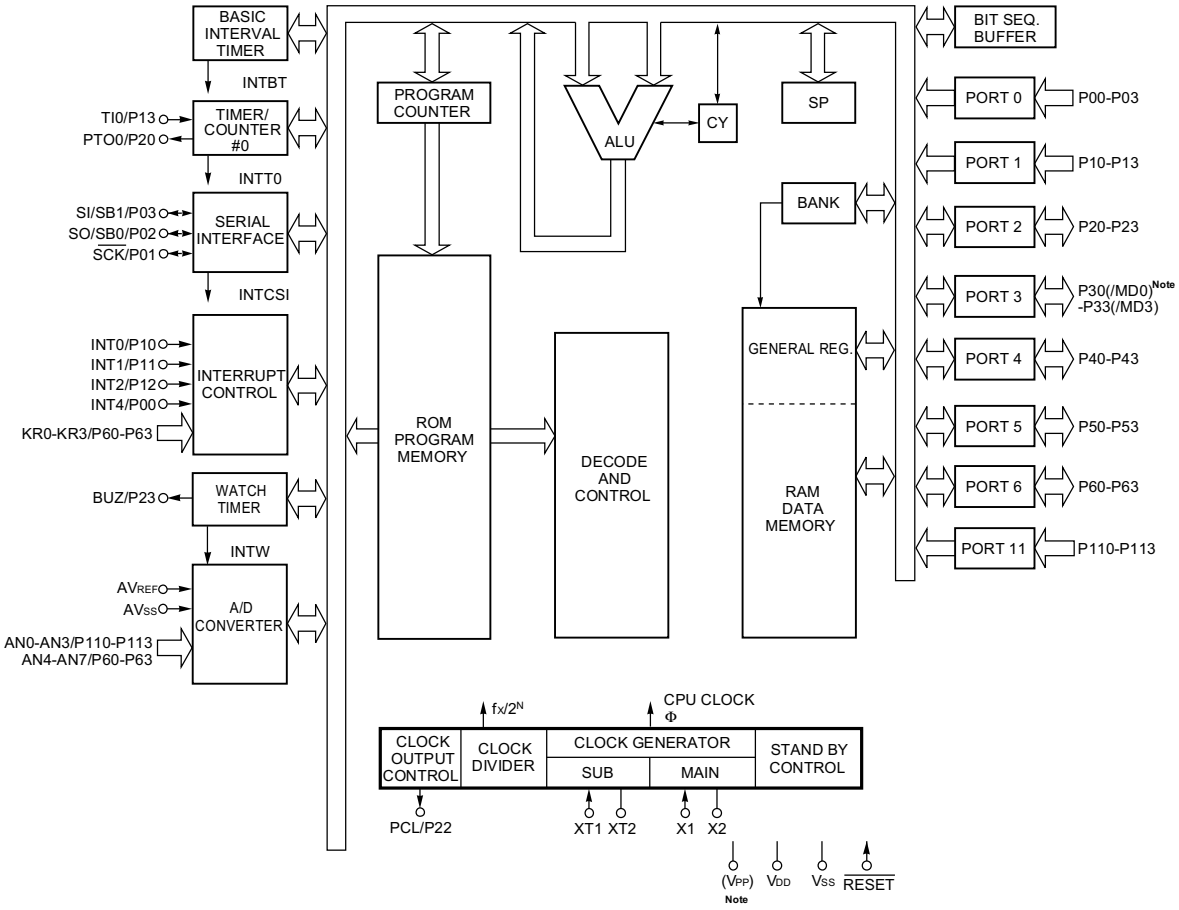
[Features]

- Contains A/D converter that can operate at low voltage.
  - 8-bit resolution × 8 channels (successive approximation)
  - Power supply voltage : V_{DD} = 2.7 to 6.0 V
- I/O ports : 32 lines
- Provides the on-chip PROM version that can operate at the same supply voltage as a mask ROM version
  - uPD75P068 (one-time PROM)

[Applications]

Home electronic appliances, cameras, air conditioners, fan heaters, sphygmomanometers, measuring instruments, etc.

Block Diagram



Note The pin name enclosed in parentheses applies to the μPD75P068.

Caution The internal ROM and RAM capacities vary depending on the product.

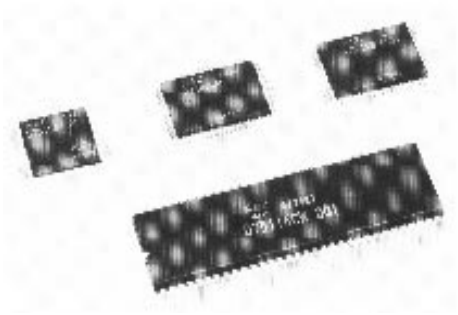
[Function List]

Item \ Part number			μPD75064/75066/75068	μPD75P068
ROM (bytes)			4K/6K/8K (mask ROM)	8K (one-time PROM)
RAM (× 4 bits)			512	
General purpose register			4 bits × 8 or 8 bits × 4	
Instruction cycle			0.95, 1.91, or 15.3 μs (main system clock: During 4.19-MHz operation) 122 μs (subsystem clock: During 32.768-kHz operation)	
Input/output port		Total	32	
		CMOS input	12 (seven lines can be pulled up by software)	
		CMOS input/output	12 (four lines can be pulled up by software and can drive LED directly)	
		N-ch open-drain input/output	8 (which are 10-V withstanding, can be pulled up by mask option and can drive LED directly)	Same as left (except that no mask option is provided)
A/D converter			• 8-bit resolution × 8 channels (successive approximation) • Can operate at low voltage: V_{DD} = 2.7 to 6.0 V	
Timer/counter			Three channels { • 8-bit timer/event counter • 8-bit basic interval timer • Watch timer	
Serial interface			• NEC standard serial bus interface (SBI) or clocked serial interface (3-line system) can be selected.	
Interrupt	External		• Three vectored interrupts • One test input	
	Internal		• Four vectored interrupts • One test input	
Power supply voltage			V_{DD} = 2.7 to 6.0 V	
Operating ambient temperature			T_a = –40 to +85°C	
Package			• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm)	

5.2 Control Series (μPD751××)

5.2.1 Control

Applicable products: μPD75104, 75106, 75108, 75112, 75116, 75104A, 75108A, 75P108B, 75P116



This series has been developed for application to machine control of consumer equipment system control and partial control of office automation equipment, automobiles, etc. For this purpose, it features an increased number of timers and improved input/output port function and interrupt function as compared with the μPD7508H, which is a μPD7500 series control product.

The μPD75104A and 75108A have been developed particularly for application to very small devices such as cameras and video camcorders. They use small package and an increased number of internal pull-up resistors (mask option).

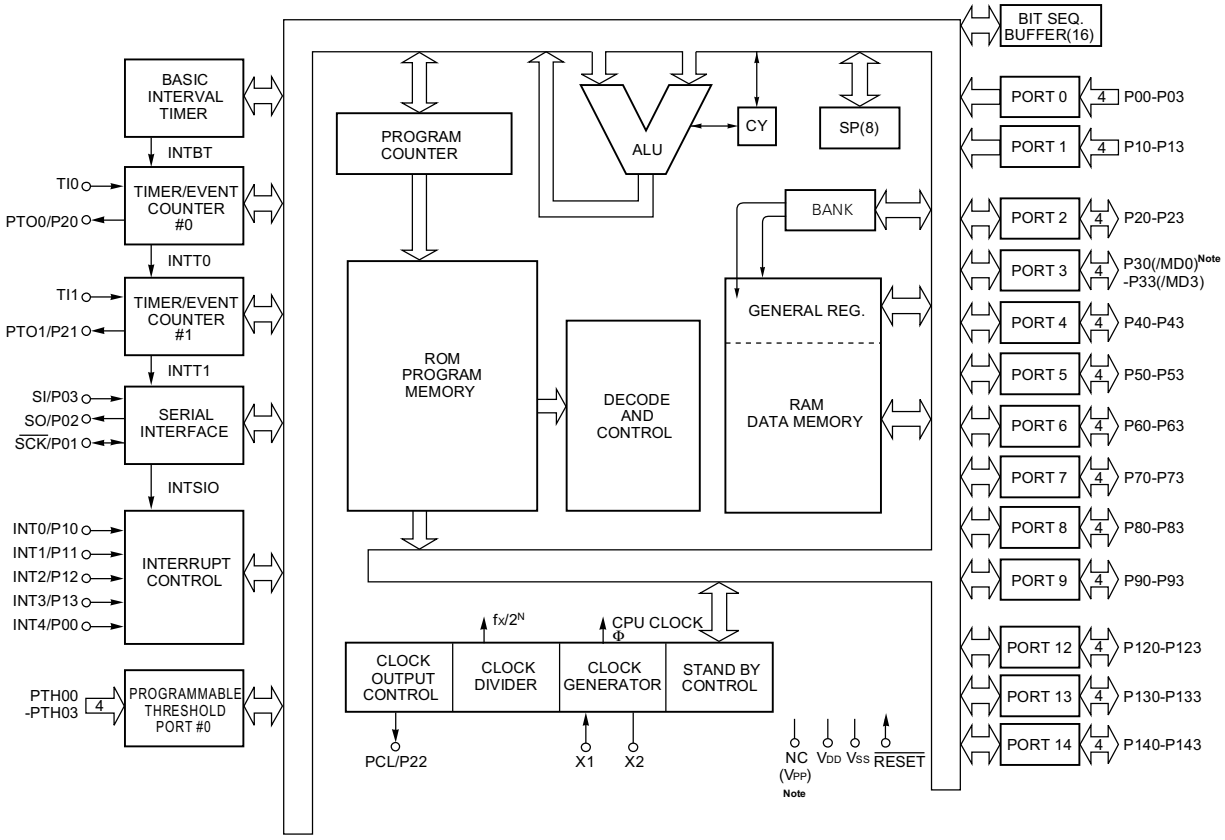
[Features]

- Instruction execution time variable function useful for highspeed operation and power saving.
  - 0.95, 1.91, or 15.3 μs (during 4.19-MHz operation)
- Powerful internal hardware
  - Timer: Three channels
  - Serial I/O: One channel
  - Interrupt sources: Seven
  - Various input/output ports: 58 lines
- Available as series of products with different internal memory capacities.
- PROM versions are provided:
  - μPD75P108B (one-time PROM, EPROM)
  - μPD75P116 (one-time PROM)

[Applications]

Video cassette recorders, audio equipment, telephones, cameras, radio equipment, home electric appliances, etc.

Block Diagram



Note The pin name enclosed in parentheses apply to μPD75P108B and 75P116.

Caution The internal ROM capacity and RAM capacity vary depending on the product.

[Function List]

Item \ Part number	μPD75104/106/108/112/116	μPD75104A/108A	μPD75P116	μPD75P108B
ROM (bytes)	4K/6K/8K/12K/16K (mask ROM)	4K/8K (mask ROM)	16K (One-time PROM)	8K (PROM Note 1)
RAM (× 4 bits)	320/320/512/512/512	320/512	512	
General purpose register	(4 bits × 8) × 4 banks or (8 bits × 4) × 4 banks			
Instruction cycle	0.95, 1.91, or 15.3 μs (main system clock: During 4.19-MHz operation)			
Input/output port — Total	58			
Input/output port — CMOS input	10 (also used for INT and SIO) Note 2	Same as left except that no mask option is provided		
Input/output port — CMOS input/output	32 (which can drive LEDs directly) Note 2			
Input/output port — N-ch open-drain input/output	12 (which can drive LEDs directly, are 12-V withstanding, and can be pulled up by mask option)			
Input/output port — Analog input	4 (4-bit precision)			
Timer/counter	Three channels { • 8-bit timer/event counter : Two channels • 8-bit basic interval timer : One channel			
Serial interface	• MSB or LSB can be selected for the date transfer top bit. • Serial bus configuration is enabled.			
Interrupt	Multiple interrupts are enabled by hardware.			
Interrupt — External	• Three vectored interrupts • Two test inputs			
Interrupt — Internal	• Four vectored interrupts			
Instruction set	• 1-bit data set, reset, test, and Boolean operations • 4-bit data transfer, operations, increment and decrement, and comparison • 8-bit data transfer, operations, increment and decrement, and comparison			
Power supply voltage	V_{DD} = 2.7 to 6.0 V		V_{DD} = 5 V ± 10 %	V_{DD} = 2.7 to 6.0 V
Operating ambient temperature	T_a = –40 to +85°C			
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic QFP (14 × 14 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm) • 64-pin ceramic shrink DIP (750 mil)

Notes 1. One-time PROM, EPROM

2. Only μPD75104A and 75108A can contain an on-chip pull-up resistor using mask options of four CMOS input and 24 CMOS input/output ports.

5.2.2 Low voltage, high-speed control

Applicable products: μPD75108F, 75112F, 75116F

The μPD751××F is a high-speed operation version of the μPD751×× at a low voltage. Both products have the same function and their pins are compatible; a set for which high-speed operation is required can be easily operated at a low voltage.

In particular, the μPD751××F is appropriate for cordless telephone handsets, pagers, etc.

However, note that the μPD751××F differs from the μPD751×× in the power supply voltage range.

Two types of μPD751×× PROM versions, μPD75P108B and 75P116, can be used for evaluation during system development[Note].

Note The μPD75P108B and 75P116 differ from the μPD751××F in some of their electrical characteristics.

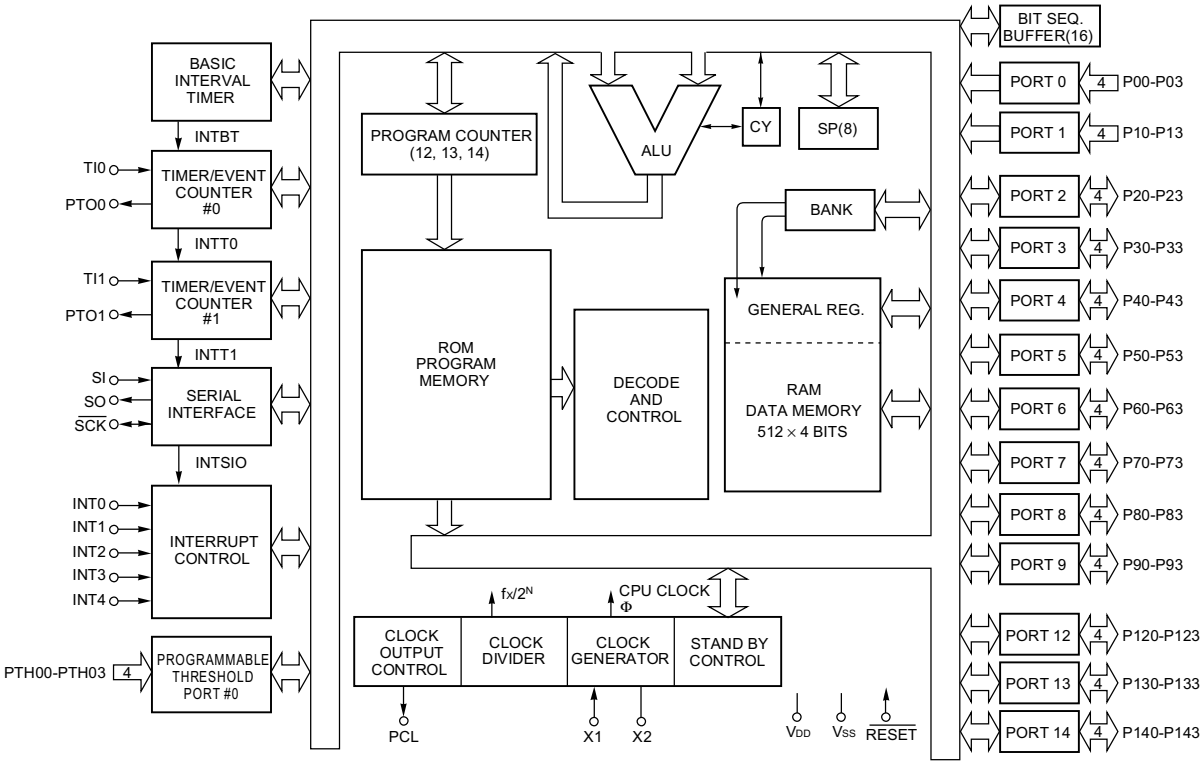
[Features]

- Allows a high-speed operation at low-voltage
  Minimum instruction execution time μPD751××F: 1.91 μs (V_{DD} = 2.7 V)
  μPD751×× : 3.8 μs (V_{DD} = 2.7 V)
- Has the same function as the μPD751×× and the pins are compatible
- Power supply voltage : 2.7 to 5.0 V (T_A = –40 to +50°C)
  : 2.8 to 5.0 V (T_A = –40 to +60°C)
- Package: 64-pin plastic QFP (14×20 mm)
- Development tools common to μPD751××

[Applications]

Cordless telephone handset, pager, portable radio equipment, etc.

Block Diagram

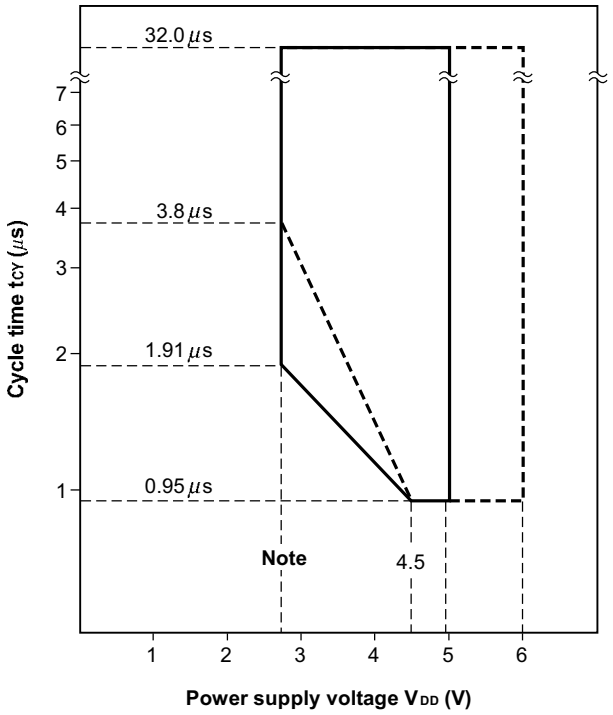


Caution The internal ROM capacity varies depending on the product.

[Function List]

Item \ Part number	μPD751××F			μPD751××		
	μPD75108F	μPD75112F	μPD75116F	μPD75108	μPD75112	μPD75116
Minimum instruction execution time	1.91 μs (V_{DD} = 2.7 V) 0.95 μs (V_{DD} = 4.5 V)			3.8 μs (V_{DD} = 2.7 V) 0.95 μs (V_{DD} = 4.5 V)		
Power supply voltage	V_{DD} = 2.7 to 5.0 V (T_A = –40 to +50°C) V_{DD} = 2.8 to 5.0 V (T_A = –40 to +60°C)			V_{DD} = 2.7 to 6.0 V		
Operating ambient temperature	–40 to +60°C			–40 to +85°C		
Power on reset circuit	None			Contained (mask option)		
Power on flag						
ROM	Mask ROM					
	8K	12K	16K	8K	12K	16K
RAM	512 × 4 bits					
I/O line	58					
Open-drain withstanding	10 V			12 V		
Package	• 64-pin plastic QFP (14 × 20 mm)			• 64-pin plastic QFP (14 × 20 mm) • 64-pin plastic shrink DIP (750 mil)		

Operation range comparison between μPD751××F and μPD751×× (main clock of 4.19 MHz and crystal resonator are used)

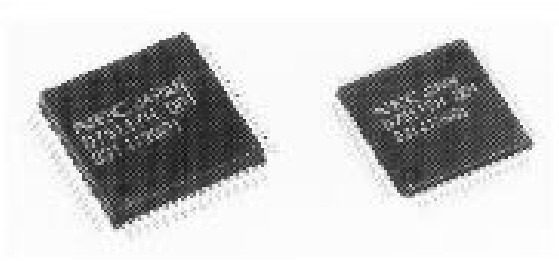


The portion surrounded by the thick solid line : μPD751××F
The portion surrounded by the thick broken line : μPD751××

Note μPD751×× and μPD751××F (T_A = –40 to +50 °C): 2.7 V
μPD751××F (T_A = –40 to +60 °C): 2.8 V

5.2.3 F product + low voltage

Applicable products: μPD75116H, 75117H, 75P117H



The μPD751××H has the same function as the μPD751××F, and the lowest operation voltage is changed to 1.8 V from 2.7 V. In addition, the μPD751××H can perform 1.91-μs operation at 1.8 V, thus it enables a set required for high speed operation to operate at lower voltage. This device is appropriate for the control of cordless telephone handsets, pagers, etc.

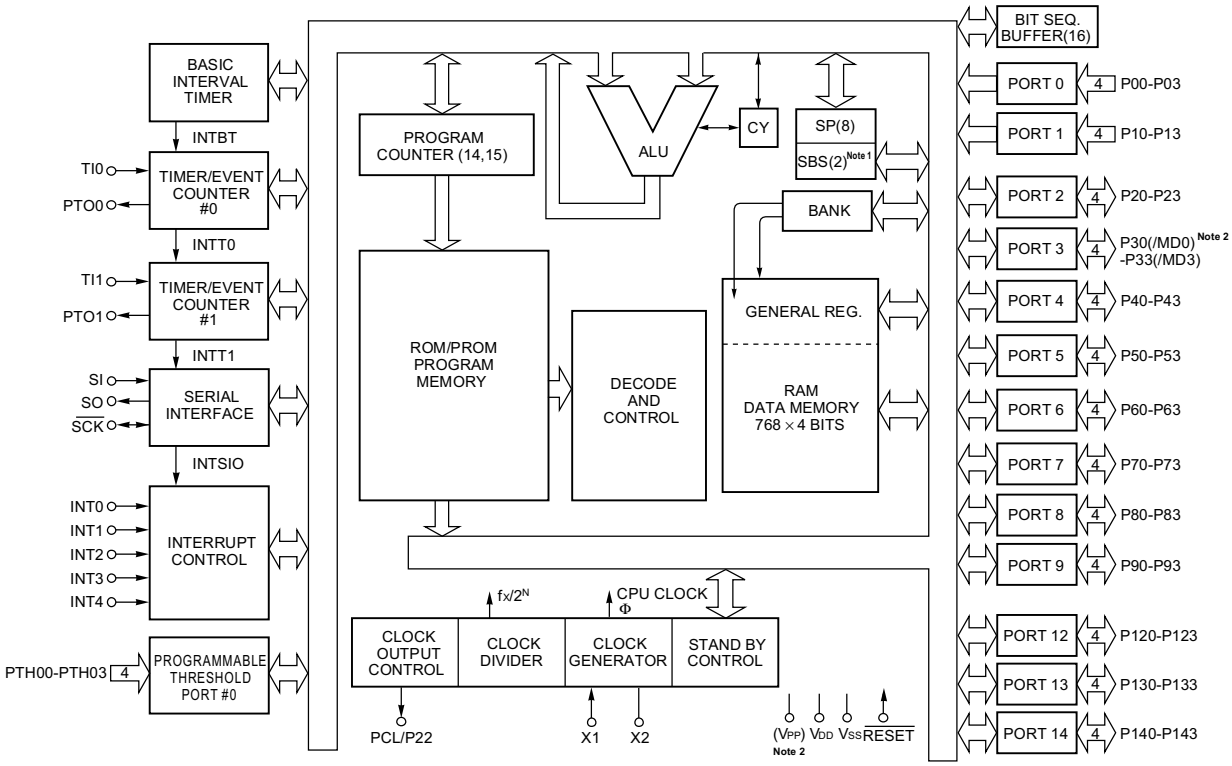
[Features]

- Equivalent function and pin compatible with the μPD751××F
- Allows a high-speed operation at low voltage.
  - Minimum instruction execution time:
    1.91 μs (V_{DD} = 1.8 V)
    0.95 μs (V_{DD} = 2.7 V)
- Power supply voltage:
    1.8 to 5.5 V (T_A = –40 to +60°C)

[Applications]

Handsets of cordless telephone, portable radio equipment, pagers, etc.

Block Diagram



Notes 1. μPD75117H and 75P117H only

2. The pin name enclosed in parentheses applies to the μPD75P117H.

Caution The internal ROM capacity varies depending on the product.

[Function List]

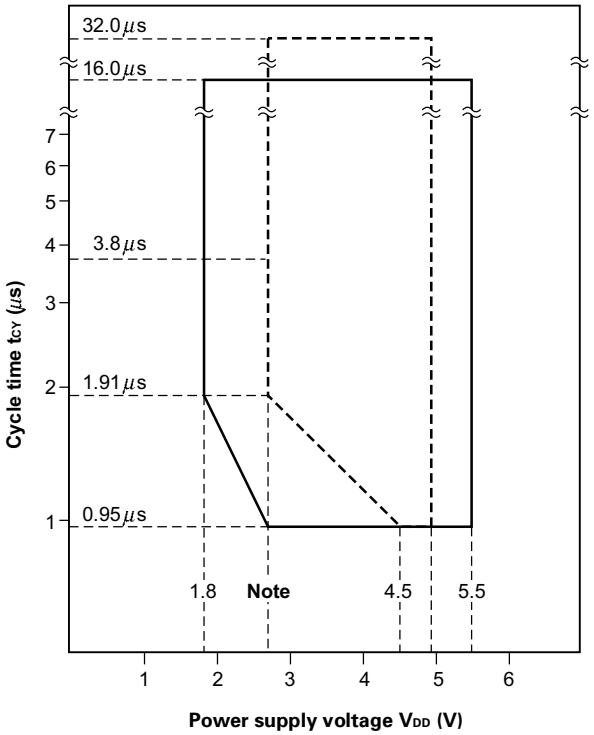
Item \ Part number	μPD751××			μPD751××F			μPD751××H		
	μPD75108	μPD75112	μPD75116	μPD75108F	μPD75112F	μPD75116F	μPD75116H	μPD75117H	μPD75P117H
ROM (bytes)	Mask ROM								PROM[Note1]
	8K	12K	16K	8K	12K	16K	16K	24K	
RAM (× 4 bits)	512						768		
General purpose register	(4 bits × 8) × 4 banks or (8 bits × 4) × 4 banks								
Instruction set	75X High-End							75X expansion High-End [Note2]	
Instruction cycle	0.95 μs, 1.91 μs, or 15.3 μs (system clock: During 4.19-MHz operation)								
Minimum instruction execution time	3.8 μs (V_{DD} = 2.7 V) 0.95 μs (V_{DD} = 4.5 V)			1.91 μs (V_{DD} = 2.7 V) 0.95 μs (V_{DD} = 4.5 V)			1.91 μs (V_{DD} = 1.8 V) 0.95 μs (V_{DD} = 2.7 V)		
Input/output port: Total	58								
Input/output port: CMOS input	10								
Input/output port: CMOS input/output	32 (All these lines can drive LEDs directly.)						32 lines (8 of these can drive LEDs directly.)		
Input/output port: N-ch open-drain output	12 (All these lines can drive LEDs directly.)						12 lines		
Input/output port: Withstanding	12 V			10 V			6 V		
Input/output port: Pull-up resistor	On-chip possible with mask option								None
Input/output port: Analog input	4 (4-bit precision)								
Power-on reset circuit	On-chip (mask option)			None					
Power-on flag									
Power supply voltage	2.7 to 6.0 V			2.7 to 5.0 V (T_A = −40 to +50°C) 2.8 to 5.0 V			1.8 to 5.5 V		
Operating ambient temperature	−40 to +85°C			−40 to +60°C					
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)			• 64-pin plastic QFP (14 × 20 mm)			• 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic QFP (12 × 12 mm) • 64-pin ceramic WQFN (μPD75P117H)		

Notes 1. One-time PROM, EPROM

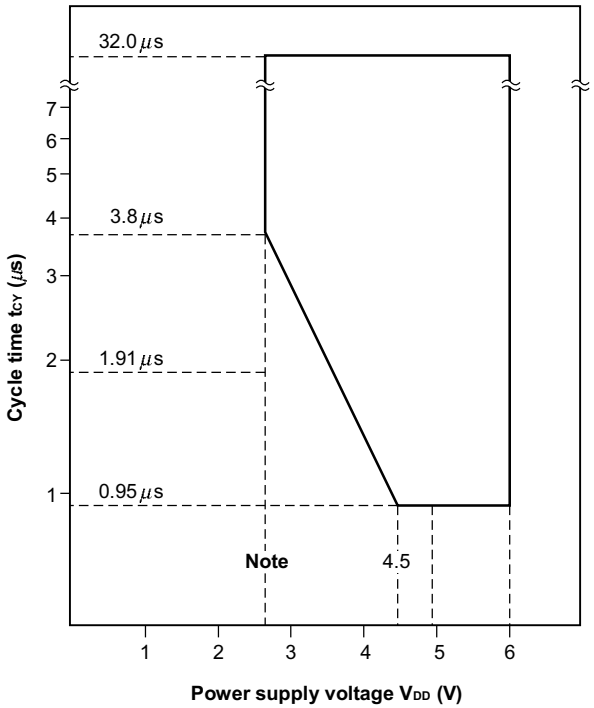
2. The μPD75P117H can be used as a 75X High-End by switching 16- or 24-Kbytes mode.

μPD751××H, μPD751××F and μPD751×× operation ranges (main clock of 4.19 MHz and crystal resonator are used)

- **Comparison between μPD751××H and μPD751××F**



- **μPD751××**



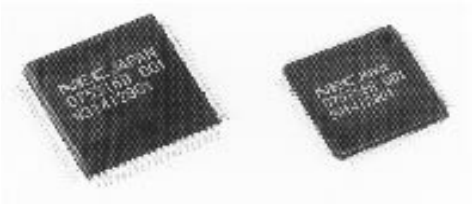
Surrounded by thick solid line : μPD751××H
Surrounded by thick broken line : μPD751××F

Note μPD751××F (T_A = –40 to +50°C) : 2.7 V
μPD751××F (T_A = –40 to +60°C) : 2.8 V
μPD751××H : 2.7 V

5.3 LCD Drive Series (μPD753××)

5.3.1 LCD driving

Applicable products: μPD75304, 75306, 75308, 75304B, 75306B, 75308B, 75P308, 75P316A, 75P316B



The μPD7530× contains an LCD panel controller/driver and features rich hardware which enables easy use, such as serial bus interface (SBI) and key input for standby mode release. The μPD7530× is appropriate for devices using LCD display.

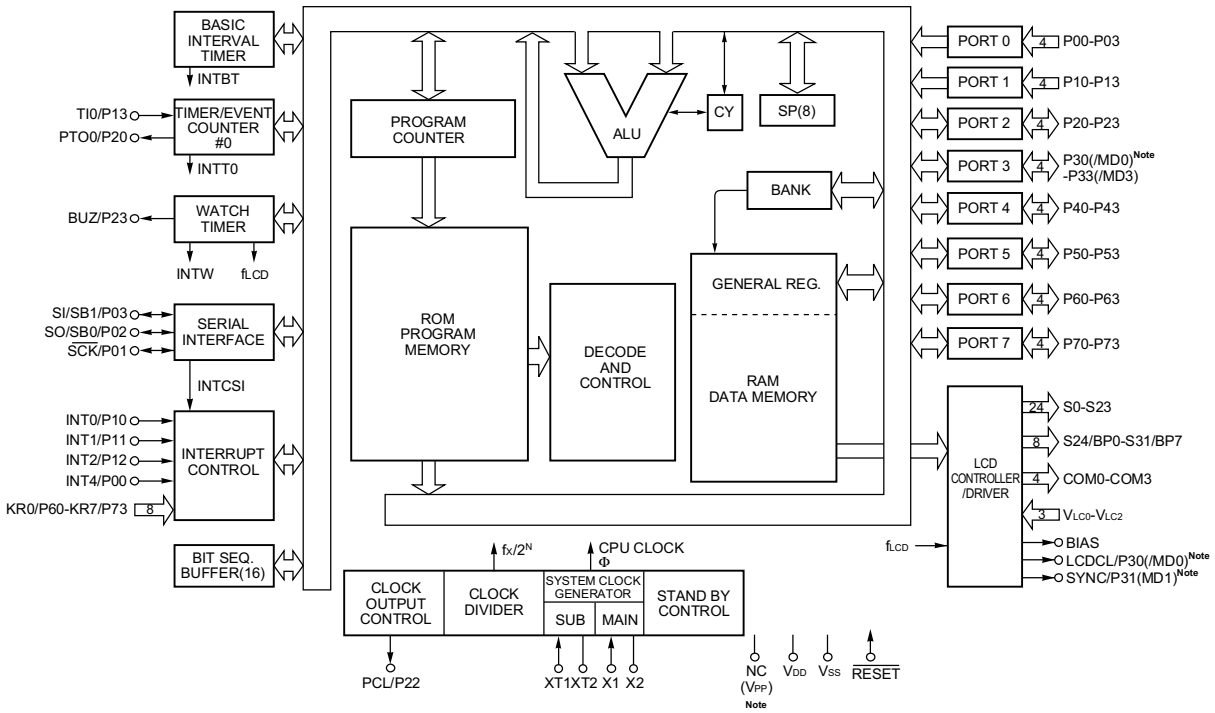
[Features]

- Instruction execution time variable function useful for high-speed operation and power saving
  - 0.95, 1.91, or 15.3 μs (during 4.19-MHz operation)
  - 122 μs (during 32.768-kHz operation)
- Contains a programmable LCD controller/driver.
- Contains an NEC standard serial bus interface (SBI).
- Enables watch operation with very low power consumption (5 μA TYP.: During 3-V operation)
- Enhanced timer function: Three channels
- Interrupt function attaching importance to application such as remote control reception.
- Each of 31 I/O lines can contain a pull-up resistor.
  - Middle-voltage N-ch open-drain input/output ports: Eight lines
- Low-voltage version products are provided:
  - μPD75304B, 75306B, 75308B (V_{DD} = 2.0 to 6.0 V, LCD drive voltage = 2.0 V to V_{DD})
- PROM version products are provided:
  - μPD75P308 (one-time PROM, EPROM)
  - μPD75P316A (one-time PROM, EPROM)
  - μPD75P316B (one-time PROM, EPROM)
- On-chip low-voltage PROMs are provided:
  - μPD75P316A (V_{DD} = 2.7 to 6.0 V)
  - μPD75P316B (V_{DD} = 2.0 to 6.0 V)

[Applications]

Video camcorders, compact disc players, telephones, cameras, sphygmomanometers, pagers, etc.

Block Diagram



Note The pin name enclosed in parentheses applies to μPD75P308, 75P316A, and 75P316B.

Caution The internal ROM capacity and RAM capacity vary depending on the products.

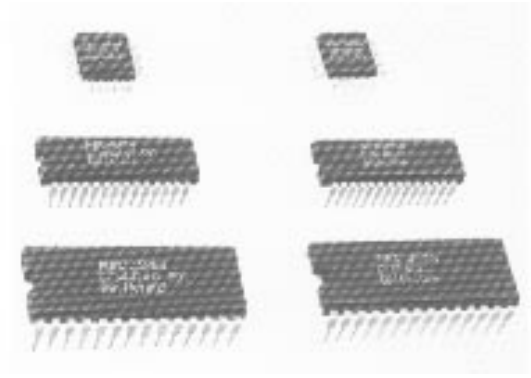
[Function List]

Item \ Part number	μPD75304/306/308	μPD75304B/306B/308B	μPD75P308	μPD75P316A	μPD75P316B
ROM (bytes)	4K/6K/8K (mask ROM)		8K (PROM[Note])	16K (PROM[Note])	
RAM (× 4 bits)	512			1024	
General purpose register	4 bits × 8 or 8 bits × 4				
Instruction cycle	0.95, 1.91, or 15.3 μs (Main system clock: During 4.19-MHz operation) 122 μs (Subsystem clock: During 32.768-kHz operation)				
Input/output port — Total	40				
Input/output port — CMOS input	8 (internal pull-up resistor can be specified by software: 7 lines)				
Input/output port — CMOS input/output	16 (internal pull-up resistor can be specified by software: 16 lines)				
Input/output port — CMOS output	8 (also used for segment output)				
Input/output port — N-ch open-drain input/output	8 (10-V withstanding, can be pulled up by mask option)		8 (10-V withstanding, no mask option)		
Display output	36 lines • Segment output: 32 • Common output: 4				
LCD controller/driver	• Common output: Static, 1/2, 1/3, 1/4 duty selectable • Segment output: 24/28/32 segments (3 steps variable)				
LCD controller/driver	Can incorporate LCD drive division resistors using a mask option		LCD drive division resistors unavailable		
LCD controller/driver	2.5 V to V_{DD}	2.0 V to V_{DD}			
Timer/counter	3 channels { • 8-bit timer/event counter • 8-bit basic interval timer • Watch timer				
Serial interface	• NEC standard serial bus interface (SBI)/clocked serial interface (3-line system) selectable				
Vectored interrupt	• External: 3 • Internal: 3				
Test input	• External: 1 • Internal: 1				
Power supply voltage	V_{DD} = 2.7 to 6.0 V	V_{DD} = 2.0 to 6.0 V	V_{DD} = 5 V ± 5 %	V_{DD} = 2.7 to 6.0 V	V_{DD} = 2.0 to 6.0 V
Operating ambient temperature	−40 to +85°C		−10 to +70°C	−40 to +85°C	
Package	• 80-pin plastic QFP (14 × 20 mm)	• 80-pin plastic QFP (14 × 14 mm) (14 × 20 mm) • 80-pin plastic TQFP (fine pitch)(12 × 12 mm)	• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic WQFN	• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic WQFN	• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm) • 80-pin ceramic WQFN

Note One-time PROM, EPROM

5.4 Submicrocontroller Series (μPD754××)

Applicable products: μPD75402A, 75P402



This series provides small general purpose microcontrollers each containing NEC standard serial bus interface (SBI) in addition to general purpose input/output ports.

In the system configuration in which 75X, 75XL, or 78K is used as host microcontrollers, this series is applicable to intelligent submicrocontrollers for key input control, display control such as LED, and remote control transfer control by making the most of the NEC standard serial bus interface (SBI). It is also applicable to small system control.

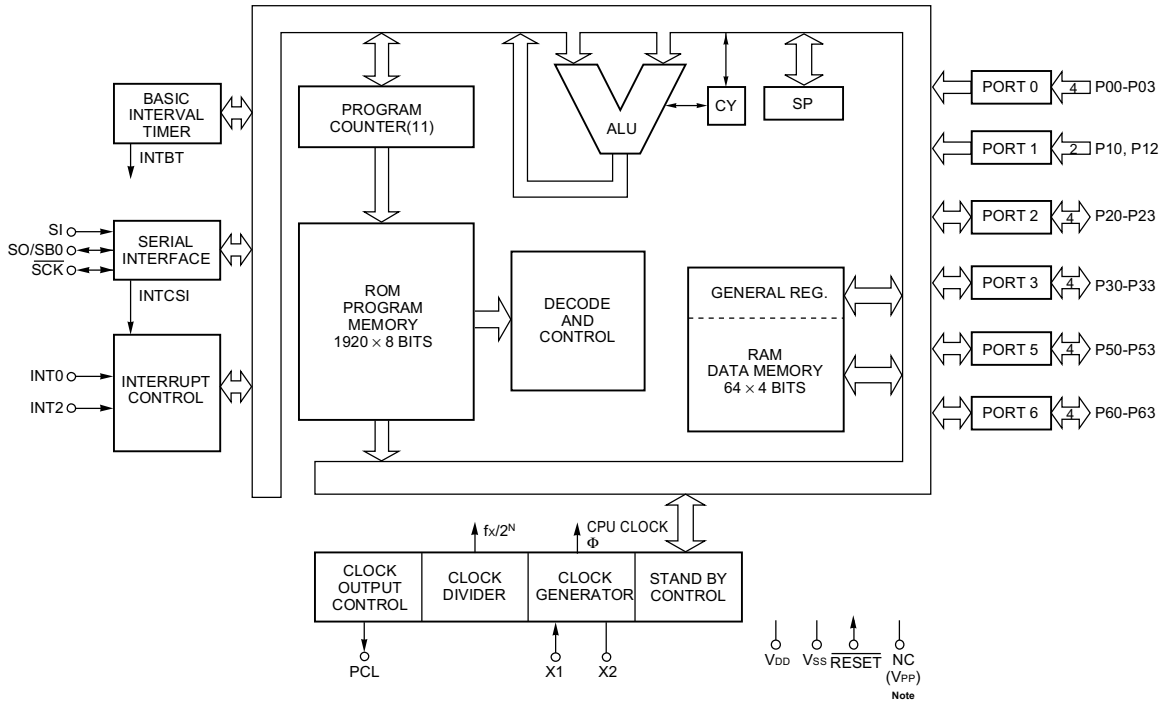
[Features]

- High-speed operation, minimum instruction execution time: 0.95 μs (during 4.19-MHz operation)
- Low-speed instruction execution time at low voltage: 15.3 μs (during 4.19-MHz operation)
- On-chip peripheral hardware is mapped in memory.
- NEC standard serial bus interface
  - Two transfer modes (clocked 3-line mode and SBI mode) can be used.
- 8-bit basic interval timer (applicable to a watchdog timer)
- Interrupt function
  - Three vectored interrupts: One external and two internal
  - One external test input
- Clock output function (applicable to remote output) control
- Specifiable for on-chip pull-up resisters by software : 16 pins
- Provides on-chip PROM versions (compatible with μPD27C256A):
  μPD75P402 (one-time PROM)

[Applications]

Facsimiles, plain paper copiers, printers, video cassette recorders, remote controllers, etc.

Block Diagram



Note The pin name enclosed in parentheses applies to the μPD75P402.

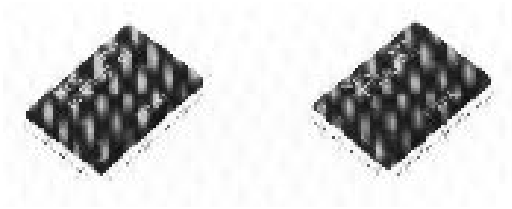
[Function List]

Item \ Part number			μPD75402A	μPD75P402
ROM (bytes)			1.9K (mask ROM)	1.9K (one-time PROM)
RAM (× 4 bits)			64	
General purpose register			4 bits × 4 or 8 bits × 2	
Instruction cycle			0.95, 1.91, or 15.3 μs (during 4.19-MHz operation)	
Input/ output port		Total	22	
		CMOS input	6 (used as both INT and SIO: 4 lines can be pulled up by software.)	Same as left except that no mask option is provided
		CMOS input/output	12 (eight lines drive LEDs; 12 lines can be pulled up by software)	
		N-ch open-drain input/output	4 (which drive LEDs, are 10-V withstanding, and can be pulled up by mask option	
Timer/counter			• Basic interval timer	
Serial interface			• NEC standard serial bus interface (SBI) or clocked serial interface (3-line system) selectable.	
Interrupt		External	• One vectored interrupt • One test input	
		Internal	• Two vectored interrupts	
Instruction set			• 1-bit data set, reset, test, and Boolean operations • 4-bit data transfer, operations, increment and decrement, and comparison • 8-bit data transfer	
Power supply voltage			V_{DD} = 2.7 to 6.0 V	V_{DD} = 5 V ± 10 %
Operating ambient temperature			–40 to +85°C	–10 to +70°C
Package			• 28-pin plastic DIP (600 mil) • 28-pin plastic Shrink DIP (400 mil) • 44-pin plastic QFP (10 × 10 mm)	

5.5 Control Series (with on-chip A/D Converter) (μPD755××)

5.5.1 Control (with on-chip A/D converter)

Applicable products: μPD75512, 75516, 75P516



The microcontrollers of this series have been developed for application to machine control of consumer products, office automation equipments, and industrial devices.

An A/D converter which can easily input from analog circuit is contained for machine control. Two serial interface channels are contained for easy connection to display devices, etc. For example, if the μPD75516 is applied to a video cassette recorder, the system control part and timer part conventionally made up of two chips can be integrated into one chip for cost reduction.

[Features]

64 I/O lines

On-chip two 8-bit serial interface channels

- NEC standard serial bus interface (SBI).

On-chip eight 8-bit A/D converter channels.

Instruction execution time variable function useful for power saving and high-speed operation

- 0.95, 1.91, or 15.3 μs (during 4.19-MHz operation)
- 122 μs (during 32.768-kHz operation)

Powerful timer function: Four channels

- 8-bit timer/event counter
- Watch timer
- 8-bit basic interval timer
- Timer/pulse generator: Can output 14-bit PWM.

A pull-up or pull-down resistor can be contained for each of 47 I/O lines.

Watch operation can be performed with very low power consumption (5 μA TYP. during 3-V operation).

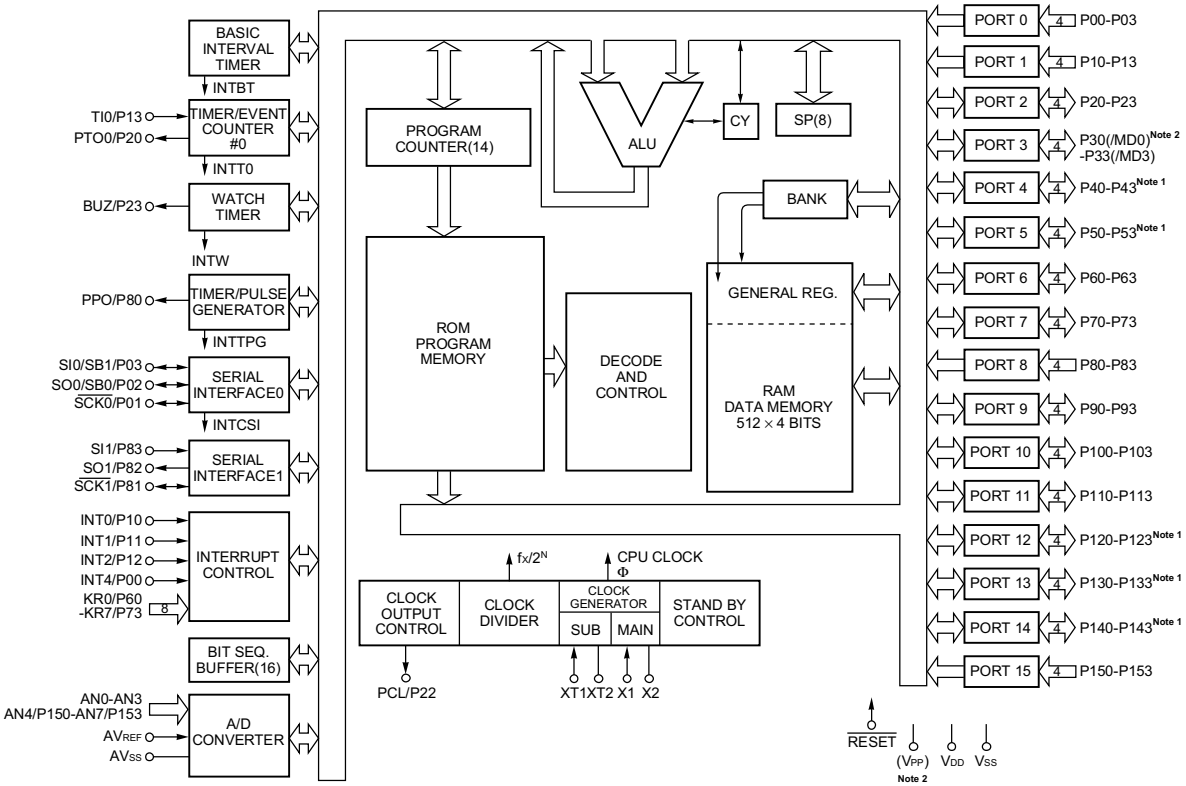
PROM version:

μPD75P516 (one-time PROM, EPROM)

[Applications]

Video cassette recorders, compact disk players, telephones, cameras, etc.

Block Diagram



Notes 1. PORT4, PORT5, and PORT 12 to PORT14 are middle-withstanding N-ch open-drain input/output ports.

2. The pin name enclosed in parentheses applies to μPD75P516.

Caution The internal ROM capacity varies depending on the product.

[Function List]

Item \ Part number		μPD75512	μPD75516	μPD75P516
ROM (bytes)		12K (mask ROM)	16K (mask ROM)	16K (PROM[Note])
RAM (× 4 bits)		512		
General purpose register		(4 bits × 8) × 4 banks or (8 bits × 4) × 4 banks		
Instruction cycle		0.95, 1.91, or 15.3 μs (main system clock: During 4.19-MHz operation) 122 μs (subsystem clock: During 32.768-kHz operation)		
Input/output port	Total	64		
	CMOS input	16 (also used for INT, SIO PPO and analog input; seven lines can be pulled up by software)		Same as left (except that no mask option is provided)
	CMOS input/output	28 (LED drive: 4) • 16 can be pulled up by software • 4 can be pulled down by mask option		
	N-ch open-drain input/output	20 (LED drive: Eight lines, 10-V voltage, 20 lines can be pulled up by mask option)		
A/D converter		• 8-bit resolution × 8 channels (successive approximation)		
Timer/counter		4 channels { • Timer/event counter • Basic interval timer • Timer/pulse generator (which can perform 14-bit PWM output) • Watch timer		
Serial interface		2 channels { • NEC standard serial bus interface (SBI)/3-line SIO: One channel • Normal clocked serial interface (3-line SIO): One channel		
Interrupt		Multiple interrupts are enabled by hardware.		
	External	• Three vectored interrupts • One test input		
	Internal	• Four vectored interrupts • One test input		
Instruction set		• 1-bit data set, reset, test, and Boolean operations • 4-bit data transfer, operations, increment and decrement, and comparison • 8-bit data transfer, operations, increment and decrement, and comparison		
Power supply voltage		V_{DD} = 2.7 to 6.0 V		V_{DD} = 4.75 to 5.5 V
Operating ambient temperature		–40 to +85°C		–10 to +70°C
Package		• 80-pin plastic QFP (14 × 20 mm)		• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic WQFN

Note One-time PROM, EPROM

5.5.2 Control (using on-chip A/D converter) + high speed

Applicable products: μPD75517, 75518, 75P518

The minimum instruction execution time of the μPD75517, 75518, 75P518 is put into high speed (0.67 μs from 0.95 μs) and the ROM and RAM capacity is enlarged, as compared with the former product, μPD75516. The μPD75517, 75518, and 75P518 are high-performance products appropriate for video cassette recorders, air conditioners, and fan heaters due to their enhanced 75X series processing capabilities.

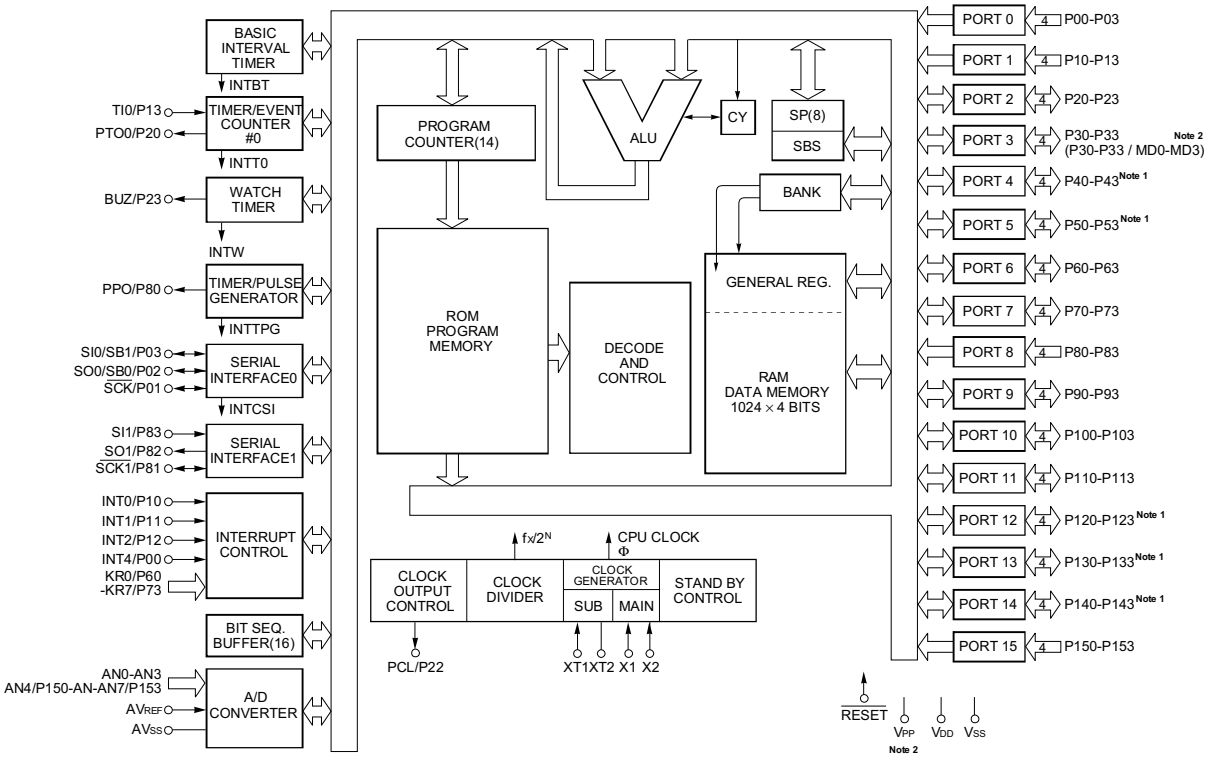
[Features]

- Instruction execution time variable function useful for highspeed operation and power saving
  - 0.67, 1.33, 2.67, or 10.7 μs (during 6.0-MHz operation)
  - 122 μs (during 32.768-kHz operation)
- Contains an A/D converter that can operate at low voltage
  - 8-bit resolution × 8 channels (successive approximation)
  - V_{DD} = 2.7 to 6.0 V
- Many I/O lines: 64
- Contains two channels of 8-bit serial interface
  - NEC standard serial bus interface (SBI)
- Enables watch operation with very low power consumption (5 μA TYP.: During 3-V operation).
- A PROM version product that can operate at the same supply voltage as a mask ROM product, is provided:
  - μPD75P518 (one-time PROM, EPROM)

[Applications]

Video cassette recorders, compact disc players, telephones, air conditioners, etc.

Block Diagram



Notes 1. PORT4, PORT5, and PORT12 to PORT14 are 10-V middle-voltage N-ch open drain input/output ports.

2. μPD75P518 only

Caution The internal ROM capacity varies depending on the product.

[Function List]

Item \ Part number		μPD75517	μPD75518	μPD75P518
ROM (bytes)		24K (mask ROM)	32K (mask ROM)	32K (PROM[Note])
RAM (× 4 bits)		1024		
General purpose register		(4 bits × 8) × 4 banks or (8 bits × 4) × 4 banks		
Instruction cycle	Main system clock	0.67, 1.33, 2.67, or 10.7 μs (during 6.0-MHz operation) 0.95, 1.91, 3.82, or 15.3 μs (during 4.19-MHz operation)		
	Subsystem clock	122 μs (during 32.768-kHz operation)		
Input/output port	Total	64		
	CMOS input	16 (also used for INT SIO, PPO and analog input; 7 can be pulled up by software)		Same as left (except that no mask option is provided)
	CMOS input/output	28 (LED drive: 4) • 16 can be pulled up by software • 4 can be pulled down by mask option		
	N-ch open-drain input/output	20 (LED drive: Eight lines, 10-V withstanding, 20 can be pulled up by mask option)		
A/D converter		• 8-bit resolution × 8 channels (successive approximation) • Operating voltage: V_{DD} = 2.7 to 6.0 V		
Timer/counter		4 • Timer/event counter • Basic interval timer • Timer/pulse generator (which can perform 14-bit PWM output) • Watch timer		
Serial interface		2 • NEC standard serial bus interface (SBI)/3-line SIO: 1 channel • Normal clocked serial interface (3-line SIO): 1 channel		
Interrupt		Multiple interrupts are enabled by hardware.		
	External	• Three vectored interrupts • One test input		
	Internal	• Four vectored interrupts • One test input		
Instruction set		• 1-bit data set, reset, test, and Boolean operations • 4-bit data transfer, operations, increment and decrement, and comparison • 8-bit data transfer, operations, increment and decrement, and comparison		
Power supply voltage		V_{DD} = 2.7 to 6.0 V		
Operating ambient temperature		–40 to +85°C		–10 to +70°C
Package		• 80-pin plastic QFP (14 × 20 mm)		• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic WQFN

Note One-time PROM, EPROM

6. 75X SERIES INSTRUCTION SET

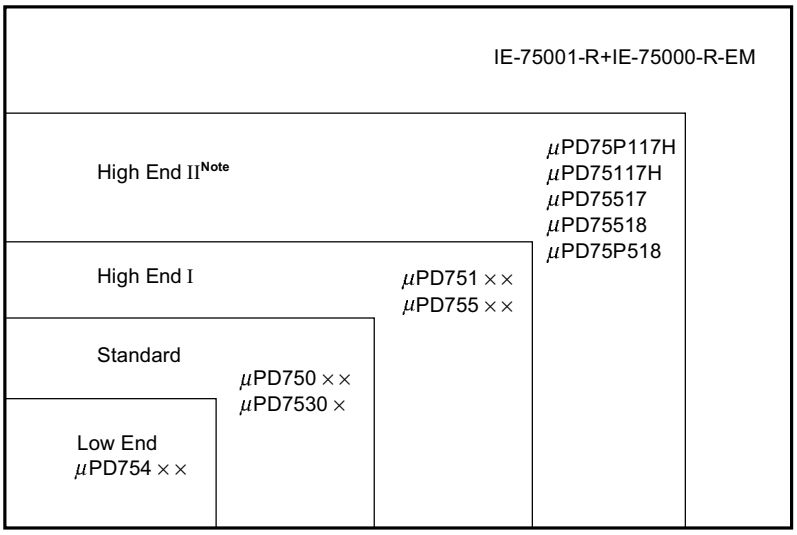
The 75X series instruction set is an enhanced version of the instruction set of the μPD7500 series, which is the predecessor of the 75X series. It is a new epoch-making instruction set that maintains continuity from the μPD7500 series. The 75X series instruction set has the following features:

(1) 1-bit manipulation instructions applicable to various purposes
(2) Efficient 4-bit manipulation instructions
(3) 8-bit manipulation instructions matching 8-bit microcomputer instructions
(4) GETI instruction for program size reduction
(5) String effect and notation adjustment instructions to raise program efficiency
(6) Table look-up instructions appropriate for consecutive reference
(7) 1-byte relative branch instructions
(8) NEC standard mnemonics arranged in an easy-to-understand manner

The 75X series products differ slightly in available instructions. Figure 6-1 shows the basic 75X series instruction system.

For the available instructions, see the following pages.

Figure 6-1. 75X Series Instruction System



Note These products increase in the number of instructions by enlarging the ROM capacity, as compared with other products of the same series.

The operand field of each instruction is described in the table below. (For details, see the RA75X Assembler Package User's Manual, Language (EEU-1363)).

- Select one of the entries under description.

  Example reg under Operands means one of X to L registers. Describe one of the X to L registers.

- Describe uppercase alphabetic characters and + and – symbols exactly as shown.
- Describe a numeric value for immediate data.
- Symbols can also be described.

Table 6-1. Operand Description

Identifier	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1 rp'2	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL' XA, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label Note1 2-bit immediate data or label
fmem pmem	FB0H-FBFH, FF0H-FFFH immediate data or label FC0H-FFFH immediate data or label
addr Note2 addr1 Note2 caddr faddr	0000H-3FFFH immediate data or label 0000H-7FFFH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H-7FH immediate data (bit = 0) or label
PORTn Note2 IE××× Note2 RBn Note2 MBn Note2	PORT0-PORT15 IEBT, IESIO, IET0, IET1, IETPG, IE0, IE1, IEKS, IEW, IE4, IECSI, IEMFT, IEEE, IEOW RB0-RB3 MB0-MB7, MB15

Notes 1. For 8-bit data operation, only an even address can be specified.

2. These identifiers vary depending on the product.

Instruction group	Mnemonic	Operands	No. of bytes	No. of machine cycle	Operation	Skip condition	High-End II	High-End I	Standard	Low-End
Transfer	MOV	A,#n4	1	1	A←n4	String effect A	○		○	○
		reg1,#n4	2	2	reg1←n4		○		○	
		XA,#n8	2	2	XA←n8	String effect A	○		○	○
		HL,#n8	2	2	HL←n8	String effect B	○		○	○
		rp2,#n8	2	2	rp2←n8		○		○	
		A,@HL	1	1	A←(HL)		○		○	○
		A,@HL+	1	2+S	A←(HL), then L←L+1	L=0	○			
		A,@HL–	1	2+S	A←(HL), then L←L–1	L=FH	○			
		A,@rpa1	1	1	A←(rpa1)		○		○	
		XA,@HL	2	2	XA←(HL)		○		○	
		@HL,A	1	1	(HL)←A		○		○	○
		@HL,XA	2	2	(HL)←XA		○		○	
		A,mem	2	2	A←(mem)		○		○	○
		XA,mem	2	2	XA←(mem)		○		○	○
		mem,A	2	2	(mem)←A		○		○	○
		mem,XA	2	2	(mem)←XA		○		○	○
		A,reg	2	2	A←reg		○		○	
		XA,rp'	2	2	XA←rp'		○		○	
		reg1,A	2	2	reg1←A		○		○	
		rp'1, XA	2	2	rp'1←XA		○		○	
	XCH	A,@HL	1	1	A↔(HL)		○		○	○
		A,@HL+	1	2+S	A↔(HL), then L←L+1	L=0	○			
		A,@HL–	1	2+S	A↔(HL), then L←L–1	L=FH	○			
		A,@rpa1	1	1	A↔(rpa1)		○		○	
		XA,@HL	2	2	XA↔(HL)		○		○	
		A,mem	2	2	A↔(mem)		○		○	○
		XA,mem	2	2	XA↔(mem)		○		○	○
		A,reg1	1	1	A↔reg1		○		○	○
		XA,rp'	2	2	XA↔rp'		○		○	
		HL,mem	2	2	HL↔(mem)					
	MOVT	XA,@PCDE	1	3	XA←$(PC_{13-8}+DE)_{ROM}$		○		○	
					XA←$(PC_{14-8}+DE)_{ROM}$		○			
		XA,@PCXA	1	3	XA←$(PC_{13-8}+XA)_{ROM}$		○		○	○
					XA←$(PC_{14-8}+XA)_{ROM}$		○			
		XA,@BCDE	1	3	XA←$(B_{2-0}+CDE)_{ROM}$		○			
		XA,@BCXA	1	3	XA←$(B_{2-0}+CXA)_{ROM}$		○			
Bit transfer	MOV1	CY,fmem.bit	2	2	CY←(fmem.bit)		○			
		CY,pmem.@L	2	2	CY←$(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$		○			
		CY,@H+mem.bit	2	2	CY←$(H+mem_{3-0}.bit)$		○			
		fmem.bit, CY	2	2	(fmem.bit)←CY		○			
		pmem.@L,CY	2	2	$(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$←CY		○			
		@H+mem.bit,CY	2	2	$(H+mem_{3-0}.bit)$←CY		○			

Remark ○ denotes that the instruction can be used.

Instruction group	Mnemonic	Operands	No. of bytes	No. of machine cycle	Operation	Skip condition	High-End II	High-End I	Standard	Low-End
Operation	ADDS	A,#n4	1	1+S	A←A+n4	carry	○		○	○
		XA,#n8	2	2+S	XA←XA+n8	carry	○			
		A,@HL	1	1+S	A←A+(HL)	carry	○		○	○
		XA,rp'	2	2+S	XA←XA+rp'	carry	○			
		rp'1, XA	2	2+S	rp'1←rp'1+XA	carry	○			
		A, reg	2	2+S	A←A+reg	carry				
		reg,A	2	2+S	reg←reg+A	carry				
		XA,@HL	2	2+S	XA←XA+(HL)	carry				
		@HL,XA	2	2+S	(HL)←(HL)+XA	carry				
	ADDC	A,@HL	1	1	A,CY←A+(HL)+CY		○		○	○
		XA,rp'	2	2	XA,CY←XA+rp'+CY		○			
		rp'1,XA	2	2	rp'1,CY←rp'1+XA+CY		○			
		A,reg	2	2	A,CY←A+reg+CY					
		reg,A	2	2	reg,CY←reg+A+CY					
		XA,@HL	2	2	XA,CY←XA+(HL)+CY					
		@HL, XA	2	2	(HL),CY←(HL)+XA+CY					
	SUBS	A,@HL	1	1+S	A←A–(HL)	borrow	○		○	
		XA, rp'	2	2+S	XA←XA–rp'	borrow	○			
		rp'1, XA	2	2+S	rp'1←rp'1–XA	borrow	○			
		A,reg	2	2+S	A←A–reg	borrow				
		reg,A	2	2+S	reg←reg–A	borrow				
		XA,@HL	2	2+S	XA←XA–(HL)	borrow				
		@HL, XA	2	2+S	(HL)←(HL)–XA	borrow				
	SUBC	A,@HL	1	1	A,CY←A–(HL)–CY		○		○	
		XA,rp'	2	2	XA,CY←XA–rp'–CY		○			
		rp'1, XA	2	2	rp'1,CY←rp'1–XA–CY		○			
		A,reg	2	2	A,CY←A–reg–CY					
		reg,A	2	2	reg,CY←reg–A–CY					
		XA,@HL	2	2	XA,CY←XA–(HL)–CY					
		@HL,XA	2	2	(HL),CY←(HL)–XA–CY					
	AND	A,#n4	2	2	A←A ∧ n4		○		○	
		A,@HL	1	1	A←A ∧ (HL)		○		○	○
		XA,rp'	2	2	XA←XA ∧ rp'		○			
		rp'1, XA	2	2	rp'1←rp'1 ∧ XA		○			
		mem,A	2	2	mem←mem ∧ A					
		A,reg	2	2	A←A ∧ reg					
		reg,A	2	2	reg←reg ∧ A					
		XA,@HL	2	2	XA←XA ∧ (HL)					
		@HL, XA	2	2	(HL)←(HL) ∧ XA					

Remark ○ denotes that the instruction can be used.

Instruction group	Mnemonic	Operands	No. of bytes	No. of machine cycle	Operation	Skip condition	High-End II	High-End I	Standard	Low-End
Operation	OR	A,#n4	2	2	A←A V n4		○		○	
		A,@HL	1	1	A←A V (HL)		○		○	○
		XA,rp'	2	2	XA←XA V rp'		○			
		rp'1, XA	2	2	rp'1←rp'1 V XA		○			
		mem,A	2	2	mem←mem V A					
		A,reg	2	2	A←A V reg					
		reg,A	2	2	reg←reg V A					
		XA,@HL	2	2	XA←XA V (HL)					
		@HL,XA	2	2	(HL)←(HL) V XA					
	XOR	A,#n4	2	2	A←A ⊻ n4		○		○	
		A,@HL	1	1	A←A ⊻ (HL)		○		○	○
		XA,rp'	2	2	XA←XA ⊻ rp'		○			
		rp'1,XA	2	2	rp'1←rp'1 ⊻ XA		○			
		mem,A	2	2	mem←mem ⊻ A					
		A,reg	2	2	A←A ⊻ reg					
		reg,A	2	2	reg←reg ⊻ A					
		XA,@HL	2	2	XA←XA ⊻ (HL)					
		@HL,XA	2	2	(HL)←(HL) ⊻ XA					
Accumulator manipulate	ROLC	rp	2	2	CY←rp_3, rp_0←CY, rp_{n+1}←rp_n					
		A	1	1	CY←A_3, A_0←CY, A_{n+1}←A_n					
	RORC	rp	2	2	CY←rp_0, rp_3←CY, rp_{n-1}←rp_n					
		A	1	2	CY←A_0, A_3←CY, A_{n-1}←A_n		○		○	○
	NOT	A	2	2	A←$\overline{A}$		○		○	○
Increment and decrement	INCS	reg	1	1+S	reg←reg+1	reg=0	○		○	○
		rp1	1	1+S	rp1←rp1+1	rp1=00H	○			
		@HL	2	2+S	(HL)←(HL)+1	(HL)=0	○		○	
		mem	2	2+S	(mem)←(mem)+1	(mem)=0	○		○	○
		rp'2	2	2+S	rp'2←rp'2+1	XA=0				
	DECS	reg	1	1+S	reg←reg–1	reg=FH	○		○	○
		rp'	2	2+S	rp'←rp'–1	rp=FFH	○			
		mem	2	2+S	mem←mem–1	(mem)=FH				
		@HL	2	2+S	(HL)←(HL)–1	(HL)=FH				
Compare	SKE	reg,#n4	2	2+S	Skip if reg=n4	reg=n4	○		○	○
		@HL,#n4	2	2+S	Skip if (HL)=n4	(HL)=n4	○		○	
		A,@HL	1	1+S	Skip if A=(HL)	A=(HL)	○		○	
		XA,@HL	2	2+S	Skip if XA=(HL)	XA=(HL)	○			
		A,reg	2	2+S	Skip if A=reg	A=reg	○		○	
		XA,rp'	2	2+S	Skip if XA=rp'	XA=rp'	○			
		A,mem	2	2+S	Skip if A=(mem)	A=(mem)				

Remark ○ denotes that the instruction can be used.

Instruction group	Mnemonic	Operands	No. of bytes	No. of machine cycle	Operation	Skip condition	High-End II	High-End I	Standard	Low-End
Carry flag manipulate	SET1	CY	1	1	CY←1		○		○	○
	CLR1	CY	1	1	CY←0		○		○	○
	SKT	CY	1	1+S	Skip if CY=1	CY=1	○		○	○
	NOT1	CY	1	1	CY←$\overline{CY}$		○		○	○
Memory bit manipulate	SET1	mem.bit	2	2	(mem.bit)←1		○		○	○
		fmem.bit	2	2	(fmem.bit)←1		○		○	○
		pmem.@L	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0})←1		○		○	
		@H+mem.bit	2	2	(H+mem_{3-0}.bit)←1		○		○	
	CLR1	mem.bit	2	2	(mem.bit)←0		○		○	○
		fmem.bit	2	2	(fmem.bit)←0		○		○	○
		pmem.@L	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))←0		○		○	
		@H+mem.bit	2	2	(H+mem_{3-0}.bit)←0		○		○	
	SKT	mem.bit	2	2+S	Skip if (mem.bit)=1	(mem.bit)=1	○		○	○
		fmem.bit	2	2+S	Skip if (fmem.bit)=1	(fmem.bit)=1	○		○	○
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))=1	(pmem.@L)=1	○		○	
		@H+mem.bit	2	2+S	Skip if (H+mem_{3-0}.bit)=1	(@H+mem.bit)=1	○		○	
	SKF	mem.bit	2	2+S	Skip if (mem.bit)=0	(mem.bit)=0	○		○	○
		fmem.bit	2	2+S	Skip if (fmem.bit)=0	(fmem.bit)=0	○		○	○
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))=0	(pmem.@L)=0	○		○	
		@H+mem.bit	2	2+S	Skip if (H+mem_{3-0}.bit)=0	(@H+mem.bit)=0	○		○	
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit)=1 and clear	(fmem.bit)=1	○		○	○
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))=1 and clear	(pmem.@L)=1	○		○	
		@H+mem.bit	2	2+S	Skip if (H+mem_{3-0}.bit)=1 and clear	(@H+mem.bit)=1	○		○	
	AND1	CY,fmem.bit	2	2	CY←CY∧ (fmem.bit)		○		○	○
		CY,pmem.@L	2	2	CY←CY∧ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))		○		○	
		CY,@H+mem.bit	2	2	CY←CY∧ (H+mem_{3-0}.bit)		○		○	
		CY,/fmem.bit	2	2	CY←CY∧ ($\overline{fmem.bit}$)					
		CY,/pmem.@L	2	2	CY←CY∧ ($\overline{pmem_{7-2}+L_{3-2}.bit(L_{1-0})}$)					
		CY,/@H+mem.bit	2	2	CY←CY∧ ($\overline{H+mem_{3-0}.bit}$)					
	OR1	CY,fmem.bit	2	2	CY←CY ∨ (fmem.bit)		○		○	○
		CY,pmem.@L	2	2	CY←CY ∨ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))		○		○	
		CY,@H+mem.bit	2	2	CY←CY ∨ (H+mem_{3-0}.bit)		○		○	
		CY,/fmem.bit	2	2	CY←CY ∨ ($\overline{fmem.bit}$)					
		CY,/pmem.@L	2	2	CY←CY ∨ ($\overline{pmem_{7-2}+L_{3-2}.bit(L_{1-0})}$)					
		CY,/@H+mem.bit	2	2	CY←CY ∨ ($\overline{H+mem_{3-0}.bit}$)					
	XOR1	CY,fmem.bit	2	2	CY←CY ∀ (fmem.bit)		○		○	○
		CY,pmem.@L	2	2	CY←CY ∀ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))		○		○	
		CY,@H+mem.bit	2	2	CY←CY ∀ (H+mem_{3-0}.bit)		○		○	
	NOT1	fmem.bit	2	2	(fmem.bit)←($\overline{fmem.bit}$)					
		pmem.@L	2	2	(pmem.bit)←($\overline{pmem.bit}$)					
		@H+mem.bit	2	2	(H+mem_{3-0}.bit)←($\overline{H+mem_{3-0}.bit}$)					

Remark ○ denotes that the instruction can be used.

Instruction group	Mnemonic	Operands	No. of bytes	No. of machine cycle	Operation	Skip condition	High-End II	High-End I	Standard	Low-End
Branch	BR	addr	–	–	PC_{13-0}←addr (optimum instruction is selected among BR !addr, BRCB !caddr, and BR $addr by the assembler)		○		○	○
		addr1	–	–	PC_{14-0}←addr1 (optimum instruction is selected among BRA !addr1, BR !addr, BRCB !caddr, and BR $addr1 by the assembler)		○			
	BRA	!addr1	3	3	PC_{14-0}←addr1		○			
	BR	!addr	3	3	PC_{13-0}←addr		Note		Note	Note
					PC_{14}←0, PC_{13-0}←addr		○			
	BRCB	!caddr	2	2	PC_{13-0}←$PC_{13,12}$+caddr$_{11-0}$		○		○	○
					PC_{14-0}←$PC_{14,13,12}$+caddr$_{11-0}$		○			
	BR	$addr	1	2	PC_{13-0}←addr		○		○	○
		$addr1			PC_{14-0}←addr1		○			
	BR	PCDE	2	3	PC_{13-0}←PC_{13-8}+DE		○			
					PC_{14-0}←PC_{14-8}+DE		○			
		PCXA	2	3	PC_{13-0}←PC_{13-8}+XA		○			
					PC_{14-0}←PC_{14-8}+XA		○			
		BCDE	2	3	PC_{13-0}←BC+DE					
		BCDE	2	3	PC_{14-0}←B_{2-0}+CDE		○			
		BCXA	2	3	PC_{13-0}←BC+XA					
		BCXA	2	3	PC_{14-0}←B_{2-0}+CXA		○			
Subroutine stack control	CALLA	!addr1	3	3	(SP–6)(SP–3)(SP–4)←PC_{11-0} (SP–5)←0, PC_{14}, PC_{13}, PC_{12} (SP–2)←×, ×, MBE, RBE PC_{14-0}←addr, SP←SP–6		○			
	CALL	!addr	3	3	(SP–4)(SP–1)(SP–2)←PC_{11-0} (SP–3)←MBE, RBE, PC_{13}, PC_{12} PC_{13-0}←addr, SP←SP–4		○		○	
				4	(SP–6)(SP–3)(SP–4)←PC_{11-0} (SP–5)←0, PC_{14}, PC_{13}, PC_{12} (SP–2)←×, ×, MBE, RBE PC_{14}←0, PC_{13-0}←addr, SP←SP–6		○			
	CALLF	!faddr	2	2	(SP–4)(SP–1)(SP–2)←PC_{11-0} (SP–3)←MBE, RBE, PC_{13}, PC_{12} PC_{13-0}←000+faddr, SP←SP–4		○		○	○
				3	(SP–6)(SP–3)(SP–4)←PC_{11-0} (SP–5)←0, PC_{14}, PC_{13}, PC_{12} (SP–2)←×, ×, MBE, RBE PC_{14-0}←0000+faddr, SP←SP–6		○			

Note For products having a ROM capacity of 4K or less, this selection is not made by the assembler.

Remark ○ denotes that the instruction can be used.

Instruction group	Mnemonic	Operands	No. of bytes	No. of machine cycle	Operation	Skip condition	High-End II	High-End I	Standard	Low-End
Subroutine stack control	RET		1	3	MBE, RBE, PC_{13}, PC_{12}←(SP+1) PC_{11-0}←(SP)(SP+3)(SP+2) SP←SP+4		○		○	○
					×, ×, MBE, RBE←(SP+4) 0, PC_{14}, PC_{13}, PC_{12}←(SP+1) PC_{11-0}←(SP) (SP+3)(SP+2) SP←SP+6		○			
	RETS		1	3+S	MBE, RBE, PC_{13}, PC_{12}←(SP+1) PC_{11-0}←(SP)(SP+3)(SP+2) SP←SP+4 then skip unconditionally	No condition	○		○	○
					×, ×, MBE, RBE←(SP+4) 0, PC_{14}, PC_{13}, PC_{12}←(SP+1) PC_{11-0}←(SP) (SP+3)(SP+2) SP←SP+6 then skip unconditionally	No condition	○			
	RETI		1	3	MBE, RBE, PC_{13}, PC_{12}, ←(SP+1) PC_{11-0}←(SP)(SP+3)(SP+2) PSW←(SP+4)(SP+5), SP←SP+6		○		○	○
					PC_{11-0}←(SP)(SP+3)(SP+2) ×, PC_{14}, PC_{13}, PC_{12}←(SP+1) PSW←(SP+4)(SP+5), SP←SP+6		○			
	PUSH	rp	1	1	(SP–1)(SP–2)←rp, SP←SP+2		○		○	○
		BS	2	2	(SP–1)←MBS, (SP–2)←RBS, SP←SP–2		○		○	
	POP	rp	1	1	rp←(SP+1)(SP), SP←SP+2		○		○	○
		BS	2	2	MBS←(SP+1), RBS←(SP), SP←SP+2		○		○	
Interrupt control	EI		2	2	IME (IPS.3)←1		○		○	○
		IE×××	2	2	IE×××←1		○		○	○
	DI		2	2	IME (IPS.3)←0		○		○	○
		IE×××	2	2	IE×××←0		○		○	○
Input/output	IN Note	A,PORTn	2	2	A←PORTn (n=0–6)		○		○	○
		XA, PORTn, A	2	2	XA←PORTn+1, PORTn (n=4)		○		○	
	OUT Note	PORTn, A	2	2	PORTn←A (n=2–6)		○		○	○
		PORTn, XA	2	2	PORTn+1, PORTn←XA (n=4)		○		○	
CPU control	HALT		2	2	Set HALT Mode (PCC.2←1)		○		○	○
	STOP		2	2	Set STOP Mode (PCC.3←1)		○		○	○
	NOP		1	1	No Operation		○		○	○

Note When the IN or OUT instruction is executed, MBE=0 or MBE=1, MBS=15 must have been set.

Remark ○ denotes that the instruction can be used.

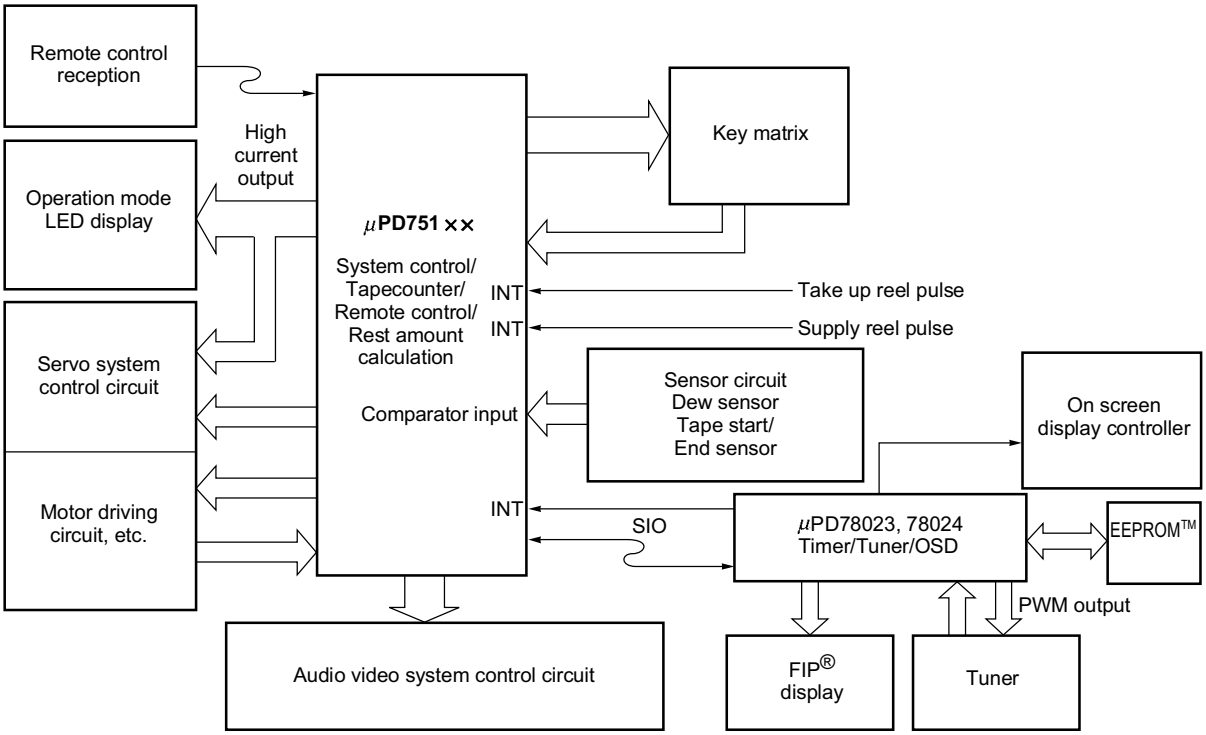
Instruction group	Mnemonic	Operands	No. of bytes	No. of machine cycle	Operation	Skip condition	High-End II	High-End I	Standard	Low-End
Special	SEL	RBn	2	2	RBS←n (n=0–3)		○			
		MBn	2	2	MBS←n (n=0, 1, 15)		○		○	
	GETI[Note]	taddr	1	3	• When TBR instruction is given PC_{13-0}←(taddr)$_{5-0}$+(taddr+1)		○		○	
					• When TCALL instruction is given (SP–4)(SP–1)(SP–2)←PC_{11-0} (SP–3)←MBE, RBE, 0, $PC_{13,12}$ PC_{13-0}←(taddr)$_{5-0}$+(taddr+1) SP←SP–4					
					• When any instruction other than TBR or TCALL is given (taddr)(taddr+1) instruction execution	Dependent on the reference instruction				
			1	3	For TBR instruction PC_{13-0}←(taddr)$_{5-0}$+(taddr+1) PC_{14}←0		○			
				4	For TCALL instruction (SP–5)(SP–6)(SP–3)(SP–4)←×,PC_{14-0} (SP–2)←×, ×, MBE, RBE PC_{13-0}←(taddr)$_{5-0}$+(taddr+1) SP←SP–6, PC_{14}←0					
				3	For any instruction other than TBR or TCALL (taddr)(taddr+1) instruction execution	Dependent on the reference instruction				

Note The TBR and TCALL instructions are assembler pseudo instructions for GETI instruction table definition.

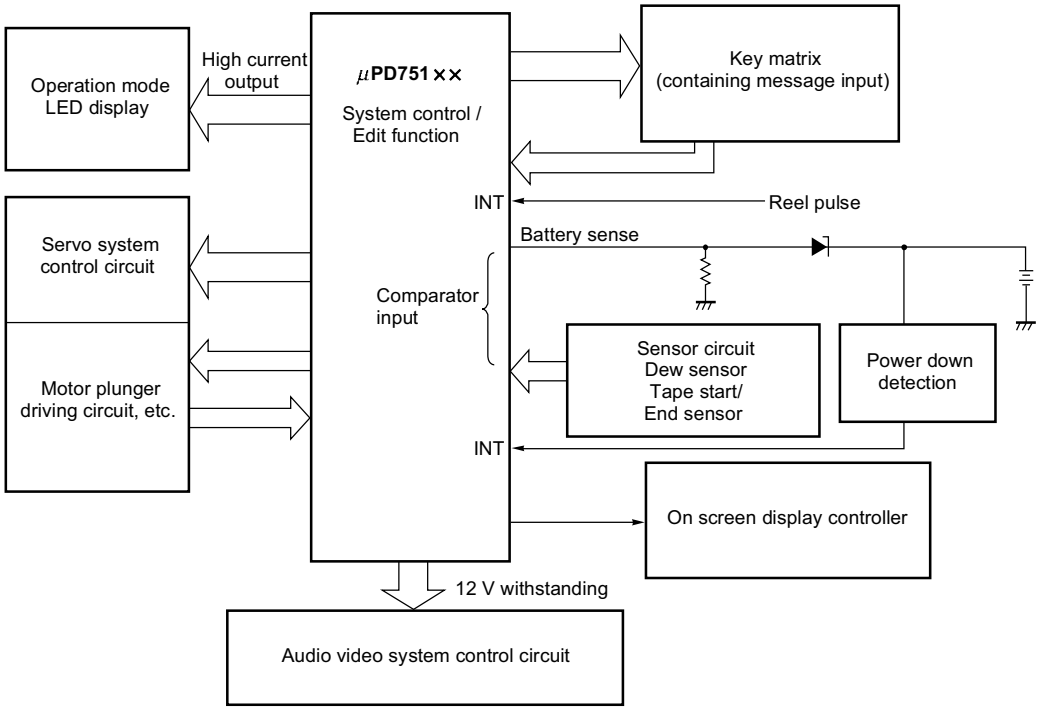
Remark ○ denotes that the instruction can be used.

7. 75X SERIES APPLICATION EXAMPLES

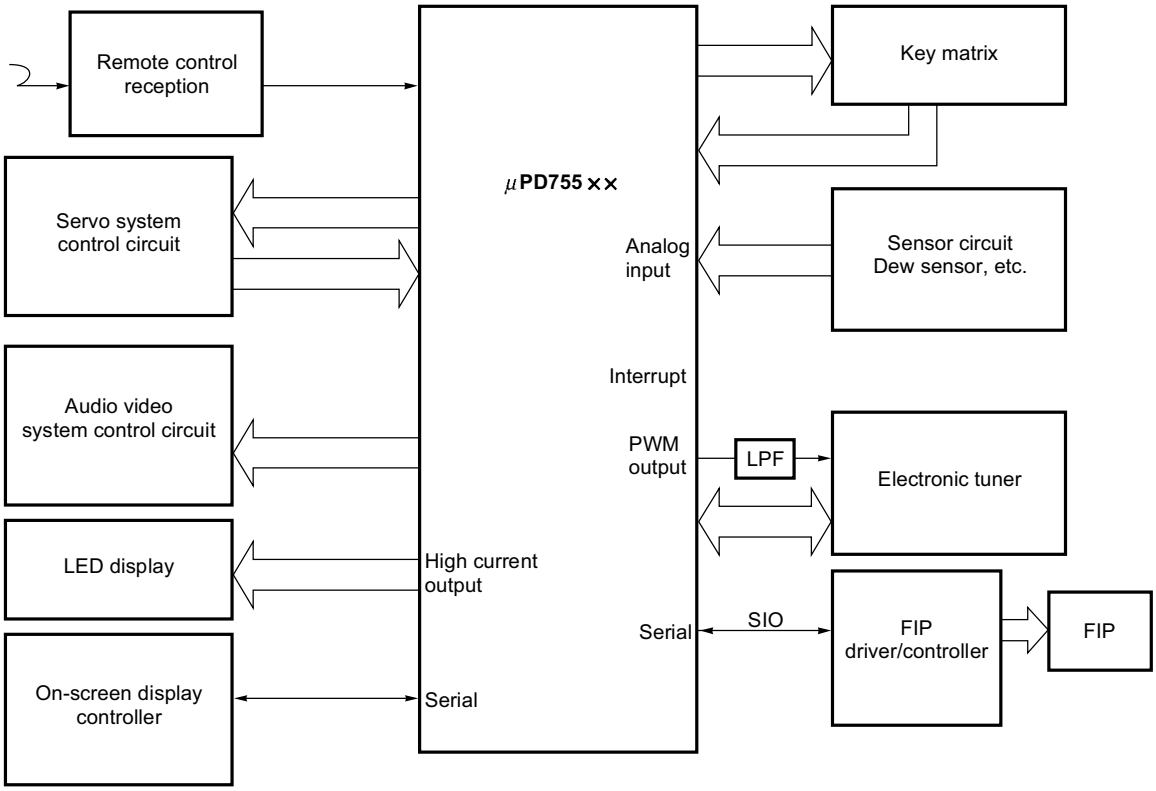
Video cassette recorder system control



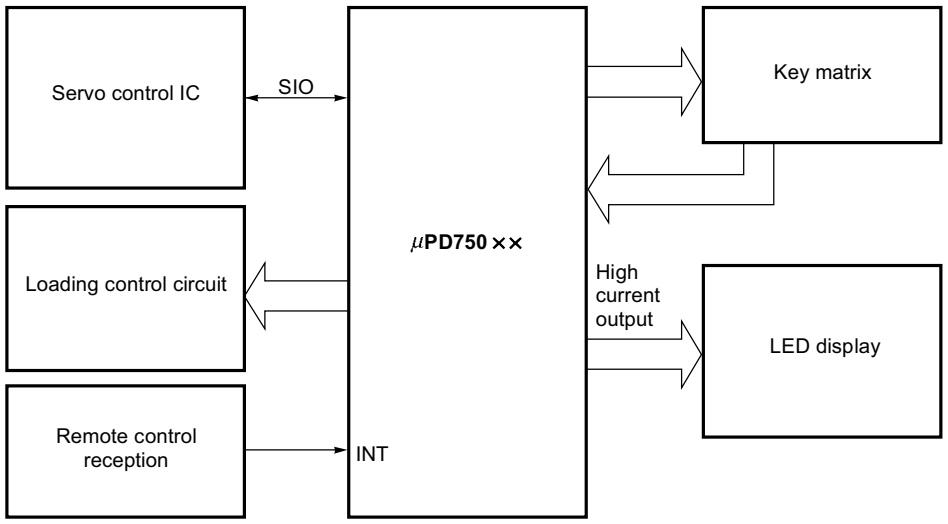
Video camcorder



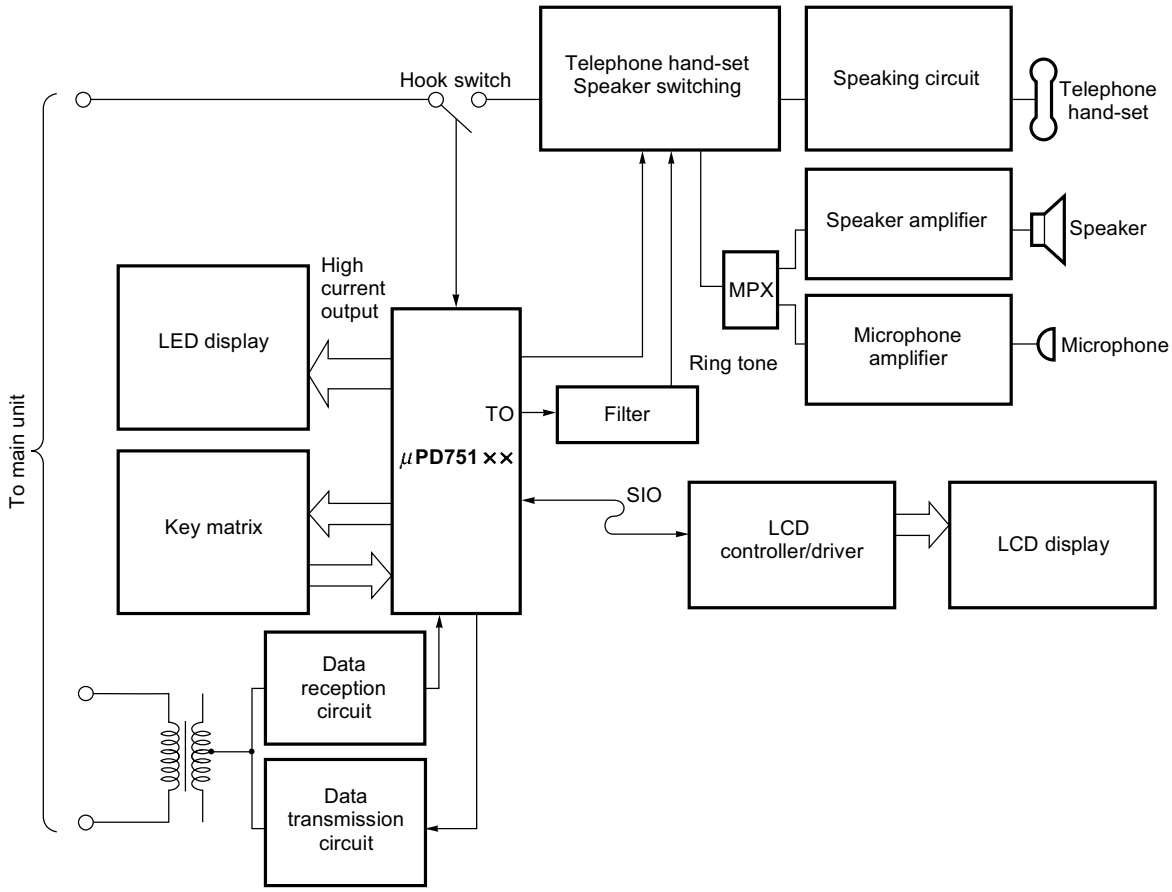
Video cassette recorder



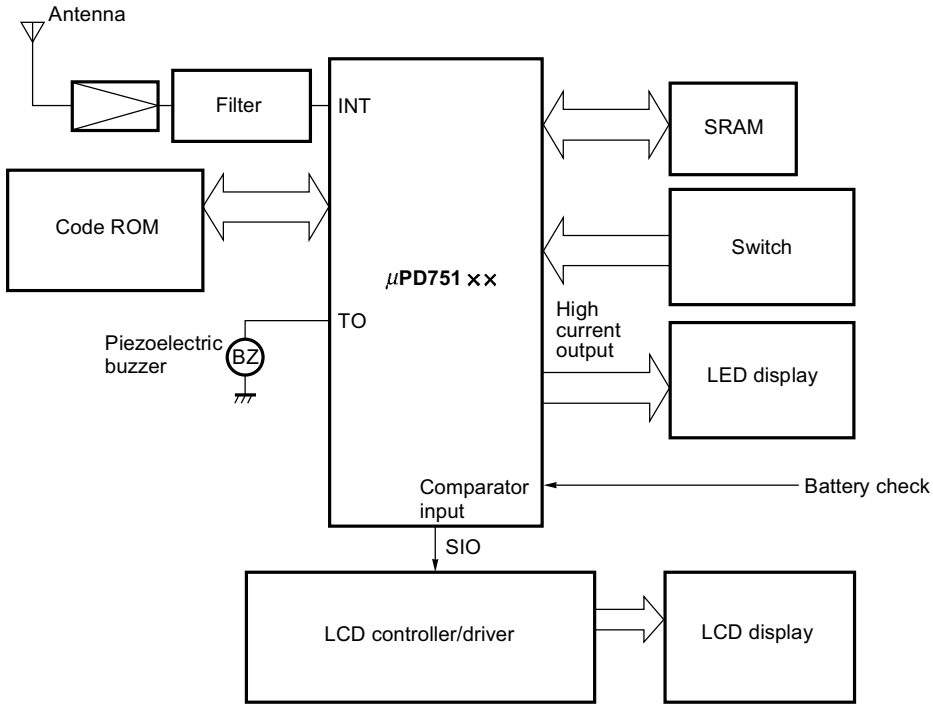
Compact disk player (standard)



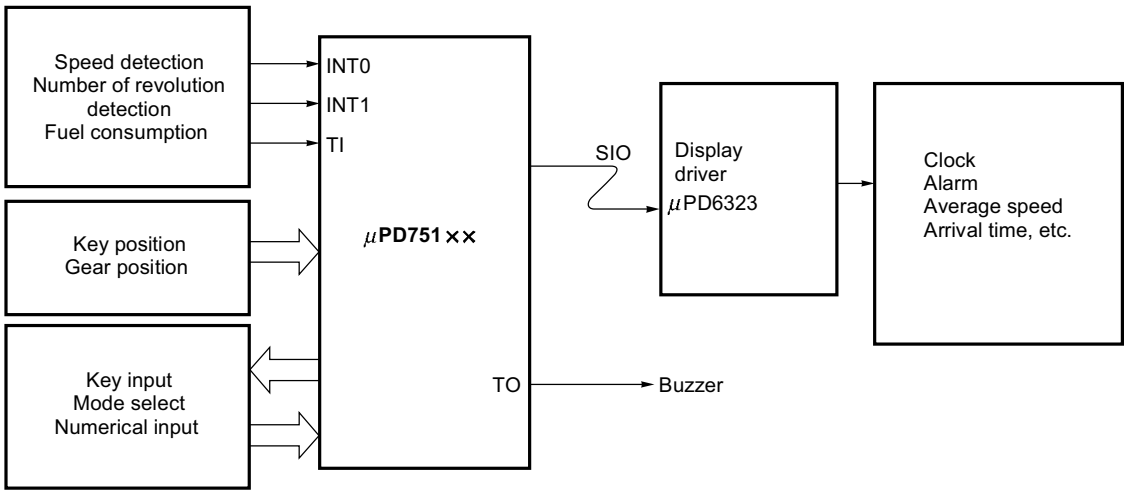
Cellular phone



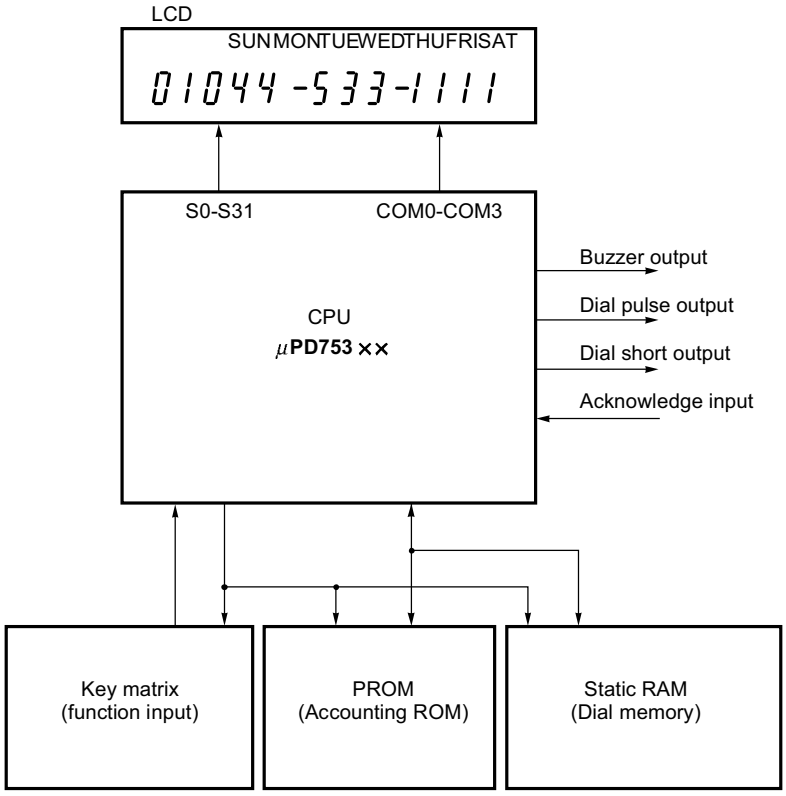
Display pager



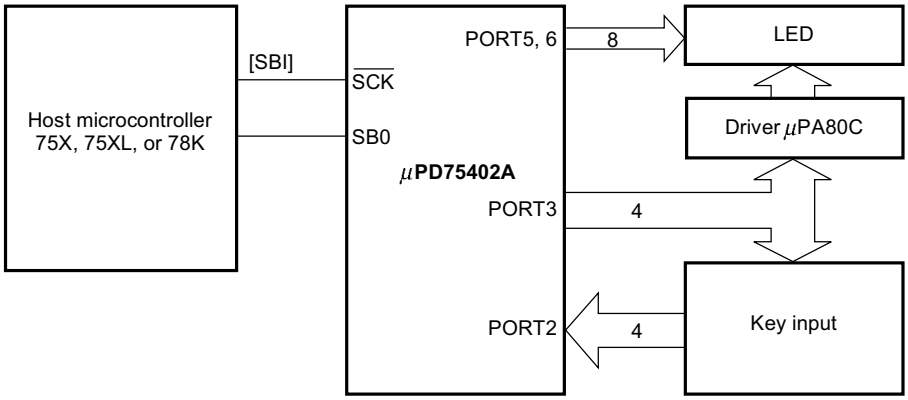
Automobile application (trip computer)



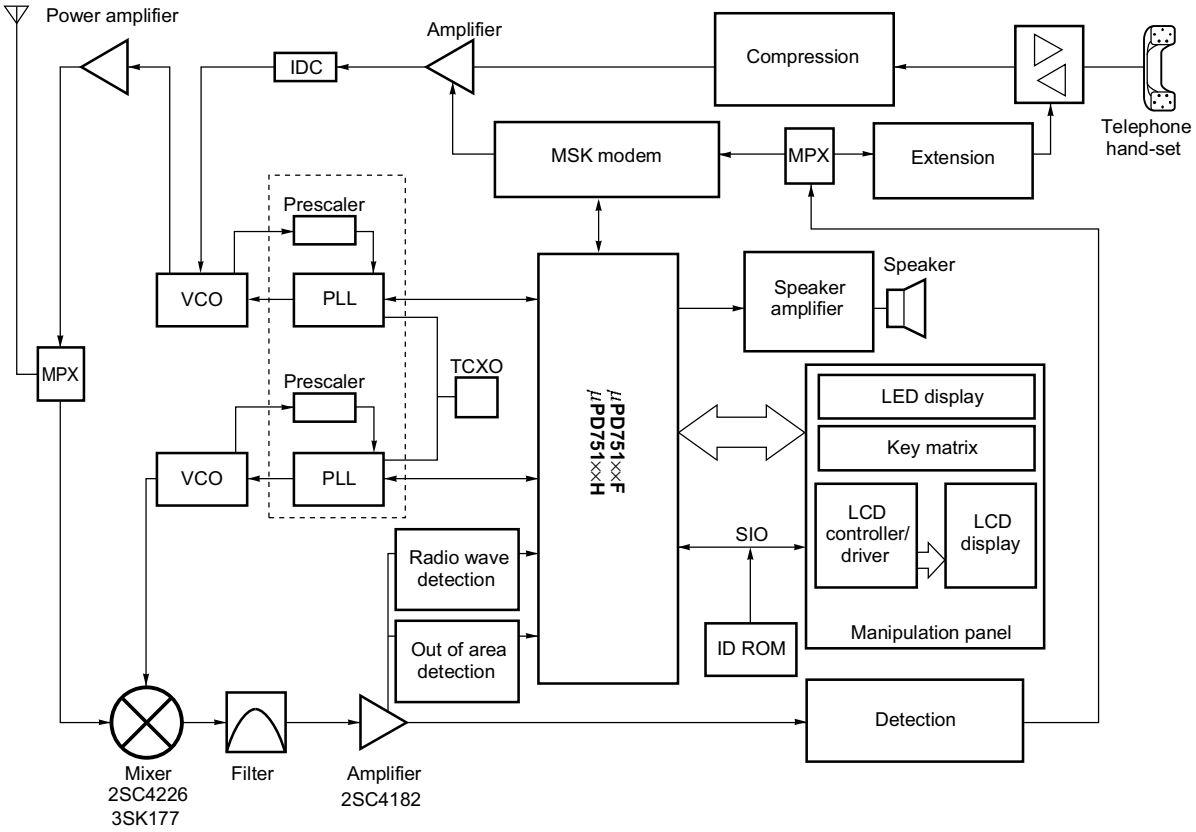
Automatic dialer



Submicrocontroller



Cordless telephone subset



[MEMO]

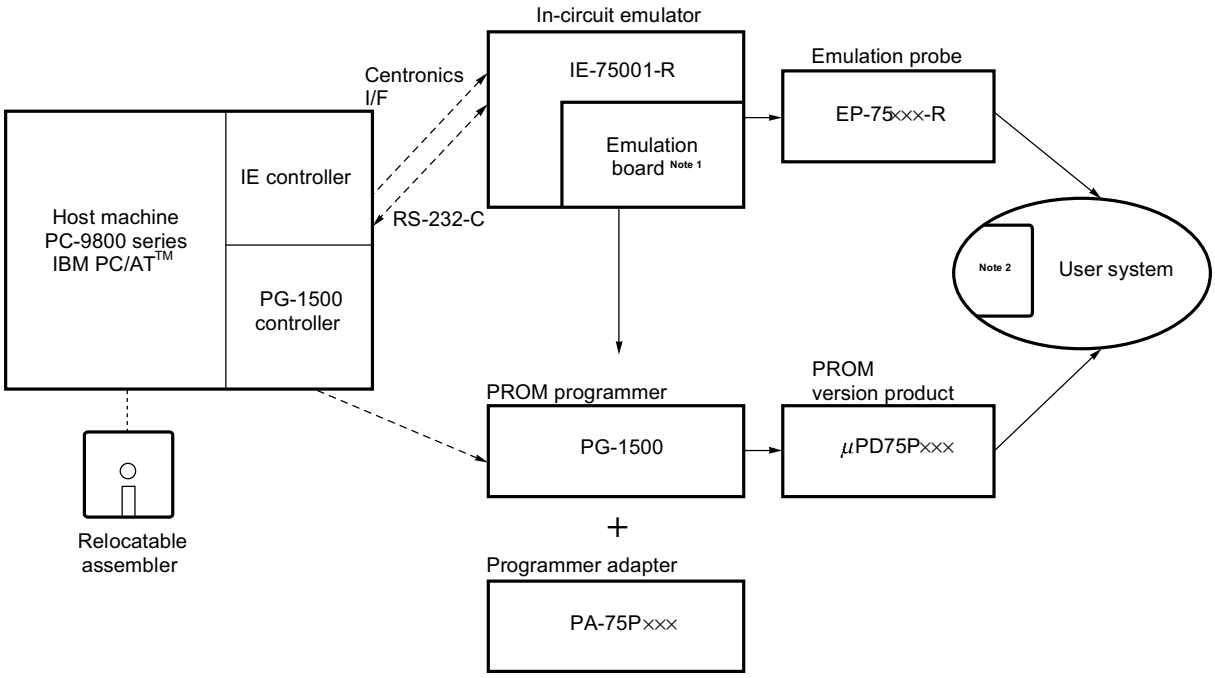
8. 75X SERIES DEVELOPMENT TOOLS

The 75X series provides the following tools for program development:

- Debugging tools
- Language processor
- PROM write tools

Figure 8-1 shows the development tools configuration.

Figure 8-1. Development Tool Configuration



Notes 1. IE-75001-R does not contain an emulation board.
IE-75000-R-EM (option) is necessary.

2. Converter socket (product whose name begins with EV-9200) or adapter (product whose name begins with EV-9500) to connect a QFP emulation probe to a user system.

Remark ×××: Product name which varies depending on the target device or package.

8.1 Debugging Tools

The 75X series provides the following as program debugging tools:

- In-circuit emulators: IE-75001-R

8.1.1 In-circuit emulators

IE-75001-R is provided as in-circuit emulator.

IE-75001-R does not contain an emulation board. To use IE-75001-R, IE-75000-R-EM is required (sold separately).

<table>
<tr><th colspan="2">Debugging tool</th><th colspan="4">Function</th></tr>
<tr><td rowspan="3">Hardware</td><td>IE-75001-R</td><td colspan="4">The IE-75001-R is an in-circuit emulator for debugging the hardware and software to develop the application systems using 75X Series. To develop 75X Series, use the IE-75001-R combined with the optional emulation board Note1 and emulation probe which are sold separately.
The IE-75001-R can be connected to a host machine and PROM programmer for efficient debugging.</td></tr>
<tr><td>IE-75000-R-EM Note1
IF-75300-R-EM Note1</td><td colspan="4">Emulation board for the IE-75001-R to evaluate the applications systems.
Use the emulation combined with the IE-75001-R to evaluate 75X Series.</td></tr>
<tr><td>EP-75×××-R</td><td colspan="4">Emulation probe for 75X Series.
Use the IE-75001-R connected with IE-75000-R-EM or IE-75300-R-EM.</td></tr>
<tr><td rowspan="6">Software</td><td rowspan="6">IE control program</td><td colspan="4">The IE-75001-R and a host machine are connected with RS-232-C and the IE-75001-R is controlled on the host machine.</td></tr>
<tr><td>Host machine</td><td>OS</td><td>Distribution media</td><td>Part number (product name)</td></tr>
<tr><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS™ Ver. 3.30 to Ver. 6.2 Note 2</td><td>3.5-inch 2HD</td><td>μS5A13IE75X</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10IE75X</td></tr>
<tr><td rowspan="2">IBM PC/AT and its compatibles</td><td rowspan="2">See section 8.4</td><td>3.5-inch 2HC</td><td>μS7B13IE75X</td></tr>
<tr><td>5-inch 2HC</td><td>μS7B10IE75X</td></tr>
</table>

Notes 1. For targeted devices, see the section 8.1.2 Development tool list.

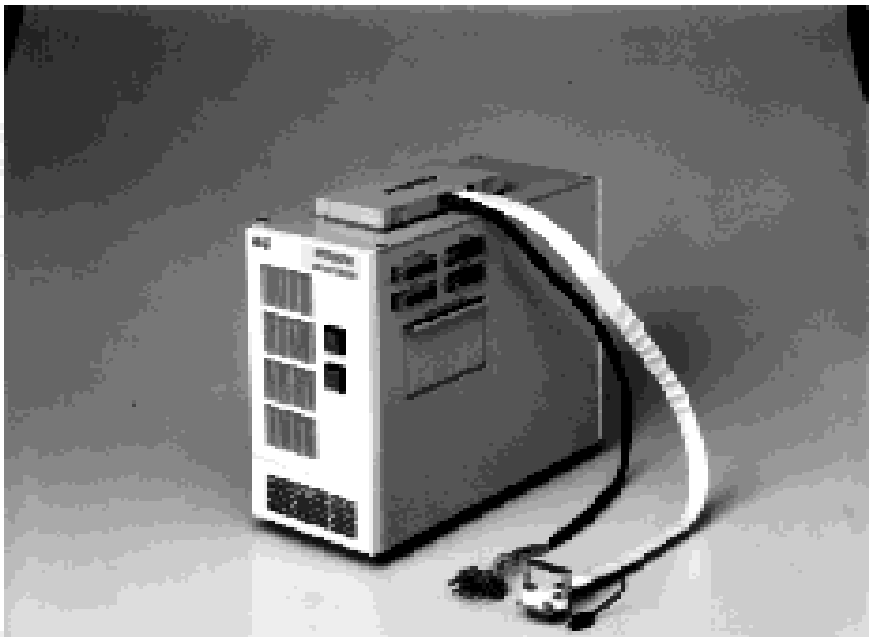
2. Although task swapping function is provided in Ver. 5.00 or later, it cannot be used by this software.

Remarks 1. ×××: Product name which varies depending on the target device or package.

2. IE control program operation is guaranteed only on the host machine under the operating system listed above.

[Features]

- Real time emulation at 6 MHz is enabled.
- Memory capacity
  - Program memory : 64 Kbytes
  - Data memory : 4 Knibbles
- Trace display is enabled during execution.
- Powerful break function
  - Sequential break, parallel break, guard external signal break
- Check trace, qualify trace, section trace
- Coverage function
- High-speed down load function through parallel interface
- Online assembly and disassembly function
- Symbolic debug function
- Data memory and internal register real time output



8.1.2 Development tool list

The development tools of the target devices are listed below.

(1) General purpose series ... μPD750××

Target device	Package	In-circuit emulator	Emulation board	Emulation probe	Conversion socket
μPD75064CU μPD75066CU μPD75068CU μPD75P068CU	42SDIP	IE-75001-R	IE-75000-R-EM	EP-75068CU-R	–
μPD75064GB μPD75066GB μPD75068GB μPD75P068GB	44QFP (10 × 10 mm)			EP-75068GB-R	EV-9200G-44

(2) Control series ... μPD751××

Target device	Package	In-circuit emulator	Emulation board	Emulation probe	Conversion socket
μPD75104CW μPD75106CW μPD75108CW μPD75112CW μPD75116CW μPD75P108BCW/DW μPD75P116CW	64SDIP	IE-75001-R	IE-75000-R-EM	EP-75108CW-R	–
μPD75104GF μPD75106GF μPD75108GF μPD75112GF μPD75116GF μPD75108FGF μPD75112FGF μPD75116FGF μPD75P108BGF μPD75P116GF	64QFP (14 × 20 mm)			EP-75108GF-R	EV-9200G-64
μPD75104AGC μPD75108AGC μPD75116HGC μPD75117HGC μPD75P117HGC	64QFP (14 × 14 mm)			EP-75108AGC-R	EV-9200GC-64
μPD75116HGK μPD75117HGK μPD75P117HGK	64QFP (12 × 12 mm)			EP-75117GK-R	TGK-064SBW[Note]
μPD75P117HKG	64WQFN			–	

Note This conversion socket is a product manufactured by TOKYO ELETECH Corp. Consult your local NEC representative for purchasing.

(3) LCD drive series ... μPD753××

Target device	Package	In-circuit emulator	Emulation board	Emulation probe	Conversion socket
μPD75304GF μPD75306GF μPD75308GF μPD75304BGF μPD75306BGF μPD75308BGF μPD75P308GF μPD75P316GF μPD75P316AGF	80QFP (14 × 20 mm)	IE-75001-R	IE-75000-R-EM IE-75300-R-EM	EP-75308GF-R	EV-9200G-80
μPD75P308K μPD75P316AK	80WQFN			–	
μPD75304BGC μPD75306BGC μPD75308BGC μPD75P316BGC	80QFP (14 × 14 mm)			EP-75308BGC-R	EV-9200GC-80
μPD75304BGK μPD75306BGK μPD75308BGK μPD75316BGK	80TQFP (12 × 12 mm)			EP-75308BGK-R	TGK-080SDW[Note]

(4) Submicrocontroller series ... μPD754××

Target device	Package	In-circuit emulator	Emulation board	Emulation probe	Conversion socket
μPD75402AC μPD75P402C	28DIP	IE-75001-R	IE-75000-R-EM	EP-75402C-R	–
μPD75402ACT μPD75P402CT	28SDIP				
μPD75402AGB μPD75P402GB	44QFP (10 × 10 mm)			EP-75402GB-R	EV-9200G-44

Note This conversion socket is manufactured by TOKYO ELETECH Corp. Consult your local NEC representative for purchasing.

(5) Controller series (with on-chip A/D converter) ... μPD755××

Target device	Package	In-circuit emulator	Emulation board	Emulation probe	Conversion socket
μPD75512GF μPD75516GF μPD75517GF μPD75518GF μPD75P516GF μPD75P518GF	80QFP (14 × 20 mm)	IE-75001-R	IE-75000-R-EM	EP-75516GF-R	EV-9200G-80
μPD75P516K μPD75P518K	80WQFN			–	

8.2 Language Processor

<table>
<tr><th>Debugging tool</th><th colspan="4">Function</th></tr>
<tr><td rowspan="6">RA75X relocatable assembler</td><td colspan="4">It is a relocatable assembler to efficiently develop 75X Series programs.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number
(product name)</td></tr>
<tr></tr>
<tr><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS
(Ver. 3.30 to
Ver. 6.2^{Note})</td><td>3.5-inch 2HD</td><td>μS5A13RA75X</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10RA75X</td></tr>
<tr><td rowspan="2">IBM PC/AT and
its compatibles</td><td rowspan="2">See section 8.4</td><td>3.5-inch 2HC</td><td>μS7B13RA75X</td></tr>
<tr><td>5-inch 2HC</td><td>μS7B10RA75X</td></tr>
</table>

Note Although task swapping function is provided in Ver. 5.00 or later, it cannot be used by this software.

Remark A relocatable assembler operation is only guaranteed on the above host machines.

- **RA75X relocatable assembler**

  The 75X Series provides a relocatable assembler common to the series.

  The relocatable assembler enables the user to divide a program into modules for each function for development and use common programs as a library. The development efficiency is improved drastically. In addition, the structured assembler attached to RA75X enables C-like structured programming.

[Features]

- Branch instruction optimization function
- Useful pseudo instruction
  - Vector table definition pseudo instruction (VENTn pseudo instruction)
  - GETI instruction table definition pseudo instructions (TBR and TCALL pseudo instructions)
- Relocation attribute of CSEG pseudo instruction
- Powerful application utilities (attached to RA75X)
  - Structured assembler (ST75X)
  - Macro processor (MP)
  - Librarian (LB75X)
  - List converter (LCNV75X)

8.3 PROM Write Tools

8.3.1 Types and functions

<table>
<tr><th colspan="2">PROM write tools</th><th colspan="4">Function</th></tr>
<tr><td rowspan="6">Hardware</td><td>PG-1500</td><td colspan="4">PROM programmer which enables you to program single chip microcomputers containing PROM using stand-alone or host machine operation, by connecting the attached board and an option programmer adapter.
It also enables you to program typical PROM devices of 256K bits to 4M bits.</td></tr>
<tr><td>PA-75P×××</td><td colspan="4">PROM programmer adapter used for the 75X series. Connect the programmer adapter to PG-1500 for use.</td></tr>
<tr><td>AF-9703^{Note 1}
AF-9704
AF-9705
AF-9706</td><td colspan="4">PROM programmer mnufactured by Ando Electric Co., Ltd.^{Note 2}</td></tr>
<tr><td>AF-××××</td><td colspan="4">Programmer adapter used for 75X series.
Connect the programmer adapter to AF-9703, AF-9704, AF-9705, and AF-9706 for use.</td></tr>
<tr><td>UNISITE
2900
3900</td><td colspan="4">PROM programmer manufactured by Data I/O Japan Corp.^{Note 3}</td></tr>
<tr><td>PPI-××××,
DIP40/48</td><td colspan="4">Programmer adapter used for 75X Series.
Connect the programmer adapter to UNISITE, 2900, 3900 for use.</td></tr>
<tr><td rowspan="6">Software</td><td rowspan="6">PG-1500 Controller</td><td colspan="4">PG-1500 and a host machine are connected by serial and parallel interfaces and PG-1500 is controlled on the host machine.</td></tr>
<tr><td>Host machine</td><td>OS</td><td>Distribution media</td><td>Part number (product name)</td></tr>
<tr><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS (Ver. 3.30 to Ver. 6.2^{Note 4})</td><td>3.5-inch 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td rowspan="2">IBM PC/AT and its compatibles</td><td rowspan="2">See section 8.4</td><td>3.5-inch 2HC</td><td>μS7B13PG1500</td></tr>
<tr><td>5-inch 2HC</td><td>μS7B10PG1500</td></tr>
</table>

Note 1. Discontinued

2. Ando Electric Co., Ltd.
4-19-7, Kamata
Ota-Ku, Tokyo, 144
Japan

3. Data I/O Japan Corp.
Sumitomo Insurance Higashi-Shinbashi Bld.
2-1-7, Higashi-Shinbashi
Minato-Ku, Tokyo 105
Japan

4. Although task swapping function is provided in Ver. 5.00 or later, it cannot be used by this software.

Remark ×××: Product name which varies depending on the target device or package.

8.3.2 PROM programmer adapter list

Target device	Package	PROM programmer	PROM programmer adapter
μPD75P068CU	42SDIP	PG-1500	PA-75P008CU
μPD75P068GB	44QFP (10 × 10 mm)		
μPD75P108BCW μPD75P108BDW μPD75P116CW	64SDIP		PA-75P108CW
μPD75P108BGF μPD75P116GF	64QFP (14 × 20 mm)		PA-75P116GF
μPD75P117HGC	64QFP (14 × 14 mm)		PA-75P117GC
μPD75P117HGK	64QFP (12 × 12 mm)		PA-75P117GK
μPD75P117HKG	64WQFN		PA-75P117KG
μPD75P308GF μPD75P316GF μPD75P316AGF	80QFP (14 × 20 mm)		PA-75P308GF
μPD75P316BGC	80QFP (14 × 14 mm)		PA-75P316BGC
μPD75P316BGK	80TQFP (12 × 12 mm)		PA-75P316BGK
μPD75P308K μPD75P316AK	80WQFN		PA-75P308K
μPD75P316BKK-T			PA-75P316BKK-T
μPD75P402CT	28SDIP		PA-75P402CT
μPD75P402GB	44QFP (10×10 mm)		PA-75P402GB
μPD75P516GF μPD75P518GF	80QFP (14×20 mm)		PA-75P516GF
μPD75P516K μPD75P518K	80WQFN		PA-75P516K

Program Adapter List (produced by Ando Electric Co., Ltd.)

Target device	Package	PROM programmer	Program adapter
μPD75P068CU	42SDIP	AF-9703[Note]	AF-9783
μPD75P068GB	44QFP (10 × 10 mm)	AF-9704	
μPD75P108BCW μPD75P108BDW μPD75P116CW	64SDIP	AF-9705 AF-9706	AF-9774
μPD75P108BGF μPD75P116GF	64QFP (14 × 20 mm)		AF-9775B
μPD75P117HGC	64QFP (14 × 14 mm)		AF-9775C
μPD75P308GF	80QFP (14 × 20 mm)		AF-9777
μPD75P308K	80WQFN		
μPD75P316BGC	80QFP (14 × 14 mm)		AF-9777B
μPD75P316BGK	80TQFP (12 × 12 mm)		
μPD75P402CT	28SDIP		AF-9788A
μPD75P402GB	44QFP (10 × 10 mm)		AF-9788B
μPD75P516GF μPD75P518GF	80QFP (14 × 20 mm)		AF-9793
μPD75P516K μPD75P518K	80WQFN		

Note Discontinued

Socket Adapter List (produced by Data I/O Japan Corp.)

Target device	Package	PROM programmer	Socket adapter
μPD75P108BCW μPD75P108BDW μPD75P116CW	64SDIP	UNISITE 2900 3900	PPI-0601
μPD75P108BGF μPD75P116GF	64QFP (14 × 20 mm)		PPI-0501
μPD75P238GJ	94QFP (20 × 20 mm)		PPI-0501
μPD75P238KF	94WQFN		PPI-0216
μPD75P308GF	80QFP (14 × 20 mm)		PPI-0502
μPD75P308K μPD75P316AK	80WQFN		PPI-0201
μPD75P402C	28DIP		DIP40/48
μPD75P402CT	28SDIP		PPI-0603
μPD75P402GB	44QFP (10 × 10 mm)		PPI-0505
μPD75P516GF	80QFP (14 × 20 mm)		PPI-0502
μPD75P516K μPD75P518K	80WQFN		PPI-0201

8.4 About IBM PC OS

The following IBM PC OS are supported.

OS	Version
PC DOS™	Ver.5.02 to Ver.6.3 J6.1/V[Note] to J6.3/V[Note]
MS-DOS	Ver.3.30 to Ver.6.22 5.0/V[Note] to 6.2/V[Note]
IBM DOS™	J5.02/V[Note]

Note Supported only in English mode.

Caution Although version 5.0 or later provides the task swap function, it cannot be used with this software.

9. 75X SERIES DOCUMENT LIST

The following tables list current documents as of August 1996.

9.1 Documents for 75X Series Common

Document	Document Number	
	Japanese	English
75X Series Data Book Vol. 1	U10450J	–
75X Series Data Book Vol. 2	U10886J	–
75X Series Development Tool Pamphlet	EF-221	EF-1110
Single-Chip Microcontroller Development Tool Selection Guide	U11069J	U11069E
SBI User's Manual	IEM-5040	–

9.2 Documents for Individual Products

(1) General purpose series (μPD750××)

Part number	Pamphlet	Data sheet	User's manual	Instruction use table	Application note
μPD75064	IF-2018	IC-3140B	IEU-1366	–	IEA-1296
μPD75066					
μPD75068					
μPD75P068		IC-3290			

(2) Control series (μPD751××)

Part number	Pamphlet	Data sheet	User's manual	Instruction use table	Application note
μPD75104	–	IC-2520B	IEM-1260	IEM-902	(I) Basic IEM-1139 (II) Remote control reception IEM-1281 (III) Bar code reader IEM-1265 (IV) IC control for MSK transmission/ reception IEA-1278
μPD75106					
μPD75108					
μPD75112		IC-2549			
μPD75116					
μPD75P116		IC-3358			
μPD75104A	–	IC-2520			
μPD75108A					
μPD75P108B	–	IC-2580			
μPD75108F	–	IC-2810			
μPD75112F					
μPD75116F					
μPD75116H	–	IC-3120	IEU-1340	IEM-5562	
μPD75117H					
μPD75P117H		IP-3130			

(3) LCD driving series (μPD753××)

Part number	Pamphlet	Data sheet	User's manual	Instruction use table	Application note
μPD75304		IC-2523	U-11023E	–	Basic IEA-1239 SBI Application IEA-1245
μPD75306					
μPD75308					
μPD75P308	–	IC-2472			
μPD75P316A	–	IC-2524			
μPD75304B	IF-2016	IC-2913			
μPD75306B					
μPD75308B					
μPD75P316B		IC-3189			

(4) Submicrocontroller series (μPD754××)

Part number	Pamphlet	Data sheet	User's manual	Instruction use table	Application note
μPD75402A	–	IC-2551	IEU-1270	–	IEA-1260
μPD75P402		IC-2650			

(5) Control series (with on-chip A/D converter) (μPD755××)

Part number	Pamphlet	Data sheet	User's manual	Instruction use table	Application note
μPD75512	–	IC-2569	IEU-1252	IEM-5036	Basic IEA-1259 A/D Converter IEA-1236
μPD75516		IC-2471			
μPD75P516		IC-2473			
μPD75517		IC-2672	IEU-1305	IEM-5523	
μPD75518		IC-2706			
μPD75P518		IC-2839			

9.3 Development Tool Relevant Documents (User's Manuals)

9.3.1 Hardware

• 75X Series Common

Document	Document Number	
	Japanese	Engllish
IE-75000-R/IE-75001-R	EEU-846	EEU-1455
IE-75000-R-EM	EEU-673	EEU-1294
PG-1500	EEU-651	EEU-1335

• Individual Products

Document	Document Number	
	Japanese	Engllish
EP-75068CU-R	EEU-873	EEU-1429
EP-75068GB-R	EEU-872	EEU-1428
EP-75108CW-R	EEU-696	EEU-1308
EP-75108GF-R	EEU-695	EEU-1318
EP-75108AGC-R	EEU-694	EEU-1307
EP-75308GF-R	EEU-689	EEU-1301
EP-75308BGC-R	EEU-825	EEU1406
EP-75308BGK-R	EEU-838	EEU-1408
EP-75402C-R	EEU-701	EEU-1319
EP-75402GB-R	EEU-702	EEU-1316
EP-75516GF-R	EEU-703	EEU-1315

9.3.2 Software

Document		Document Number	
		Japanese	English
RA75X assembler package	Operation	EEU-731	EEU-1346
	Language	EEU-730	EEU-1363
PG-1500 controller	PC-9800 Series (MS-DOS) Base	EEU-704	EEU-1291
	IBM PC Series (PC DOS) Base	EEU-5008	U10540E

Remark For explanation of the IE control program, refer to the **IE-75000-R/IE-75001-R User's Manual (EEU-1455)**.

10. PROCEDURE FOR ORDERING MASK ROM

Upon completion of the program development, order mask ROM as required according to the following procedure:

<1> Reserve mask ROM ordering

Contact an authorized NEC distributor or the NEC sales department and inform them about your planned ROM ordering date. Failure to do so may result in processing delays.

<2> Prepare ordering media

The following three media are available for ordering mask ROM:

- UV-EPROM[Note]
- 3.5-inch IBM formatted floppy diskettes
- 5-inch IBM formatted floppy diskettes

Note To order mask ROM using UV-EPROM, prepare three UV-EPROM chips which contain the same data. Enter the mask option data under Mask Option Information.

<3> Complete required documents

To order mask ROM, fill out the following documents:

- Mask ROM Order Slip
- Mask ROM Order Check Sheet
- Mask Option Information

<4> Order

Send the media prepared in <2> together with the documents prepared in <3> to your authorized NEC distributor or the NEC sales department by the set ordering date.

Note For details, refer to the information document “ROM code ordering” (document number: C10302E).

[MEMO]