Vivado

Family – Artix 7
Package – CPG236
Speed Grade – (-1)

Block RAM – 50
DSPs – 90
Flip-Flop – 41,600

Add sources – Add create design – Create file – Verilog – switches

SW0
SW1
SW2
SW3
} IN

LED0
LED1
LED2
LED3
} OUT

Assign LED0 = SW0
...
..
...

Run Synthesis

Add Source – Create simulation source – Switches4_Testbench

Testbench only in simulation

Test bench

```
reg  sw0;
reg  sw1;
 ↓
 ↓
wire LED0;
wire LED1;
 ↓
 ↓
```

(unit under test)

```
Switches4 UUT (sw0, sw1, sw2, sw3, LED0, LED1, LED2, LED3)
```

```
Initial begin
SW0=0;
SW1=0;
↓
↓
#100;
SW0=1;
#100;
SW0=0;
SW1=1;
#100;
SW1=0;
SW2=1;
#100;
SW2=0;
SW3=1;
#100;
SW3=0;
END
```