
STM32
CubeMX

1. Description

1.1. Project

Project Name	NorthSide_0
Board Name	custom
Generated with:	STM32CubeMX 6.14.1
Date	07/14/2025

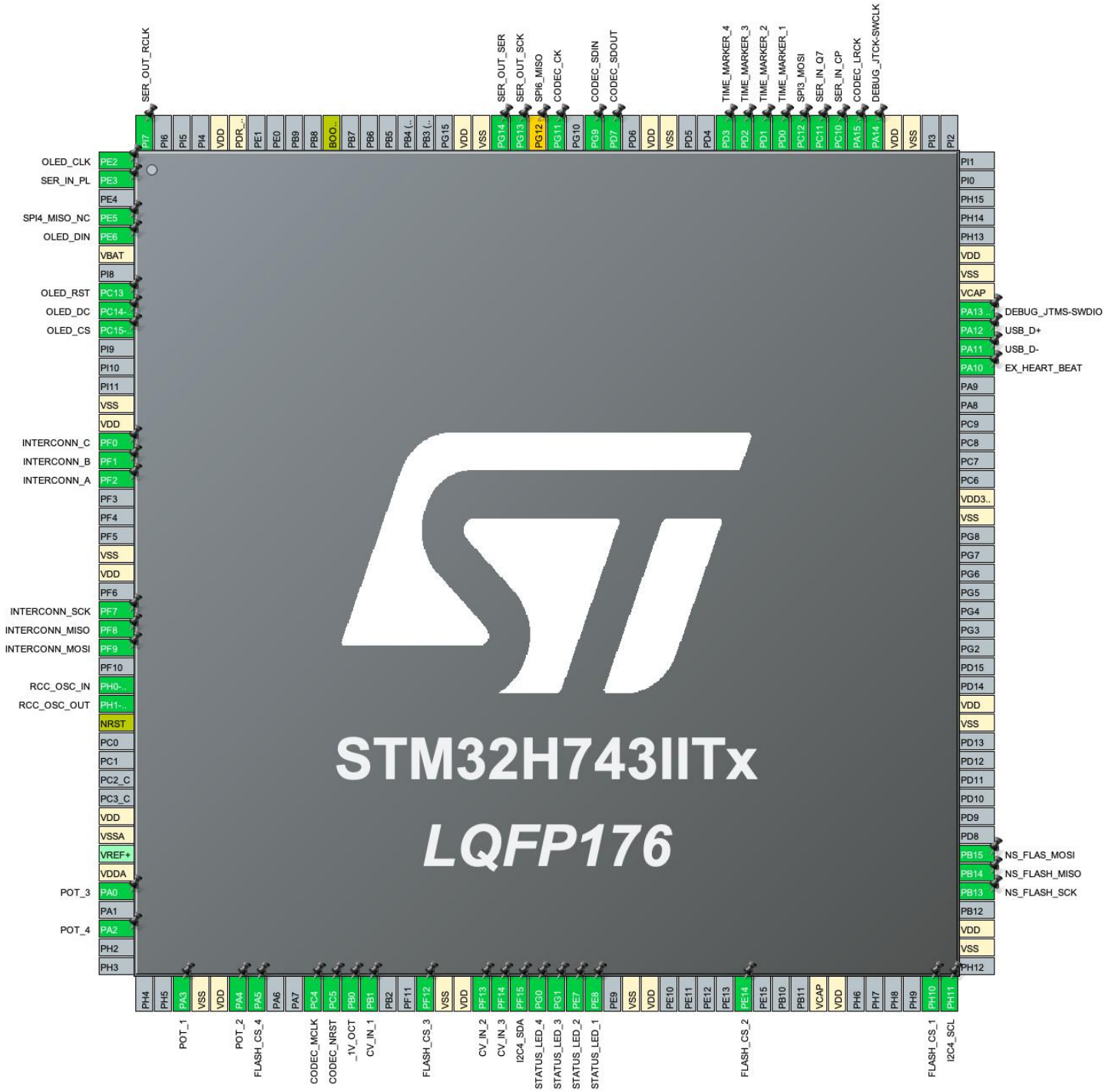
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743IITx
MCU Package	LQFP176
MCU Pin number	176

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	OLED_CLK
2	PE3 *	I/O	GPIO_Output	SER_IN_PL
4	PE5	I/O	SPI4_MISO	SPI4_MISO_NC
5	PE6	I/O	SPI4_MOSI	OLED_DIN
6	VBAT	Power		
8	PC13 *	I/O	GPIO_Output	OLED_RST
9	PC14-OSC32_IN (OSC32_IN) *	I/O	GPIO_Output	OLED_DC
10	PC15-OSC32_OUT (OSC32_OUT) *	I/O	GPIO_Output	OLED_CS
14	VSS	Power		
15	VDD	Power		
16	PF0 *	I/O	GPIO_Output	INTERCONN_C
17	PF1	I/O	GPIO_EXTI1	INTERCONN_B
18	PF2 *	I/O	GPIO_Output	INTERCONN_A
22	VSS	Power		
23	VDD	Power		
25	PF7	I/O	SPI5_SCK	INTERCONN_SCK
26	PF8	I/O	SPI5_MISO	INTERCONN_MISO
27	PF9	I/O	SPI5_MOSI	INTERCONN_MOSI
29	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
30	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
31	NRST	Reset		
36	VDD	Power		
37	VSSA	Power		
39	VDDA	Power		
40	PA0	I/O	ADC1_INP16	POT_3
42	PA2	I/O	ADC1_INP14	POT_4
47	PA3	I/O	ADC1_INP15	POT_1
48	VSS	Power		
49	VDD	Power		
50	PA4	I/O	ADC1_INP18	POT_2
51	PA5 *	I/O	GPIO_Output	FLASH_CS_4
54	PC4	I/O	I2S1_MCK	CODEC_MCLK
55	PC5 *	I/O	GPIO_Output	CODEC_NRST
56	PB0	I/O	ADC2_INP9	_1V_OCT

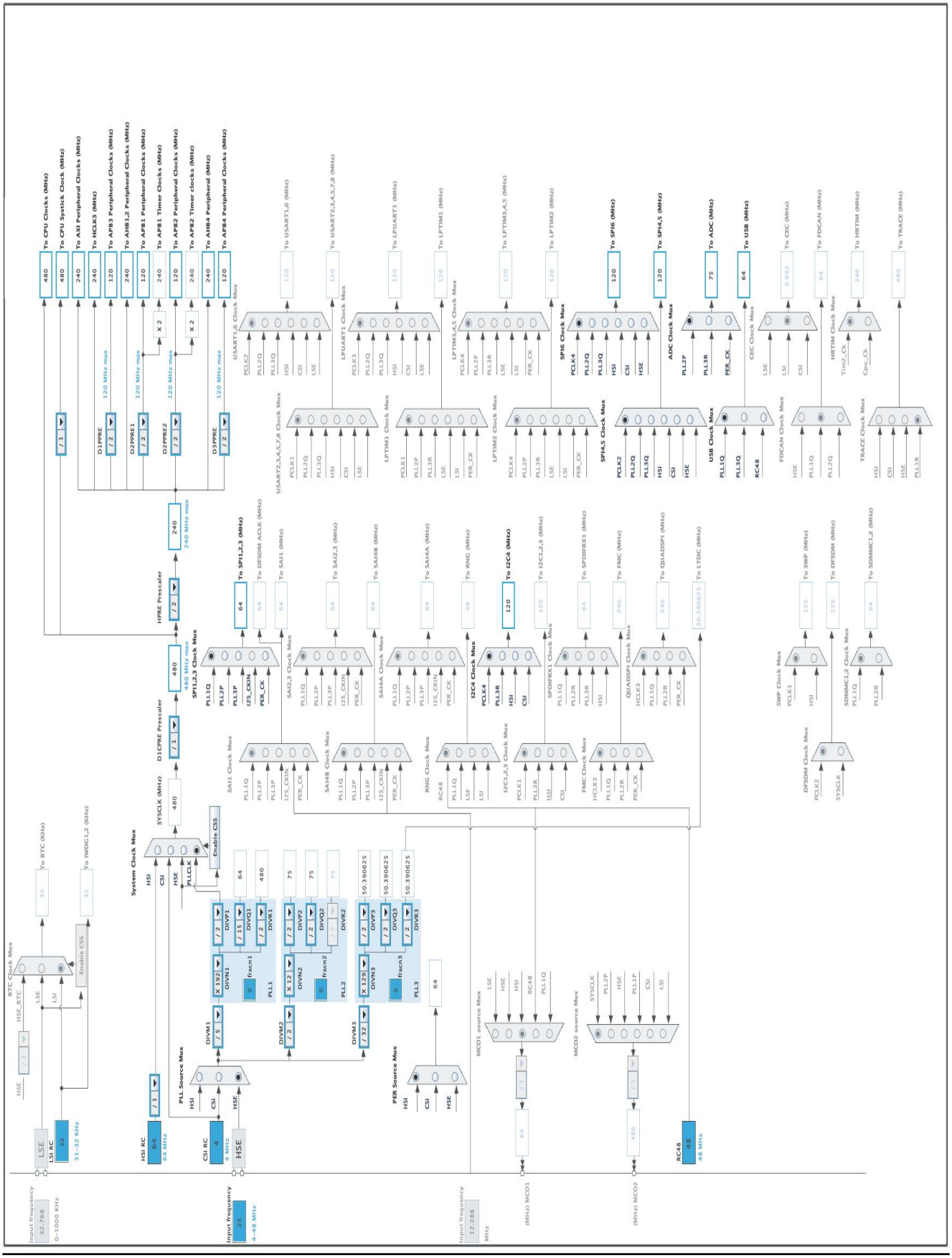
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
57	PB1	I/O	ADC2_INP5	CV_IN_1
60	PF12 *	I/O	GPIO_Output	FLASH_CS_3
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	ADC2_INP2	CV_IN_2
64	PF14	I/O	ADC2_INP6	CV_IN_3
65	PF15	I/O	I2C4_SDA	
66	PG0 *	I/O	GPIO_Output	STATUS_LED_4
67	PG1 *	I/O	GPIO_Output	STATUS_LED_3
68	PE7 *	I/O	GPIO_Output	STATUS_LED_2
69	PE8 *	I/O	GPIO_Output	STATUS_LED_1
71	VSS	Power		
72	VDD	Power		
77	PE14 *	I/O	GPIO_Output	FLASH_CS_2
81	VCAP	Power		
82	VDD	Power		
87	PH10 *	I/O	GPIO_Output	FLASH_CS_1
88	PH11	I/O	I2C4_SCL	
90	VSS	Power		
91	VDD	Power		
93	PB13	I/O	SPI2_SCK	NS_FLASH_SCK
94	PB14	I/O	SPI2_MISO	NS_FLASH_MISO
95	PB15	I/O	SPI2_MOSI	NS_FLAS_MOSI
102	VSS	Power		
103	VDD	Power		
113	VSS	Power		
114	VDD33_USB	Power		
121	PA10 *	I/O	GPIO_Output	EX_HEART_BEAT
122	PA11	I/O	USB_OTG_FS_DM	USB_D-
123	PA12	I/O	USB_OTG_FS_DP	USB_D+
124	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
125	VCAP	Power		
126	VSS	Power		
127	VDD	Power		
135	VSS	Power		
136	VDD	Power		
137	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
138	PA15 (JTDI)	I/O	I2S1_WS	CODEC_LRCK
139	PC10	I/O	SPI3_SCK	SER_IN_CP

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
140	PC11	I/O	SPI3_MISO	SER_IN_Q7
141	PC12	I/O	SPI3_MOSI	
142	PD0 *	I/O	GPIO_Output	TIME_MARKER_1
143	PD1 *	I/O	GPIO_Output	TIME_MARKER_2
144	PD2 *	I/O	GPIO_Output	TIME_MARKER_3
145	PD3 *	I/O	GPIO_Output	TIME_MARKER_4
148	VSS	Power		
149	VDD	Power		
151	PD7	I/O	I2S1_SDO	CODEC_SDOUT
152	PG9	I/O	I2S1_SDI	CODEC_SDIN
154	PG11	I/O	I2S1_CK	CODEC_CK
155	PG12 **	I/O	SPI6_MISO	
156	PG13	I/O	SPI6_SCK	SER_OUT_SCK
157	PG14	I/O	SPI6_MOSI	SER_OUT_SER
158	VSS	Power		
159	VDD	Power		
166	BOOT0	Boot		
171	PDR_ON	Power		
172	VDD	Power		
176	PI7 *	I/O	GPIO_Output	SER_OUT_RCLK

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743IITx
Datasheet	DS12110_Rev8

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

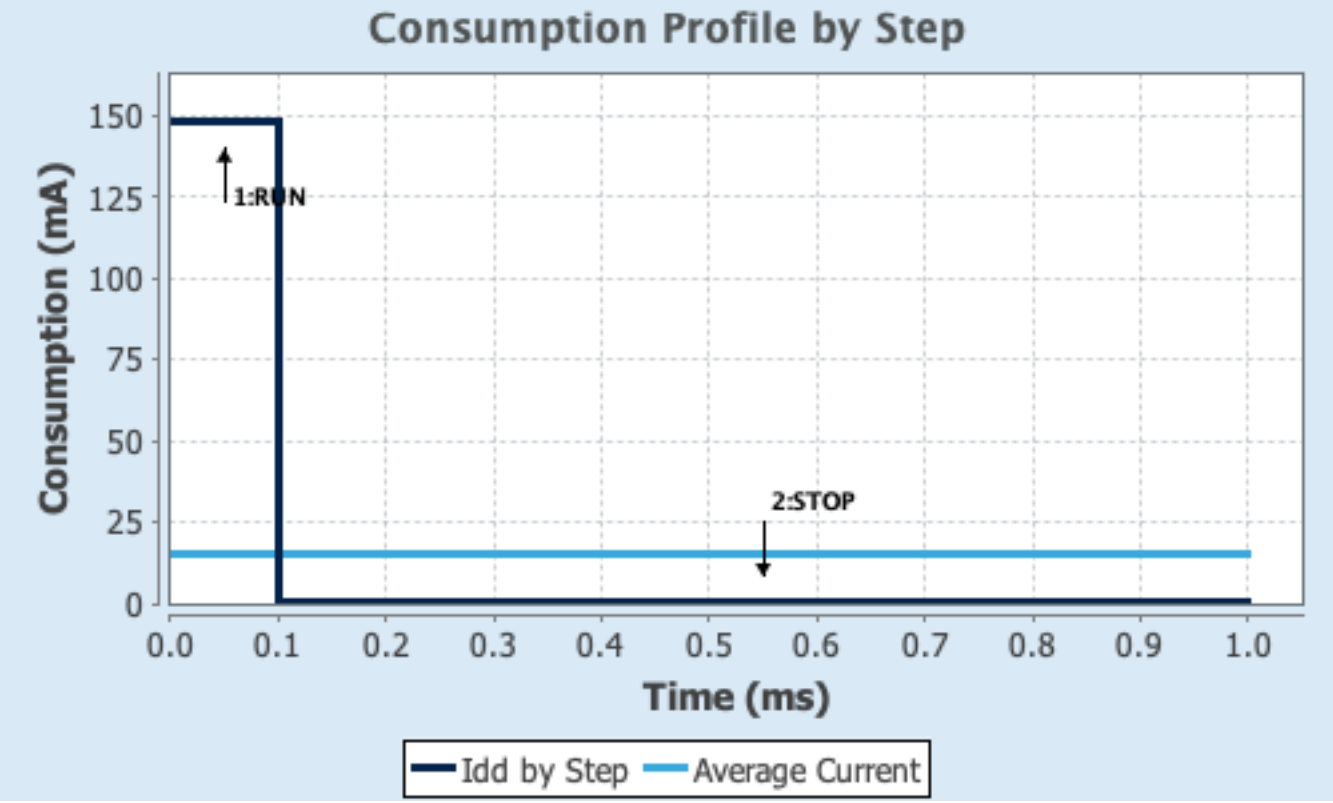
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.91	124.98
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	NorthSide_0.1
Project Folder	/Users/dirktjantele/Desktop/Hardware Projects/Hardware Synth/_Current
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_BDMA_Init	BDMA
5	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
6	MX_SPI2_Init	SPI2
7	MX_SPI3_Init	SPI3
8	MX_SPI4_Init	SPI4
9	MX_SPI5_Init	SPI5
10	MX_SPI6_Init	SPI6
11	MX_ADC1_Init	ADC1

Rank	Function Name	Peripheral Instance Name
12	MX_ADC2_Init	ADC2
13	MX_I2S1_Init	I2S1
14	MX_TIM2_Init	TIM2
15	MX_I2C4_Init	I2C4
16	MX_TIM8_Init	TIM8
17	MX_TIM4_Init	TIM4

3. Peripherals and Middlewares Configuration

3.1. ADC1

mode: IN14

mode: IN15

IN16: IN16 Single-ended

IN18: IN18 Single-ended

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	**4 ***
External Trigger Conversion Source	**Timer 2 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	**Channel 15 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	**Channel 18 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	

	3 *
Channel	**Channel 16 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**4 ***
Channel	Channel 14
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable
ADC_Injected_ConversionMode:	
Enable Injected Conversions	Disable
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	false
Analog Watchdog 2:	
Enable Analog WatchDog2 Mode	false
Analog Watchdog 3:	
Enable Analog WatchDog3 Mode	false

3.2. ADC2

IN2: IN2 Single-ended

IN5: IN5 Single-ended

mode: IN6

mode: IN9

3.2.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	**Asynchronous clock mode divided by 2 ***
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***

Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	**4 ***
External Trigger Conversion Source	**Timer 8 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	**Channel 9 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	**Channel 5 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**3 ***
Channel	Channel 2
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**4 ***
Channel	**Channel 6 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

3.3. CORTEX_M7

3.3.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode	**Enabled ***

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	Enabled
MPU Region Base Address	**0x30000000 ***
MPU Region Size	**256KB ***
MPU SubRegion Disable	**0x87 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	DISABLE
MPU Shareability Permission	ENABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

3.4. DEBUG

Debug: Serial Wire

3.5. I2C4

I2C: I2C

3.5.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	**20 ***
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0xF01075FF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

3.6. I2S1

Mode: Full-Duplex Master

mode: Master Clock Output

3.6.1. Parameter Settings:

Generic Parameters:

Communication Standard	I2S Philips
Data and Frame Format	**24 Bits Data on 32 Bits Frame ***
Selected Audio Frequency	**44 KHz ***
Real Audio Frequency	**41.666 KHz ***
Error between Selected and Real	**-5.3 % ***

Clock Parameters:

Clock Source	PLL I2SR Clock
Clock Polarity	Low

Advanced Parameters:

First Bit	Firstbit Msb
Ws Inversion	Ws Inversion Disable
Data24 Bit Alignment	**Data 24 Bit Alignment Left ***
Master Keep Io State	Master Keep Io State Disable

3.7. MEMORYMAP

mode: Activated

3.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.8.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range

3.9. SPI2

Mode: Full-Duplex Master

3.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.10. SPI3

Mode: Full-Duplex Master

3.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.11. SPI4

Mode: Full-Duplex Master

3.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**128 ***
Baud Rate	**937.5 KBits/s ***
Clock Polarity (CPOL)	Low

Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.12. SPI5

Mode: Full-Duplex Master

3.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**15.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable

Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.13. SPI6

Mode: Transmit Only Master

3.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**256 ***
Baud Rate	**468.75 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.14. SYS

Timebase Source: TIM1

3.15. TIM2

Clock Source : Internal Clock

3.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**24000-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

3.16. TIM4

Clock Source : Internal Clock

3.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120 - 1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 - 1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

3.17. TIM8

Clock Source : Internal Clock

3.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2400-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

3.18. USB_OTG_FS

Mode: Device_Only

3.18.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

3.19. FREERTOS

Interface: CMSIS_V2

3.19.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	**Enabled ***

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16

USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

3.19.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

3.19.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	POT_3
	PA2	ADC1_INP14	Analog mode	No pull-up and no pull-down	n/a	POT_4
	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	POT_1
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	POT_2
ADC2	PB0	ADC2_INP9	Analog mode	No pull-up and no pull-down	n/a	_1V_OCT
	PB1	ADC2_INP5	Analog mode	No pull-up and no pull-down	n/a	CV_IN_1
	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	CV_IN_2
	PF14	ADC2_INP6	Analog mode	No pull-up and no pull-down	n/a	CV_IN_3
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
I2C4	PF15	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PH11	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2S1	PC4	I2S1_MCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODEC_MCLK
	PA15 (JTDI)	I2S1_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODEC_LRCK
	PD7	I2S1_SDO	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODEC_SDOUT
	PG9	I2S1_SDI	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODEC_SDIN
	PG11	I2S1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	CODEC_CK
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	NS_FLASH_SCK
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	NS_FLASH_MISO
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	NS_FLAS_MOSI
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_IN_CP
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_IN_Q7
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	OLED_CLK
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI4_MISO_NC
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	OLED_DIN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	INTERCONN_SCK
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	INTERCONN_MISO
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	INTERCONN_MOSI
SPI6	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_OUT_SCK
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_OUT_SER
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_D-
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_D+
Single Mapped Signals	PG12	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE3	GPIO_Output	Output Push Pull	**Pull-up ***	Low	SER_IN_PL
	PC13	GPIO_Output	**Output Open Drain ***	**Pull-up ***	Low	OLED_RST
	PC14-OSC32_IN (OSC32_IN)	GPIO_Output	**Output Open Drain ***	**Pull-up ***	Low	OLED_DC
	PC15-OSC32_OUT	GPIO_Output	**Output Open Drain ***	**Pull-up ***	Low	OLED_CS
	PF0	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	INTERCONN_C
	PF1	GPIO_EXTI1	**External Interrupt Mode with Rising/Falling edge**	No pull-up and no pull-down	**n/a**	INTERCONN_B
	PF2	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	INTERCONN_A
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	FLASH_CS_4
	PC5	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	CODEC_NRST
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	FLASH_CS_3
	PG0	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	STATUS_LED_4
	PG1	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	STATUS_LED_3
	PE7	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	STATUS_LED_2
	PE8	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	STATUS_LED_1
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	FLASH_CS_2
	PH10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	FLASH_CS_1
	PA10	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	EX_HEART_BEAT
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	TIME_MARKER_1
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	TIME_MARKER_2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	TIME_MARKER_3

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	TIME_MARKER_4
	PI7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SER_OUT_RCLK

4.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI5_RX	DMA1_Stream0	Peripheral To Memory	Low
SPI5_TX	DMA1_Stream1	Memory To Peripheral	Low
ADC1	DMA1_Stream2	Peripheral To Memory	Low
SPI1_RX	DMA1_Stream3	Peripheral To Memory	Low
SPI1_TX	DMA1_Stream4	Memory To Peripheral	Low
ADC2	DMA1_Stream5	Peripheral To Memory	Low

SPI5_RX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI5_TX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SPI1_RX: DMA1_Stream3 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

SPI1_TX: DMA1_Stream4 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

ADC2: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

4.3. BDMA configuration

DMA request	Stream	Direction	Priority
SPI6_TX	BDMA_Channel0	Memory To Peripheral	Low

SPI6_TX: BDMA_Channel0 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

4.4. MDMA configuration

nothing configured in DMA service

4.5. NVIC configuration

4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line1 interrupt	true	5	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream2 global interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream4 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
ADC1 and ADC2 global interrupts	true	5	0
TIM1 update interrupt	true	15	0
TIM4 global interrupt	true	5	0
SPI5 global interrupt	true	5	0
SPI6 global interrupt	true	5	0
BDMA channel0 global interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
SPI3 global interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
I2C4 event interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
I2C4 error interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
USB On The Go FS global interrupt	unused		
HSEM1 global interrupt	unused		

4.5.2. NVIC Code generation

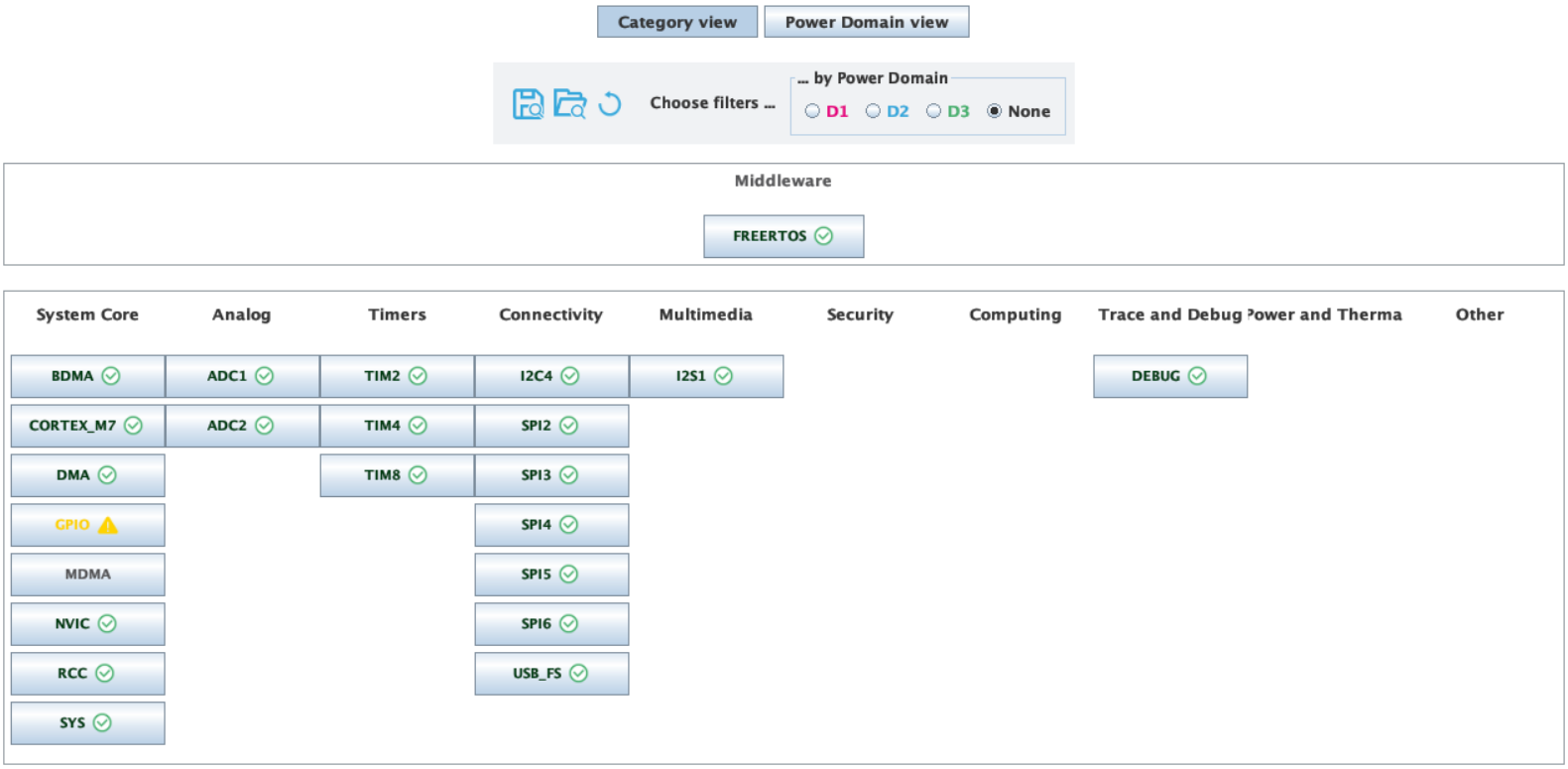
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
EXTI line1 interrupt	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream2 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true
DMA1 stream4 global interrupt	false	true	true
DMA1 stream5 global interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
TIM1 update interrupt	false	true	true
TIM4 global interrupt	false	true	true
SPI5 global interrupt	false	true	true
SPI6 global interrupt	false	true	true
BDMA channel0 global interrupt	false	true	true

*** User modified value**

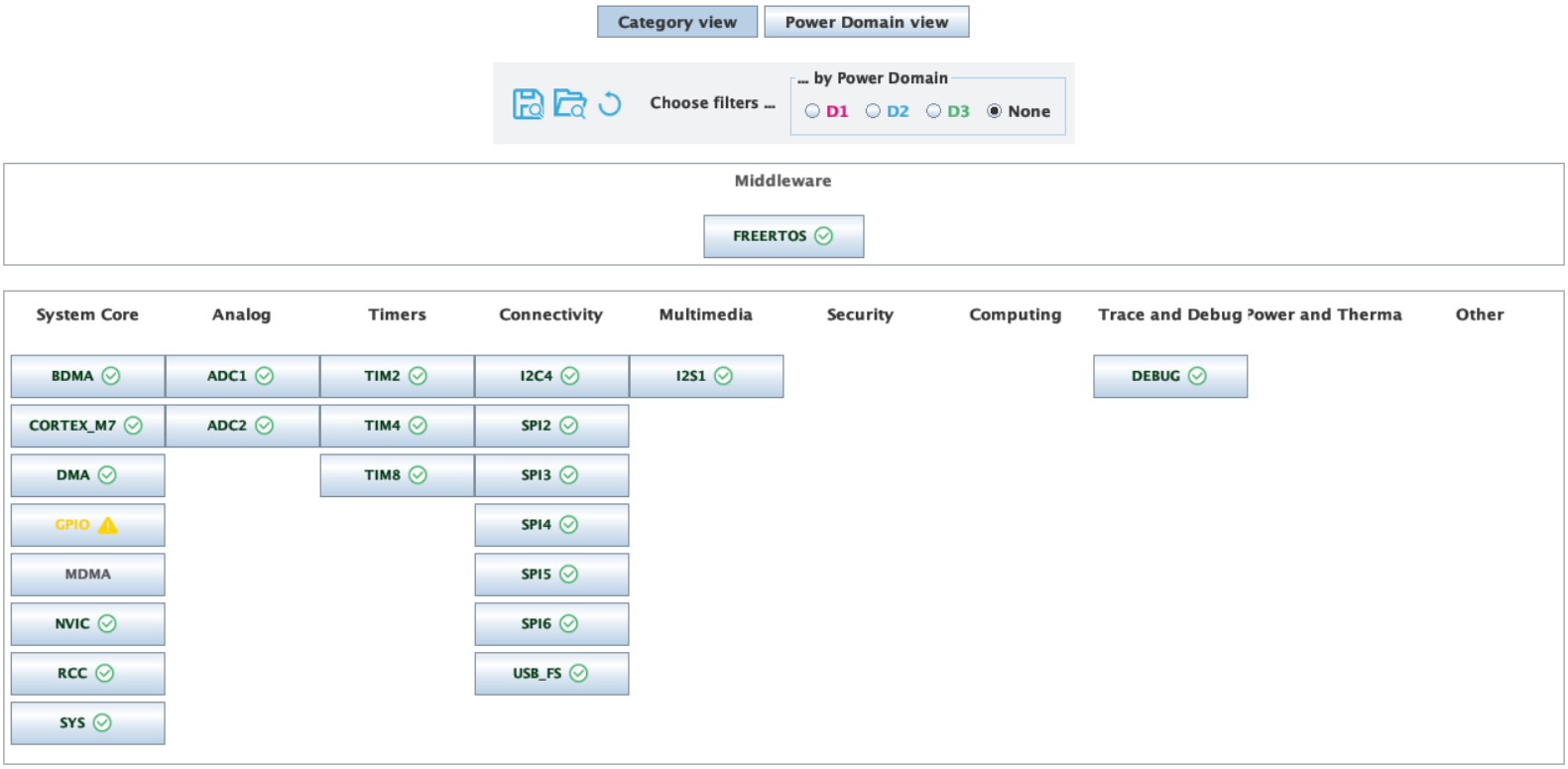
5. System Views

5.1. Category view

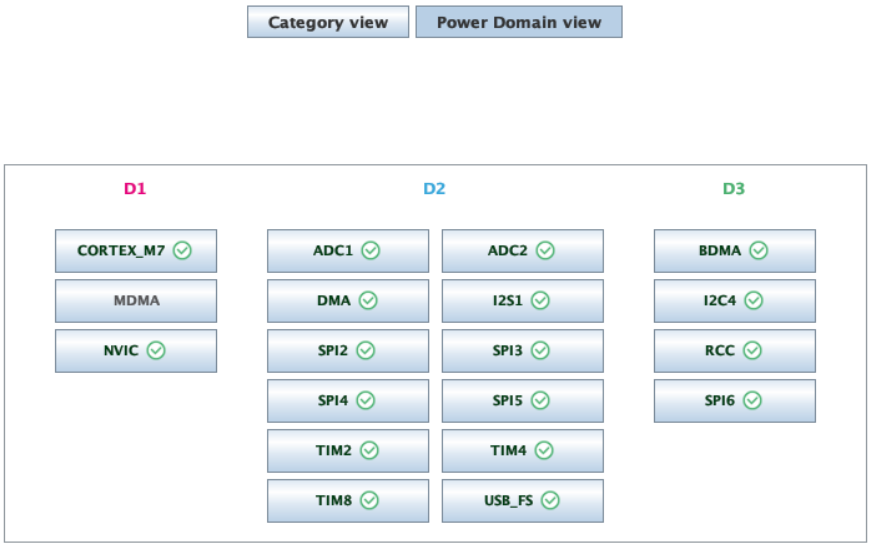
5.1.1. Current



5.1.2. Without filters



5.2. Power Domain view



6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers	https://www.st.com/resource/en/flyer/flpowerstbd.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32h7rs.pdf
Security Bulletin	https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-

	microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4891-stm32h72x-stm32h73x-and-singlecore-stm32h74x75x-system-architecture-and-performance-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4936-migration-of-microcontroller-applications-from-stm32f7-series-to-stm32h743753-line-

	stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5312-migration-from-revy-to-revv-for-stm32h743753-and-stm32h750-value-line-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4760-quadspi-interface-on-stm32-microcontrollers-and-microprocessors--stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4899-stm32-microcontroller-gpio-hardware-settings-and-lowpower-consumption-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5293-migration-guide-from-stm32f7-series-to-stmh74x75x-stm32h72x73x-and-stmh7a37bx-devices-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4991-how-to-wake-up-an-stm32-microcontroller-from-lowpower-mode-with-the-usart-or-the-lpuart-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4838-introduction-to-memory-protection-unit-management-on-stm32-mcus-

	stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5927-i3c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4879-introduction-to-usb-hardware-and-pcb-guidelines-using-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5342--how-to-use-error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4938-getting-started-with-stm32h74xig-and-stm32h75xig-mcu-hardware-development-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5537-how-to-use-adc-oversampling-techniques-to-improve-signaltonoise-ratio-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-guidelines-for-thermal-management-on-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5405-how-to-use-fdcan-bootloader-protocol-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5690-how-to-use-vrefbuf-peripheral-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4230-introduction-to-random-number-generation-validation-using-the-nist-statistical-test-suite-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-guidelines-for-oscillator-design-on-stm8afals-and-stm32-mcusmpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-introduction-to-timers-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4277-how-to-use-

	pwm-shutdown-for-motor-control-and-digital-power-conversion-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4635-how-to-optimize-lpuart-power-consumption-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4759-introduction-to-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4861-introduction-to-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4908-getting-started-with-usart-automatic-baud-rater-detection-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4943-how-to-use-chromart-accelerator-to-refresh-an-lcdtft-display-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5156-introduction-to-security-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5200-getting-started-with-stm32h7-mcus-sdmmc-host-controller-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5224-introduction-to-dmamux-for-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5507-how-to-use-crc-to-check-the-integrity-of-the-internal-flash-memory-on-stm32h7-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5543-guidelines-for-enhanced-spi-communication-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5337-guidelines-for-estimating-stm32h7-mcus-lifetime-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4996-how-to-use-the-jpeg-codec-peripheral-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5348-introduction-to-

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