

# STM32 CubeMX

## 1. Description

### 1.1. Project

Project Name	FH_DeviceBoard
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	12/17/2025

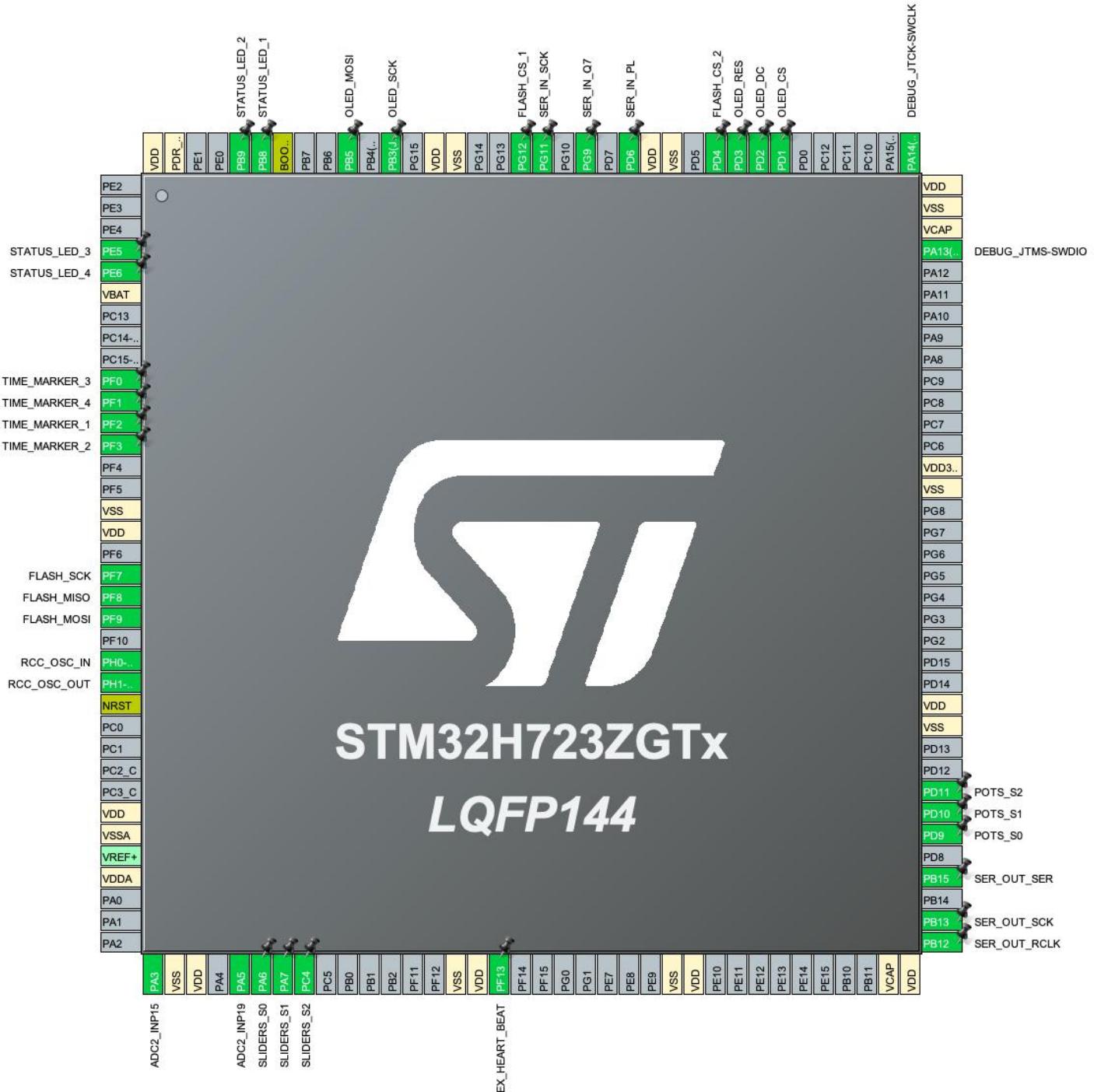
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723ZGTx
MCU Package	LQFP144
MCU Pin number	144

### 1.3. Core(s) information

Core(s)	Arm Cortex-M7
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## **2. Pinout Configuration**



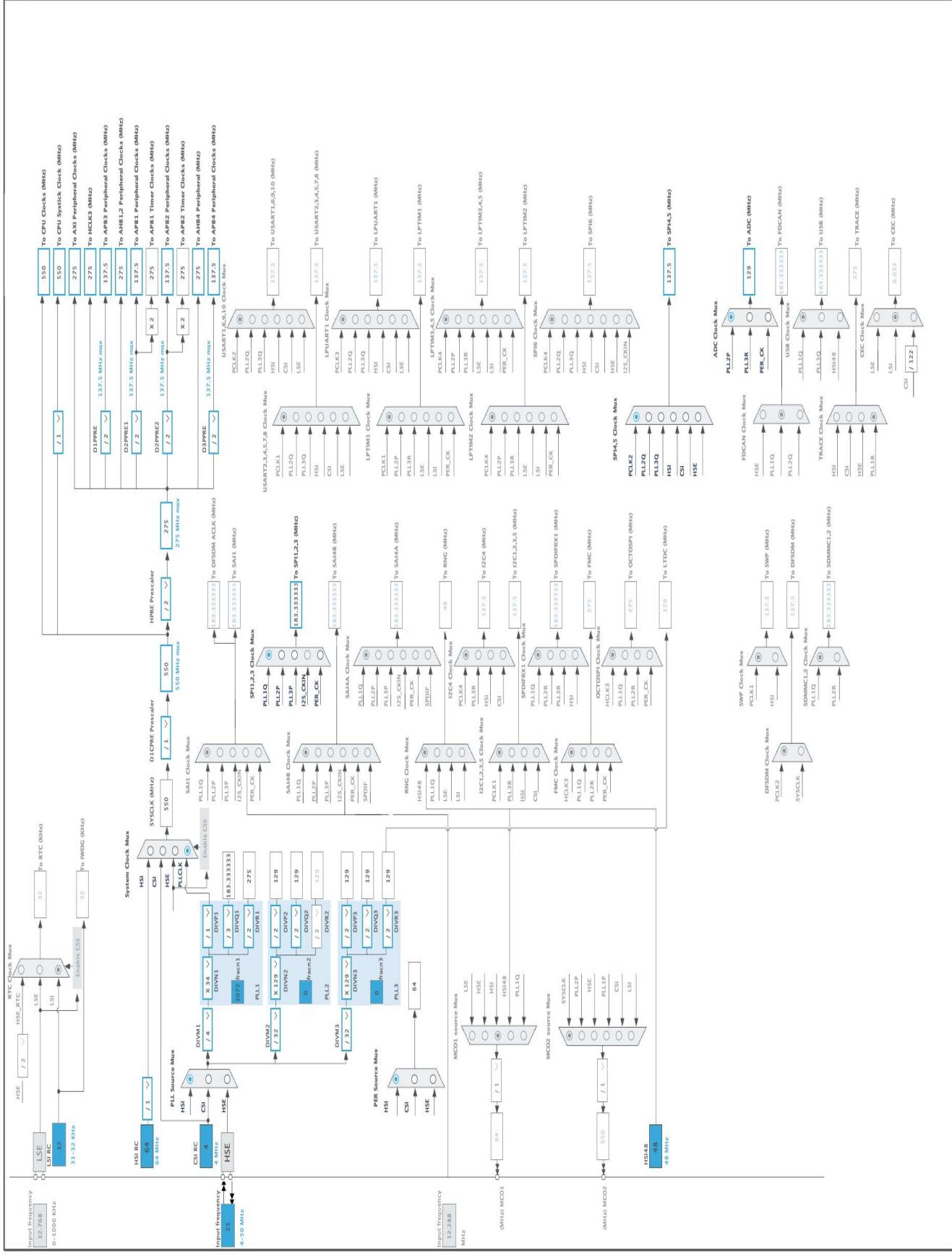
### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4	PE5 *	I/O	GPIO_Output	STATUS_LED_3
5	PE6 *	I/O	GPIO_Output	STATUS_LED_4
6	VBAT	Power		
10	PF0 *	I/O	GPIO_Output	TIME_MARKER_3
11	PF1 *	I/O	GPIO_Output	TIME_MARKER_4
12	PF2 *	I/O	GPIO_Output	TIME_MARKER_1
13	PF3 *	I/O	GPIO_Output	TIME_MARKER_2
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	SPI5_SCK	FLASH_SCK
20	PF8	I/O	SPI5_MISO	FLASH_MISO
21	PF9	I/O	SPI5_MOSI	FLASH_MOSI
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
37	PA3	I/O	ADC2_INP15	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	ADC2_INP19	
42	PA6 *	I/O	GPIO_Output	SLIDERS_S0
43	PA7 *	I/O	GPIO_Output	SLIDERS_S1
44	PC4 *	I/O	GPIO_Output	SLIDERS_S2
51	VSS	Power		
52	VDD	Power		
53	PF13 *	I/O	GPIO_Output	EX_HEART_BEAT
61	VSS	Power		
62	VDD	Power		
71	VCAP	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Output	SER_OUT_RCLK
74	PB13	I/O	SPI2_SCK	SER_OUT_SCK
76	PB15	I/O	SPI2_MOSI	SER_OUT_SER
78	PD9 *	I/O	GPIO_Output	POTS_S0

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
79	PD10 *	I/O	GPIO_Output	POTS_S1
80	PD11 *	I/O	GPIO_Output	POTS_S2
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD33USB	Power		
105	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
115	PD1 *	I/O	GPIO_Output	OLED_CS
116	PD2 *	I/O	GPIO_Output	OLED_DC
117	PD3 *	I/O	GPIO_Output	OLED_RES
118	PD4 *	I/O	GPIO_Output	FLASH_CS_2
120	VSS	Power		
121	VDD	Power		
122	PD6 *	I/O	GPIO_Output	SER_IN_PL
124	PG9	I/O	SPI1_MISO	SER_IN_Q7
126	PG11	I/O	SPI1_SCK	SER_IN_SCK
127	PG12 *	I/O	GPIO_Output	FLASH_CS_1
130	VSS	Power		
131	VDD	Power		
133	PB3(JTDO/TRACESWO)	I/O	SPI3_SCK	OLED_SCK
135	PB5	I/O	SPI3_MOSI	OLED_MOSI
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	STATUS_LED_1
140	PB9 *	I/O	GPIO_Output	STATUS_LED_2
143	PDR_ON	Power		
144	VDD	Power		

\* The pin is affected with an I/O function

## **4. Clock Tree Configuration**



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
MCU	STM32H723ZGTx
Datasheet	DS13313_Rev1

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

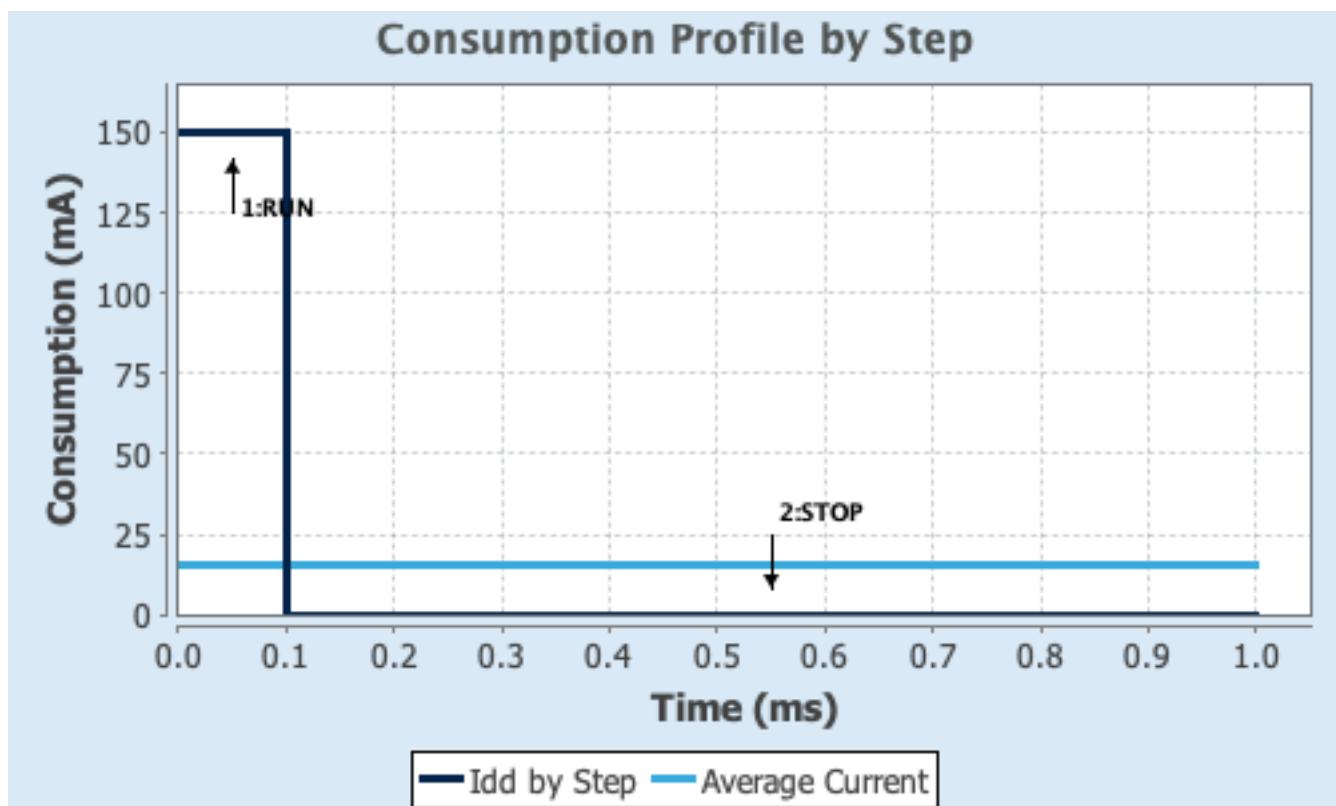
## 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0/Boost	SVOS5: System-Scale5
<b>D1 Mode</b>	DRUN	DSTANDBY
<b>D2 Mode</b>	DRUN	DSTANDBY
<b>D3 Mode</b>	DRUN	DSTOP
<b>Fetch Type</b>	SRAM1/FlashMode-ON/Cache	NA
<b>CPU Frequency</b>	550 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	ALL CLOCKS OFF
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	150 mA	94.5 µA
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	1177.0	0.0
<b>Ta Max</b>	105.2	124.99
<b>Category</b>	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	15.09 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

## 1.6. Chart



## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	FH_DeviceBoard
Project Folder	/Users/dirkjantele/Desktop/Hardware Projects/Hardware Synth/_Current
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_SPI2_Init	SPI2
5	MX_SPI3_Init	SPI3
6	MX_SPI5_Init	SPI5
7	MX_TIM4_Init	TIM4
8	MX_SPI1_Init	SPI1
9	MX_ADC2_Init	ADC2
10	MX_TIM2_Init	TIM2
11	MX_TIM6_Init	TIM6

FH\_DeviceBoard Project  
Configuration Report

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### 3. Peripherals and Middlewares Configuration

#### 3.1. ADC2

**mode:** IN15

**mode:** IN19

##### 3.1.1. Parameter Settings:

###### **ADCs\_Common\_Settings:**

Mode	Independent mode
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###### **ADC\_Settings:**

Clock Prescaler	<b>Asynchronous clock mode divided by 8 *</b>
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	<b>End of sequence of conversion *</b>
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

###### **ADC-Regular\_ConversionMode:**

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	<b>2 *</b>
External Trigger Conversion Source	<b>Timer 2 Capture Compare 2 event *</b>
External Trigger Conversion Edge	Trigger detection on the rising edge
<u>Rank</u>	1
Channel	Channel 15
Sampling Time	<b>32.5 Cycles *</b>
Offset Number	No offset
Offset Signed Saturation	Disable
<u>Rank</u>	<b>2 *</b>
Channel	<b>Channel 19 *</b>
Sampling Time	<b>32.5 Cycles *</b>
Offset Number	No offset
Offset Signed Saturation	Disable

###### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions	Disable
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###### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:**

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:**

Enable Analog WatchDog3 Mode false

## 3.2. CORTEX\_M7

### 3.2.1. Parameter Settings:

**Speculation default mode Settings:**

Speculation default mode **Enabled \***

**Cortex Interface Settings:**

CPU ICache Disabled

CPU DCache Disabled

**Cortex Memory Protection Unit Control Settings:**

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault,  
NMI and FAULTMASK handlers

**Cortex Memory Protection Unit Region 0 Settings:**

MPU Region Enabled

MPU Region Base Address **0x0 \***

MPU Region Size 4GB

MPU SubRegion Disable **0x87 \***

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE

MPU Shareability Permission ENABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

**Cortex Memory Protection Unit Region 1 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 2 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 3 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 4 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 5 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 6 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 7 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 8 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 9 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 10 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 11 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 12 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 13 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 14 Settings:**

MPU Region                          Disabled

**Cortex Memory Protection Unit Region 15 Settings:**

MPU Region                          Disabled

### 3.3. DEBUG

**Debug: Serial Wire**

### 3.4. MEMORYMAP

**mode: Activated**

### 3.5. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

3.5.1. Parameter Settings:

**Power Parameters:**

SupplySource                        PWR\_LDO\_SUPPLY

Power Regulator Voltage Scale    Power Regulator Voltage Scale 0

**RCC Parameters:**

TIM Prescaler Selection            Disabled

HSE Startup Timeout Value (ms)   100

LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

**System Parameters:**

VDD voltage (V)	3.3
Flash Latency(WS)	3 WS (4 CPU cycle)

**PLL range Parameters:**

PLL1 input frequency range	Between 8 and 16 MHz
PLL2 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

### 3.6. SPI1

#### Mode: Receive Only Master

##### 3.6.1. Parameter Settings:

**Basic Parameters:**

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	<b>8 *</b>
Baud Rate	<b>22.916666 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.7. SPI2

#### Mode: Transmit Only Master

##### 3.7.1. Parameter Settings:

###### **Basic Parameters:**

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

###### **Clock Parameters:**

Prescaler (for Baud Rate)	<b>256 *</b>
Baud Rate	<b>716.145 KBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

###### **Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.8. SPI3

#### Mode: Transmit Only Master

##### 3.8.1. Parameter Settings:

###### **Basic Parameters:**

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

###### **Clock Parameters:**

Prescaler (for Baud Rate)	<b>16 *</b>
Baud Rate	<b>11.458333 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.9. SPI5

#### Mode: Full-Duplex Master

##### 3.9.1. Parameter Settings:

**Basic Parameters:**

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	<b>8 *</b>
Baud Rate	<b>17.1875 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low

Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.10. SYS

#### Timebase Source: TIM1

### 3.11. TIM2

#### Clock Source : Internal Clock

##### 3.11.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>240 - 1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	<b>1000 - 1 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

### 3.12. TIM4

#### Clock Source : Internal Clock

##### 3.12.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>120 - 1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>1000 - 1 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

### 3.13. TIM6

#### mode: Activated

##### 3.13.1. Parameter Settings:

###### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>120 - 1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
auto-reload preload	Disable

###### **Trigger Output (TRGO) Parameters:**

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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### 3.14. FREERTOS

#### Interface: CMSIS\_V2

##### 3.14.1. Config parameters:

###### **API:**

FreeRTOS API	CMSIS v2
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###### **Versions:**

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

###### **MPU/FPU:**

ENABLE_MPU	Disabled
ENABLE_FPU	<b>Enabled *</b>

###### **Kernel settings:**

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled

QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

**Memory management settings:**

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

**Hook function related definitions:**

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

**Run time and task stats gathering related definitions:**

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

**Co-routine related definitions:**

USE_CO_Routines	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

**Software timer definitions:**

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

**Interrupt nesting behaviour configuration:**

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

**Added with 10.2.1 support:**

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

**CMSIS-RTOS V2 flags:**

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled

USE\_OS2\_MUTEX                          Enabled

### 3.14.2. Include parameters:

#### **Include definitions:**

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

### 3.14.3. Advanced settings:

#### **Newlib settings (see parameter description first):**

USE\_NEWLIB\_REENTRANT                          **Enabled \***

#### **Project settings (see parameter description first):**

Use FW pack heap file                          Enabled

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\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC2	PA3	ADC2_INP15	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC2_INP19	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PG9	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_IN_Q7
	PG11	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_IN_SCK
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_OUT_SCK
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SER_OUT_SER
SPI3	PB3(JTDO/T RACESWO)	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	OLED_SCK
	PB5	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	OLED_MOSI
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	FLASH_SCK
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	FLASH_MISO
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	FLASH_MOSI
GPIO	PE5	GPIO_Output	<b>Output Open Drain *</b>	No pull-up and no pull-down	Low	STATUS_LED_3
	PE6	GPIO_Output	<b>Output Open Drain *</b>	No pull-up and no pull-down	Low	STATUS_LED_4
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Very High *</b>	TIME_MARKER_3
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Very High *</b>	TIME_MARKER_4
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Very High *</b>	TIME_MARKER_1
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Very High *</b>	TIME_MARKER_2
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Medium *</b>	SLIDERS_S0
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Medium *</b>	SLIDERS_S1
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Medium *</b>	SLIDERS_S2
	PF13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EX_HEART_BEAT
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Medium *</b>	SER_OUT_RCLK

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	POTS_S0
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	POTS_S1
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	POTS_S2
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	OLED_CS
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	OLED_DC
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	OLED_RES
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	FLASH_CS_2
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	SER_IN_PL
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	FLASH_CS_1
	PB8	GPIO_Output	<b>Output Open Drain *</b>	No pull-up and no pull-down	Low	STATUS_LED_1
	PB9	GPIO_Output	<b>Output Open Drain *</b>	No pull-up and no pull-down	Low	STATUS_LED_2

#### 4.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_TX	DMA1_Stream0	Memory To Peripheral	Low
ADC2	DMA1_Stream1	Peripheral To Memory	<b>Medium *</b>

##### SPI2\_TX: DMA1\_Stream0 DMA request Settings:

Mode: Normal  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

##### ADC2: DMA1\_Stream1 DMA request Settings:

Mode: **Circular \***  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word

#### 4.3. BDMA configuration

nothing configured in DMA service

#### 4.4. MDMA configuration

nothing configured in DMA service

## 4.5. NVIC configuration

### 4.5.1. NVIC

Interrupt Table	Enable	Preenemption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
ADC1 and ADC2 global interrupts	true	5	0
TIM1 update interrupt	true	15	0
TIM2 global interrupt	true	5	0
TIM4 global interrupt	true	5	0
SPI2 global interrupt	true	5	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	5	0
PVD/AVD through EXTI Line detection Interrupt		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
SPI1 global interrupt		unused	
SPI3 global interrupt		unused	
FPU global interrupt		unused	
SPI5 global interrupt		unused	
HSEM1 global interrupt		unused	

### 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false

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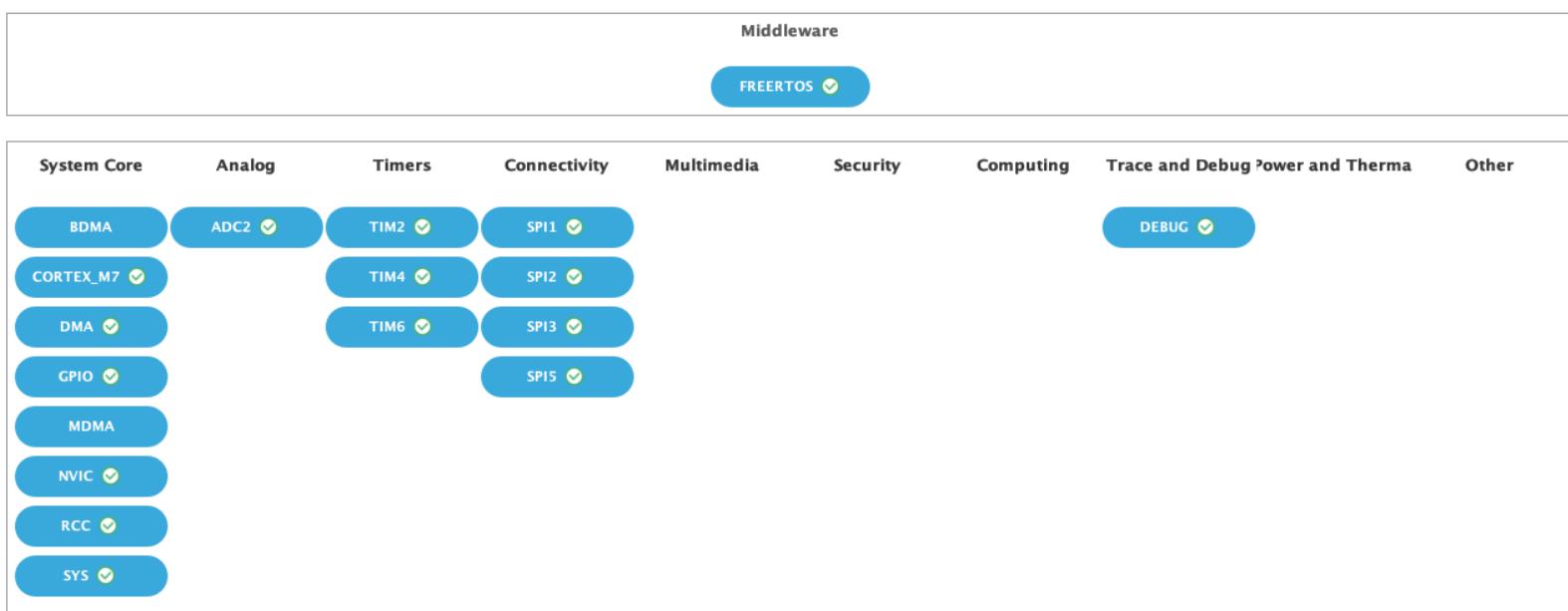
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
TIM1 update interrupt	false	true	true
TIM2 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true

\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current



## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip</a>
System View	<a href="https://www.st.com/resource/en/svd/stm32h7-svd.zip">https://www.st.com/resource/en/svd/stm32h7-svd.zip</a>
Description	
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
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Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf</a>
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Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32h7rs.pdf">https://www.st.com/resource/en/flyer/flstm32h7rs.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-">https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-</a>

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