

Hardware resource	# available	Cycle 1	Cycle 2	Cycle3
8 bit multiplier	2	$a * b,$ $c * d$		
16 bit adder	1		$p + q$	

Hardware resource	# available	Cycle 1	Cycle 2	Cycle3
8 bit multiplier	1	$a * b$	$c * d$	
16 bit adder	1			$p + q$