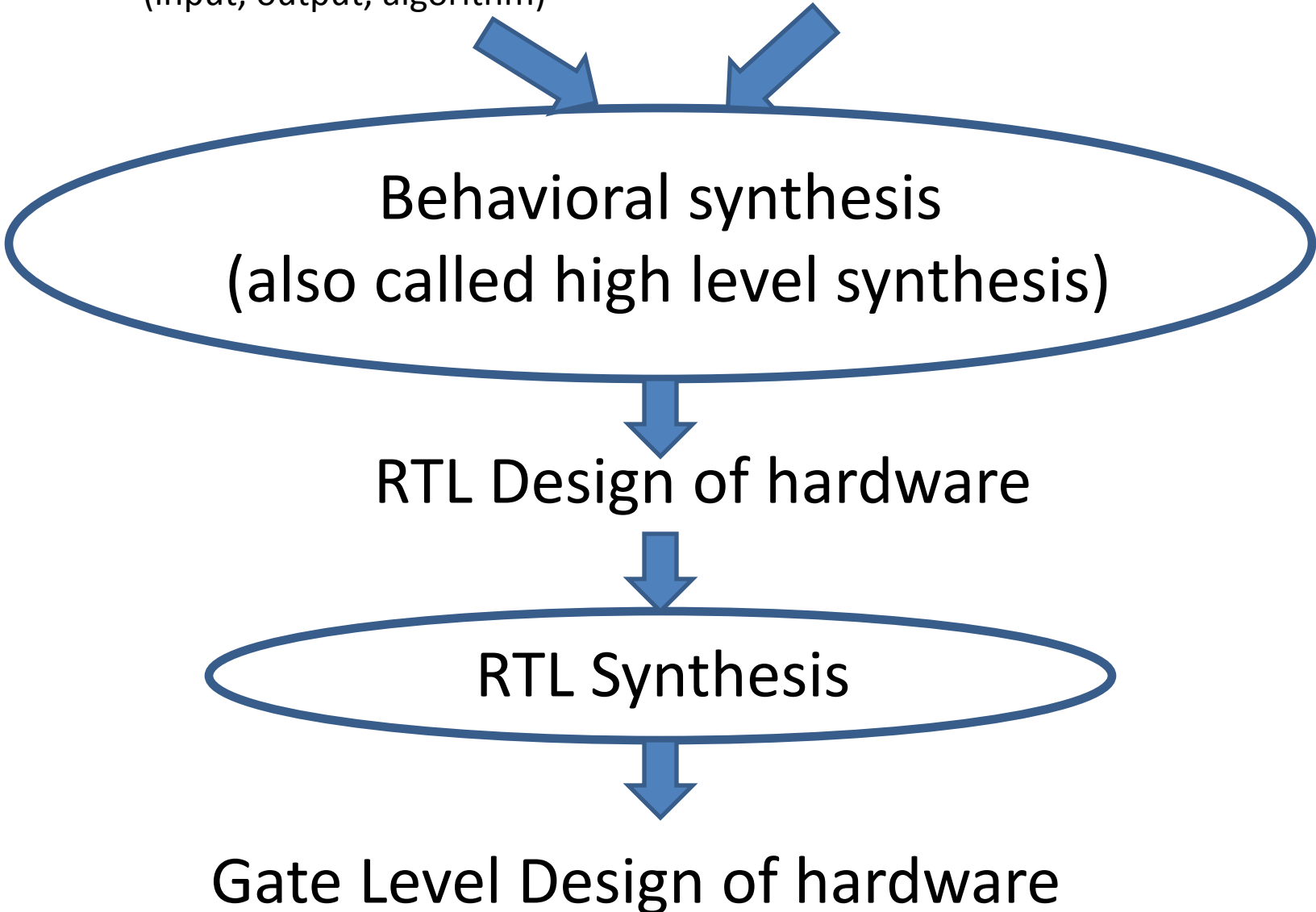


High Level behavioral specification
(input, output, algorithm)

Library of hardware resources



```
graph TD; A[High Level behavioral specification<br/>(input, output, algorithm)] --> B(Behavioral synthesis<br/>(also called high level synthesis)); C[Library of hardware resources] --> B; B --> D[RTL Design of hardware]; D --> E(RTL Synthesis); E --> F[Gate Level Design of hardware];
```

Behavioral synthesis
(also called high level synthesis)

RTL Design of hardware

RTL Synthesis

Gate Level Design of hardware