ECE 337 CDL

Group 3

Team Members

Workload Distribution

1) Disha Maheshwari: Receiver, top level test bench, receiver test bench
2) Stuti Rastogi: Transmitter, top level test bench, transmitter testbench
3) Neha Sharma: FIFO, AHB-lite-slave, and corresponding testbenches

Top Level Test Cases (Will be demonstrated in the DEMO)

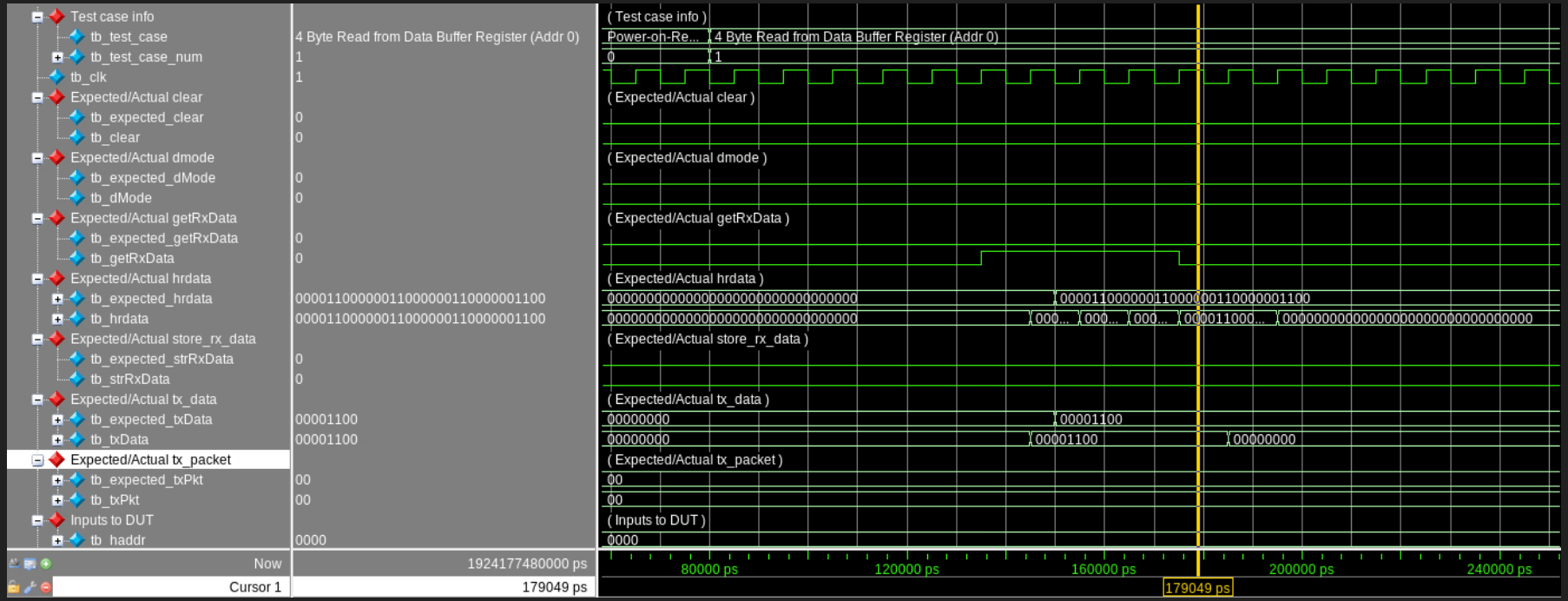
1) Transmit an ACK Handshake
2) Transmit a NAK Handshake
3) Transmit a STALL Handshake
4) Receiver to AHB ACK Handshake
5) Receiver to AHB IN Handshake
6) Receiver sends data to buffer, AHB reads data from buffer
7) Receiver tries writing more than 64 bytes on the buffer, RX Error goes high and error is read from the AHB lite slave.
8) FIFO sends data to transmitter

AHB-Lite Slave Test Cases

- 1 Byte Read and Write from Data Buffer Register (Addr 0)
- 2 Byte Read and Write from Data Buffer Register (Addr 0)
- **4 Byte Read and Write from Data Buffer Register (Addr 0)**
- Overlapping Reads from status register then error register
- 1 Byte Write to Packet Control Register (Addr C)
- 1 Byte Write to Flush Buffer Control Register (Addr D)
- 1 Byte Overlapping Writes to Flush Buffer Control and Packet Control Register (Addr C,D)
- 1 Byte Write to a read only register
- 1 Byte Write to an invalid register
- 1 Byte read from an invalid register

AHB-Lite Slave Waveforms

4 Byte Read from Data Buffer Register (Addr 0):



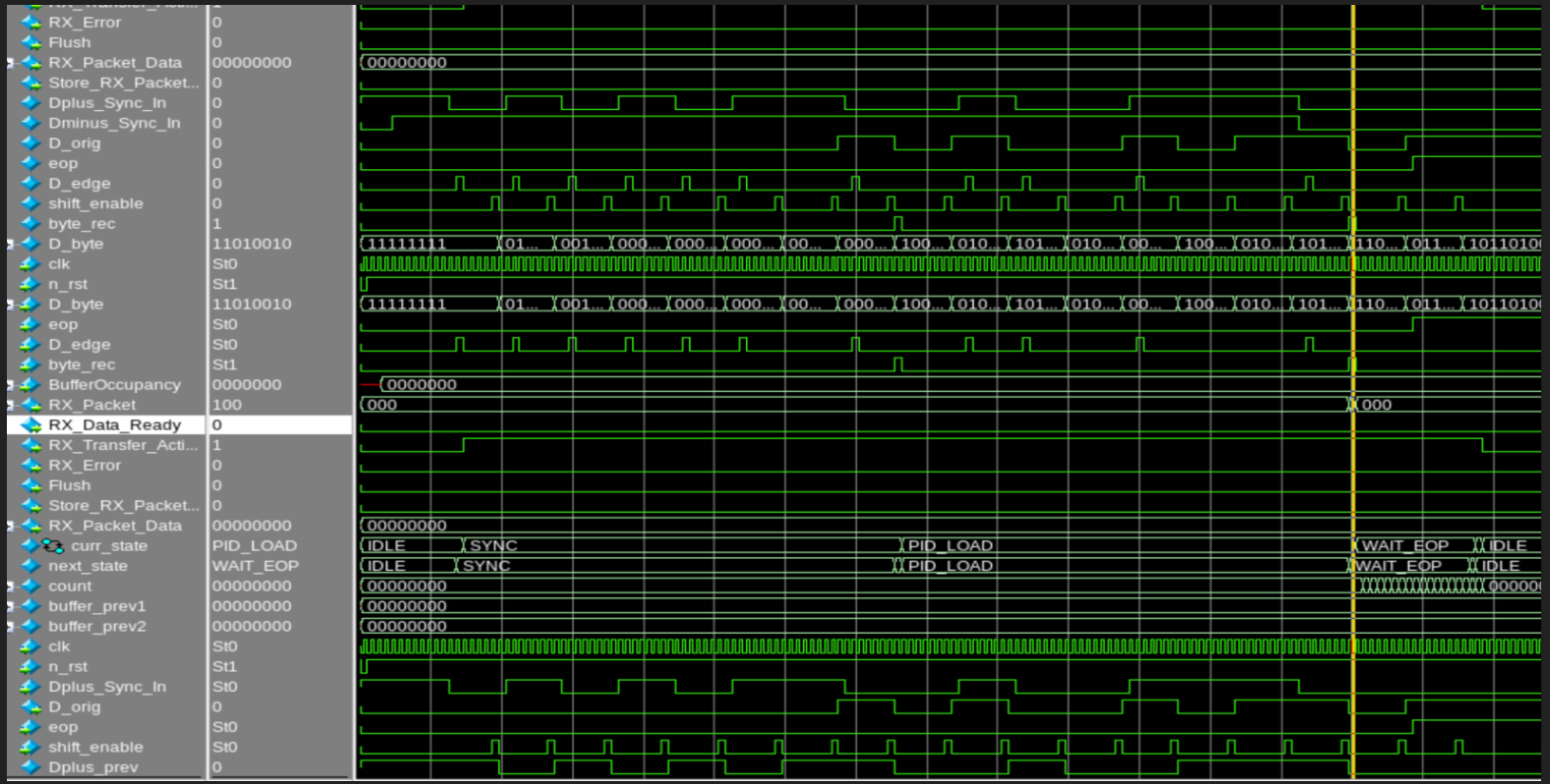
Data Buffer (64B FIFO) Test Cases

- Flush the FIFO
- Push 1 Byte into FIFO from the AHB Lite
- Push 1 byte consecutively into FIFO from the AHB Lite
- Push 1 byte consecutively into FIFO from the AHB Lite, then pop twice immediately

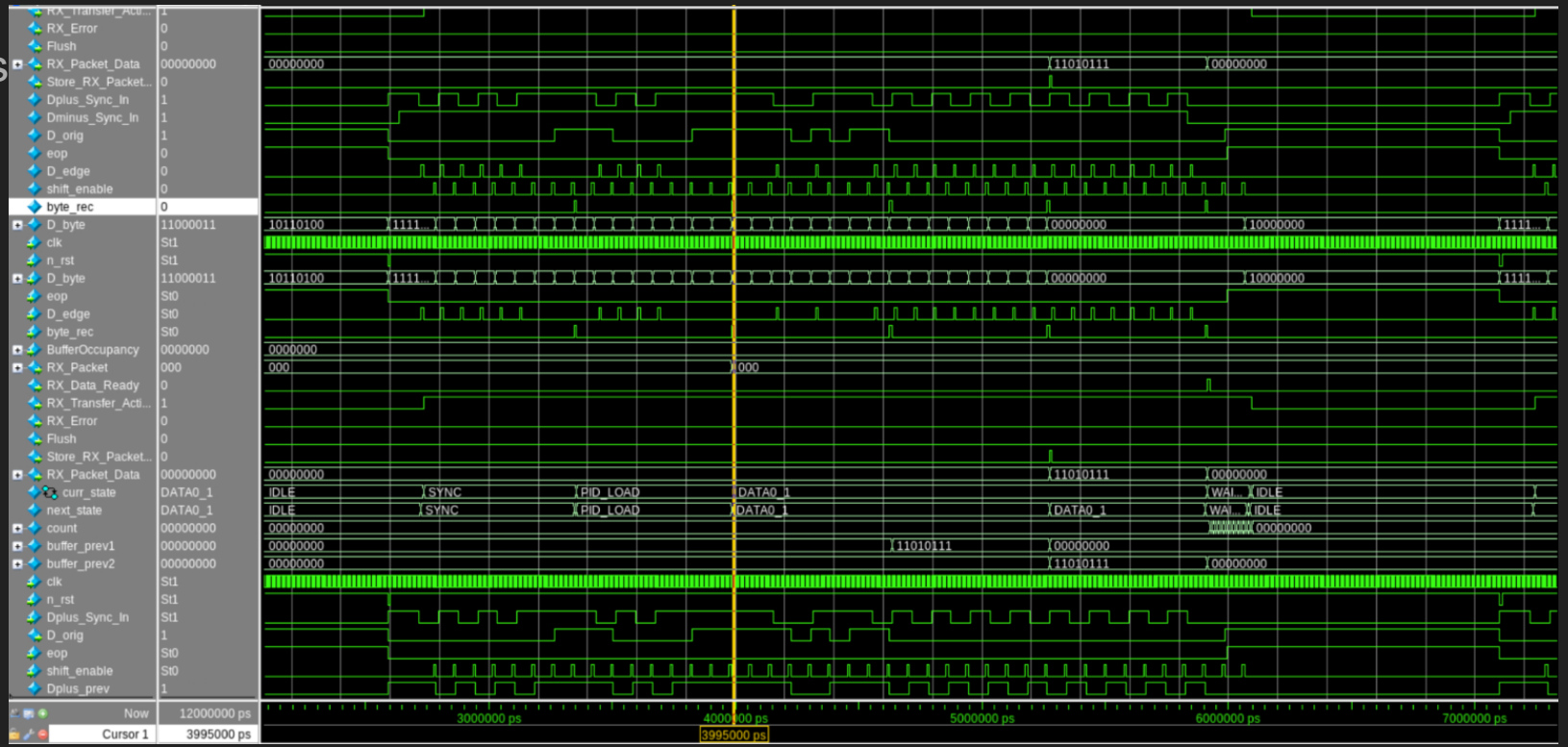
Receiver Test Cases

- Send ACK
- Send 1 DATA byte
- Send IN/OUT

Receiver Waveforms (ACK)



Receiver Waveforms (DATA)



Transmitter Test Case

```
/************************Test case 1: Behavior with ACK*************************************************
 // Synchronize to falling edge of clock to prevent timing shifts from prior test case(s)
@(negedge tb_clk);
 tb_test_num  += 1;
 tb_test_case = "Behavior with ACK";

 tb_test_buffer_occupancy  = '0;
 tb_test_TX_Packet          = 3'd2;
 tb_test_TX_Packet_Data     = '0;

 tb_expected_TX_Transfer_Active  = 0;
 tb_expected_TX_error    = 1'b0;
 tb_expected_Get_TX_packet_data = 0;

 check_outputs();

 #83.3;

 tb_expected_TX_Transfer_Active  = 1;
 tb_expected_TX_error    = 1'b0;
 tb_expected_Get_TX_packet_data = 0;

 check_outputs();
```

Transmitter Waveforms

```
VSIM 1> run 2000ns
# ** Info: Test case 0: TX Transfer Active correctly asserted
#    Time: 8750 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 87
# ** Info: Test case 0: DUT correctly shows an error
#    Time: 8750 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 93
# ** Info: Test case 0: DUT correctly shows Get_TX_packet_data
#    Time: 8750 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 98
# ** Info: Test case 1: TX Transfer Active correctly asserted
#    Time: 10 ns  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 87
# ** Info: Test case 1: DUT correctly shows an error
#    Time: 10 ns  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 93
# ** Info: Test case 1: DUT correctly shows Get_TX_packet_data
#    Time: 10 ns  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 98
# ** Info: Test case 1: TX Transfer Active correctly asserted
#    Time: 93300 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 87
# ** Info: Test case 1: DUT correctly shows an error
#    Time: 93300 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 93
# ** Info: Test case 1: DUT correctly shows Get_TX_packet_data
#    Time: 93300 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 98
# ** Info: Test case 1: TX Transfer Active correctly asserted
#    Time: 176600 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 87
# ** Info: Test case 1: DUT correctly shows an error
#    Time: 176600 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 93
# ** Info: Test case 1: DUT correctly shows Get_TX_packet_data
#    Time: 176600 ps  Scope: tb_TX_top_level.check_outputs File: source/tb_TX_top_level.sv Line: 98
```

Transmitter Waveforms (ACK)