Disha Maheshwari

765-767-2068 | dsmahesh@purdue.edu | https://www.linkedin.com/in/disha-m03/

Education

Purdue University *Jan 2022 – May 2025*
BS in Computer Engineering ***GPA**: 3.97/4.0*
Concentration in Artificial Intelligence, Computer Systems, Software Engineering
Minor in Mathematics,
Certificate in Applications of Data Science
Courses: *Data Structures in C, Microprocessor Systems, OOP in C++, Computer Graphics, AI, Operating Systems, Signals and Systems, Animation (Maya), ASIC, NLP, Computer Security, Software Engineering, Computer Networks, Computer Design and Prototyping*

Work Experience

Amazon *June 2025 – Present*
Software Development Engineer *Tempe, AZ, US*

- Worked on feature computation platform integral for fraud detection pipeline which included a Java-based service handling 147.7M feature computation per second worldwide during business-as-usual (BAU) operations and Python-based service handling 2.25M TPS during BAU with 3K tasks, supporting p99 latency of 20-80ms.
- Led critical end-to-end security migration for multiple services, successfully migrating bindings from insecure HTTP to secure HTTPS as part of achieving 100% encryption-in-transit compliance for Tier-1 services
- Set up new service cells and service infrastructure in multiple AWS regions for Shadow Testing as part of service migration and datacenter migrations.
- Performed on-call duties managing incident escalation, root cause analysis, implementing measures to reduce future operational risk and managed high-traffic scaling operations for multiple services.
- Enabled secure database calls by passing auth tokens from incoming requests through the request context.

Amazon *May 2024 – Aug 2024*
SDE Intern *Tempe, AZ, US*

- Implemented and deployed a scalable authentication pipeline in the cloud (AWS) for a java based service.
- Built an S3 interface to fetch authentication data periodically, designed an in-memory auth refresher for comparison, and implemented caching.

OakRidge National Laboratory *May 2023 – Aug 2023*
Research Intern *Oak Ridge, TN, US*

- Implemented Spinking Neural Networks as a Neuromorphic Architecture on the Artix-7 FPGA on Basys3 in Verilog using Xilinx Vivado Development Tool.
- Designed and Packaged IP including UART transceiver, receiver modules with baud rate of 9600bps for FPGA interfacing, customized FIFO modules and SNN modules running on 100MHz clock.
- Worked on optimizing and analyzing FPGA utilization, used debugging tools for troubleshooting FPGA designs.

Research

Research Assistant *June 2024 - June 2025*
Professor Ruqi Zhang

- Developed SDSI, a variational inference framework that constrains posterior variances to a sparse, low-dimensional subspace, enabling scalable Bayesian NNs.
- Proposed a subspace addition strategy preserving high-gradient directions, enhancing accuracy and calibration across clean and corrupted datasets.
- Achieved 76.36% accuracy, 0.9655 AUROC, and 0.0014 ECE on CIFAR-100 (10% subnet), outperforming Sparse BNNs, VBLL methods, and Laplace Subnetworks.

Additional Projects

[Re] BiRT: Bio-inspired Replay in Vision Transformers for Continual Learning *Nov 23 - Jun 24*

- Conducted a reproducibility study on BiRT, a continual learning framework using vision transformers with constructive noises and an episodic memory replay to mitigate catastrophic forgetting.
- Evaluated model performance on benchmark datasets, providing key insights into BiRT's reproducibility and practical applicability and published the findings in ReScience C Journal.

Dual Core Cache Coherent Pipelined RISC-V Processor *Jan 2025- Apr 2025*
System Verilog, Questa Sim

- Designed a 5-stage pipelined RISC-V CPU with variable-latency RAM, hazard handling, branch prediction; implemented & integrated memory controller & datapath
- Implemented split instruction/data caches complete with MSI coherence protocol over two cores.

CLI for Trustworthy Modules
Typescript, REST API, GraphQL *Aug – Dec 2024*

- Developed APIs and corresponding UI to store, rate and perform various operations an Node.js packages and GitHub repositories in Typescript and hosted it on AWS EC2, used dynamoDB and S3 for storage.

USB Full-Speed Bulk-Transfer Endpoint AHB-Lite SoC Module
System Verilog, Questa Sim *Mar 2024 - Apr 2024*

- Developed a high-performance System on Chip (SoC) module that integrates a USB full-speed bulk-transfer endpoint with an AHB-Lite slave interface, data buffer, and USB RX/TX functionalities.

Wisebucks.AI (Founder) *July 2023 – May 2024*

- Won **$6000** worth funding in JMEC startup incubator in a team of 6
- Developed an integrated platfrom offering financial insights, portfolio suggestions, trading simulation, and chatbot. support for user queries, using a combination of traditional and state of the art data analysis techniques.

Procedural Modelling of Terrain *Apr – May 2023*
OpenGL, C++, glfw, glad, glsl

- Used diamond square algorithms to generate height maps, implemented GPU shaders using glsl library.
- Built graphic pipeline including vertex shading, camera transformations, mouse/key controls.

Technical Skills

- **Languages**: Python, Pytorch, C, C#, C++, Java, SQL, JavaScript, HTML/CSS, TypeScript, Arduino, MATLAB, ReactJS, Verilog
- **Tools**: Git, VS Code, Visual Studio, Vim, IntelliJ, Linux, Bash, Vim, Sublime, Vivado, Maya, Unity, Docker, Kubernetes, AWS
- **Libraries**: Pandas, NumPy, SciPy, scikit-learn, matplotlib, OpenGL, GLSL, PyTorch, jQuery, Flask,

Publications

An FPGA-based Neuromorphic Processor with All-To-All Connectivity First Author
IEEE ICRC 2023 (Accepted)
[Re]Bio-Inspired Replay in Vision Transformers
ReScience 2025 (Accepted) First Author

Awards

William Hart Hayt Jr. Memorial, Charles W Brown Scholarship & Gold Expo Scholarship
JEE : 99.65 percentile, **KVPY**: AIR 205