An Efficient Design of a Reversible Fault Tolerant n-to-2^n Sequence Counter Using Nano Meter MOS Transistors

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Abstract. This paper proposes an efficient reversible synthesis for the n-to-2^n sequence counter, where $n \geq 2$ and $n\epsilon\ N$. The proposed circuits are designed using only reversible fault tolerant gates. Thus, the entire circuit inherently becomes fault tolerant. In addition, an algorithm to design the n-to-2^n reversible fault tolerant sequence counter based on fault tolerant J-K flip-flops has been presented. The functional verification of the proposed circuit is completed through the simulation results. Moreover, the comparative results show that the proposed method performs much better and is much more scalable than the existing approaches.

Keywords: Counter · Fault tolerant · Reversible logic · Transistor

1 Introduction

In logic computation, every bit of information loss generates $KTln2$ joules of heat [1]. These heat dissipation can be reduced to zero joule, if the circuit is constructed only with reversible gates as it maintains one-to-one mapping between inputs-outputs and thus recovers from bit loss [2]. Moreover, reversible circuit is also viewed as a special type of quantum circuit because quantum evaluation must be reversible [3]. On the other hand, fault tolerant reversible gate can detect faulty signal in its primary outputs through parity checking. Researchers showed that an entire circuit can preserve parity if its individual gate is parity preserving [4–6]. In addition, reversible and fault tolerant computing gained remarkable interests in the development of highly efficient algorithms [7,8], optimal architecture [4], simulation and testing [5], DNA and nano-computing [9], quantum dot cellular automata [10] etc. In these consequences, this paper investigates the design methodologies for the reversible fault tolerant sequence counter based on low power MOS transistor. The counter is used in the control unit of a

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microprocessor [11]. It has also been used in memory and I/O [12]. The transistor implementation of the reversible circuits is considered in this paper because of its scalability and easier fabrication process [4–6].

2 Basic Definitions and Literature Review

Some basic definitions, notations and background study of the existing works are presented in this section.

2.1 Reversible and Fault Tolerant Gates

An n bit ***reversible gate*** is a data block that uniquely maps between input vector $I_v = (I_0, I_1, ..., I_{n-1})$ and output vector $O_v = (O_0, O_1, \ldots, O_{n-1})$ [6]. The ***Fault tolerant gate*** is a reversible gate that preserves parity between inputs and outputs [5]. In other words, an n-bit fault tolerant gate maintains the following property among the inputs and outputs:

$$I_0 \oplus I_1 \oplus ... \oplus I_{n-1} = O_0 \oplus O_1 \oplus ... \oplus O_{n-1} \quad (1)$$

2.2 Garbage Output, Hardware Complexity and Quantum Cost

The output of a reversible gate that neither used as primary output nor as input to another gate is the **garbage output** [6], *i.e.*, the output which are needed only to maintain the reversibility is known as garbage output [7]−[12]. The number of basic operations (AND, OR, NOT, Ex-OR, etc.) needed to realize a gate/circuit is referred as its ***hardware complexity*** [4,5]. The ***quantum cost*** of a reversible gate is the total number of 2×2 quantum gate used in it, since quantum cost of the all 1×1 and 2×2 reversible gates is considered as 0 and 1, respectively [7]−[12]. The quantum computer with many qubits is difficult to realize. Thus, the reversible circuit with the fewer quantum cost is considered as beneficial.

2.3 Popular Reversible Fault Tolerant Gates

Feynman double gate ($F2G$) and Fredkin gate (FRG) are the most popular reversible fault tolerant gates. Following subsections present these gates along with their all necessary properties. This section also presents the transistor representations of these gates. We already proposed these representations in [5,6] using 901 and 920 MOS models. But in this paper we use advanced p-MOS 901(ax4) and n-MOS 902(bx5) for more efficient realization.

Feynman Double Gate. Inputs and outputs for a 3×3 $F2G$ is define as follows: $I_v = (a, b, c)$ and $O_v = (a, a \oplus b, a \oplus c)$. Block diagram of $F2G$ is shown in Fig. 1(a), whereas Fig. 1(b) represents $F2G$'s quantum equivalent realization. From Fig. 1(b), we find that an $F2G$ is realized with two 2×2 Ex-OR gates and thus its quantum cost is two. Figs. 1(c) and (d) represent the transistors realization and the corresponding timing diagram of $F2G$[1].

[1] Throughout the paper we consider the signal less than $0.01ns$ stability are glitches and thus omitted from the simulation results. Moreover, considering these gate representation as schema all the proposed circuit of Sec. 3 is simulated.

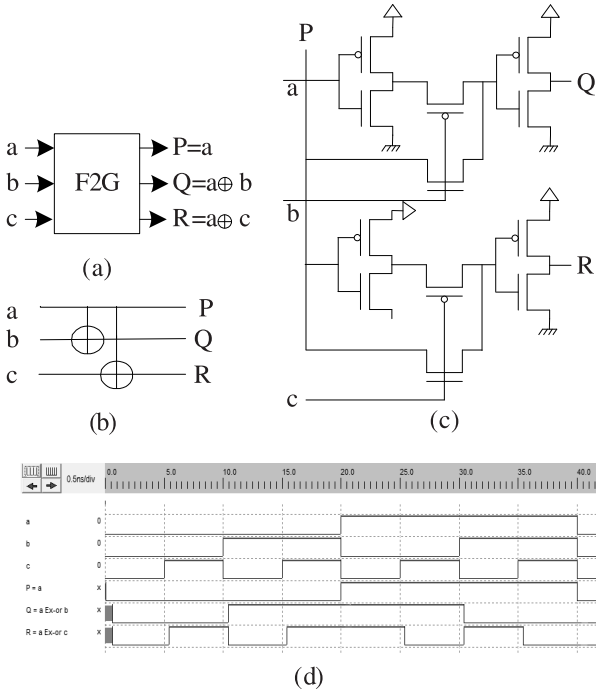


Fig. 1. Reversible 3×3 Feynman double gate (a) Block diagram (b) Quantum equivalent realization (c) Transistor equivalent realization (d) Simulation result

Fredkin Gate. Input-output vectors of a 3×3 FRG is define as follows: $I_v = (a, b, c)$ and $O_v = (a, a'b \oplus ac, a'c \oplus ab)$. The block diagram of an FRG is shown in Fig. 2(a). Fig. 2(b) represents the quantum equivalent realization of the FRG. To realize the FRG, four transistors are needed as shown in Fig. 2(c). The corresponding timing diagram of Fig. 2(c) is shown in Fig. 2(d), which proves the functional correctness of the proposed realization. It has been shown in [4–6] that both $F2G$ and FRG maintain the parity preserving property of Eq. (1).

3 Proposed Reversible Fault Tolerant Sequence Counter

This section illustrates the design methodologies of the proposed reversible fault tolerant sequence counter. The proposed counter for a reversible fault tolerant microprocessor based on J-K flip-flops is designed. The working procedure of the proposed J-K flip-flop is dependent both on its previous state and clock. There are several designs of reversible sequence counters in the literature among which the design from [13] is considered to be the most compact and efficient. In this section, initially we propose a reversible fault tolerant J-K flip-flop. Then, the proposed flip-flop is used to design the proposed fault tolerant counter circuit.

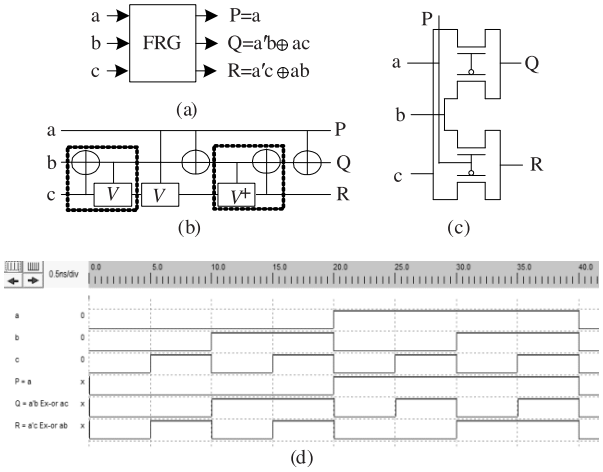


Fig. 2. Reversible 3 × 3 Fredkin gate (a) Block diagram (b) Quantum equivalent realization (c) Transistor equivalent realization (d) Simulation result

3.1 Proposed Reversible Fault Tolerant J-K Flip-Flop

Fig. 3(a) presents the architectural block diagram of the proposed reversible fault tolerant J-K flip-flop. The corresponding quantum equivalent realization is shown in Fig. 3(b). From the quantum representation of the proposed flip-flop, we find that the proposed J-K flip-flop is constructed with total of nine 2×2 quantum equivalent gates. Thus its total quantum cost should be nine. But, in this quantum realization, there are two consecutive Ex-OR gate, one from FRG and the other from $F2G$ (dashed area), which have the identical level from its I/O. As shown by the researchers [5,6], if there are two consecutive Ex-OR gates with identical I/O level, then it only represents a quantum wire and is realized without any quantum cost. Thus, the total quantum cost of the proposed fault tolerant J-K flip-flop is 7 rather than 9.

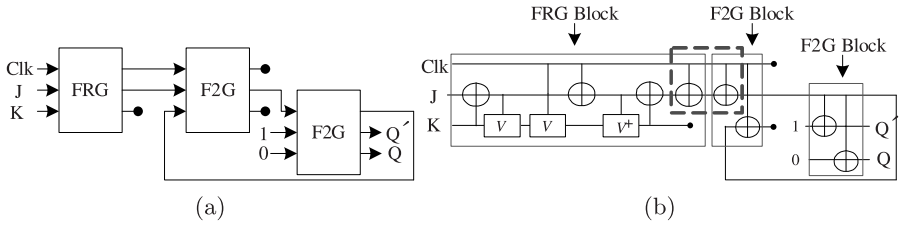


Fig. 3. Proposed reversible fault tolerant J-K flip-flop (a) Architectural block diagram (b) Quantum equivalent realization

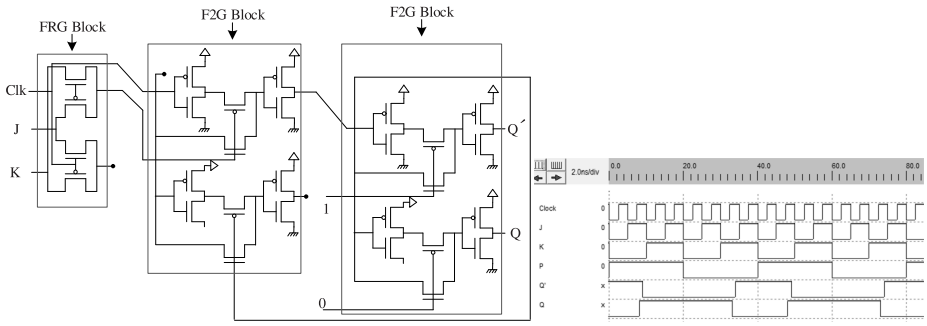


Fig. 4. Proposed J-K flip-flop (a) Transistor realization (b) Simulation result

Transistor equivalent realization of the proposed reversible fault tolerant J-K flip-flop is shown in Fig. 4(a). The corresponding simulation result is shown in Fig. 4(b), which proves the functional correctness of the proposed circuit. From Fig. 4(b), we find that the output Q depends on both the clock and the P. The P represents the value of previous state, which is initially set to high. When clock is low, the value of J or K has no effect on Q (0 to $2ns$). However, when clock is high, Q doesn't change its state till 5 ns, as both J and K are low during this time. If the clock changes from low to high, J is set to high, K is set to low and Q becomes high (10 to 25 ns). In opposite case, Q also stays at high (25 to 35 ns). But, if both J and K are set to high, then Q is equal to P'. Table. 1 shows the comparison of the proposed fault tolerant J-K flip-flop with the existing non-fault tolerant flip-flops. Generally, a fault tolerant design is much more expensive than the non-fault tolerant design. However, Table. 1 shows that the proposed design performs much better than the existing non-fault tolerant designs which is also much scalable[2].

Table 1. Comparison of reversible J-K flip-flops

Evaluation Criteria	QC	HC	TR	P	CD	CL	DS
Existing Circuit [11]	14	$9\alpha + 8\beta + 2\gamma$	39	58.5	1.8901	1755	0.0325
Existing Circuit [13]	12	$4\alpha + 5\beta + 4\gamma$	33	49.5	2.1357	1485	0.0275
Proposed Circuit	7	$4\alpha + 4\beta + 2\gamma$	28	21.0	0.3082	1260	0.0233

[2] In this table and all the following tables, we consider QC=Quantum cost, HC=Hardware Complexity, TR=No. of Transistors, P=Average Power Consumption in nW, CD=Critical Path Delay in ns, CL=Average Channel Length and DS=Average Density per $kgates/mm^2$. We also consider that α, β, γ are the hardware complexities of a two-input Ex-OR, an AND and a NOT calculations respectively.

3.2 Proposed Reversible Fault Tolerant Sequence Counter

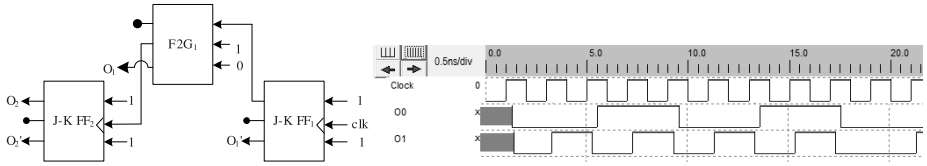
Fig. 5(a) shows the architectural block diagram of the proposed 2-to-4 sequence counter[3]. The combination of one $F2G$ and two reversible fault tolerant J-K flip-flops schema can work together as a 2-to-4 **R**eversible **F**ault tolerant **S**equence **C**ounter (RFSC). From now on, we denote a reversible fault tolerant sequence counter as RFSC. The corresponding simulation result is shown in Fig. 5(b). Figs. 6(a) and (b) present the architecture of a 3-to-8 RFSC and its corresponding simulation result, respectively. From the presented simulation results, we find that the initial clock transition occurs at $1ns$ and the output becomes available in $1.637ns$. Thus, the maximum possible delay of the proposed circuit is less than $0.65ns$. Algorithm 1 presents the detailed design procedure of the proposed n-to-2^n RFSC. Primary inputs of this proposed algorithm are clock pulse, $F2G$ and FRG. Initially, the algorithm builds an architectural block of the proposed reversible fault tolerant J-K flip-flop (RFJKFF), which is shown in lines 5 to 10 of the Algorithm 1. Then, n numbers of RFJKFF blocks and (n-1) numbers of $F2G$s are used to create the entire structure of the n-to-2^n RFSC.

Algorithm 1. Algorithm for the proposed reversible fault tolerant n-to-2^n sequence counter, ***RFSC(clk, F2G, FRG)***

Input : Clock pulse *clk*, $F2G$ and FRG
Output: n-to-2^n reversible fault tolerant sequence counter circuit

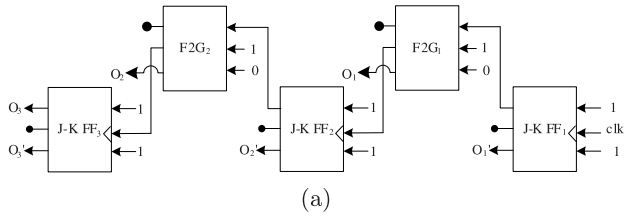
1 **begin**
2 $i = input$, $o = output$
3 **begin procedure**
4 ***RFJKFF(clk, F2G, FRG)***
5 $clk \rightarrow first.i.FRG$,
6 $J \rightarrow second.i.FRG$,
7 $K \rightarrow third.i.FRG$
8 $first.o.FRG \rightarrow first.i.F2G_1$, $second.o.FRG \rightarrow second.i.F2G_1$, $third.o.FRG \rightarrow third.i.F2G_1$
9 $second.o.F2G_1 \rightarrow first.i.F2G_2$, $1 \rightarrow second.i.F2G_2$, $0 \rightarrow third.i.F2G_2$
10 $second.o.F2G_2 \rightarrow Q', third.o.F2G_2 \rightarrow Q$,
11 **end procedure**
12 **for** $j \leftarrow 2$ **to** n **do**
13 **call *RFJKFF (clk, F2G, FRG)*** $first.o.RFJKFF \rightarrow first.i.F2G_{j-1}$, $1 \rightarrow second.i.F2G_{j-1}$, $0 \rightarrow third.i.F2G_{j-1}$,
14 $second.o.F2G_{j-1} \rightarrow second.i.RFJKFF_j$, $remaining.i.RFJKFFR \leftarrow 1$
15 $third.o.F2G_j \rightarrow Q_{j-1}$
16 $first_j.o.RFJKFF \rightarrow Q_j$
17 **end for**
18 **return** *remaining F2G.o, FRG.o and RFJKFF.* $\rightarrow$ *garbage outputs.*
19 **end**

[3] This is trivial case *i.e.*, n=2.

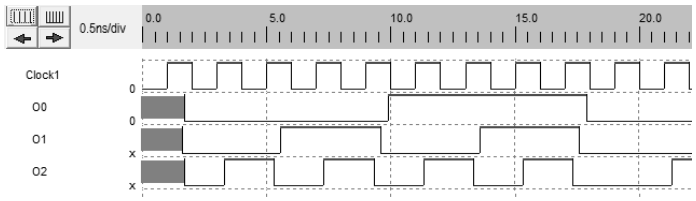


(a) (b)

Fig. 5. Proposed 2-to-4 RFSC (a) Architecture (b) Simulation result



(a)



(b)

Fig. 6. Proposed 3-to-8 RFSC (a) Architectural block diagram (b) Simulation result

Table 2. Comparison of Reversible Sequence Counters

n	Proposed Method			Existing Method [11]			Existing Method [13]		
	QC	TR	HC	QC	TR	HC	QC	TR	HC
2	16	68	$10\alpha + 8\beta + 4\gamma$	35	95	$27\alpha + 24\beta + 6\gamma$	25	72	$7\alpha + 10\beta + 8\gamma$
3	25	108	$16\alpha + 12\beta + 6\gamma$	56	151	$45\alpha + 40\beta + 10\gamma$	38	111	$24\alpha + 15\beta + 12\gamma$
4	34	148	$22\alpha + 16\beta + 8\gamma$	59	207	$63\alpha + 56\beta + 14\gamma$	51	150	$34\alpha + 20\beta + 16\gamma$

4 Evaluation of the Proposed Methods

Table 2 compares the performance of the proposed scheme with the existing methods [11,13]. From this table, we find that the performance of the proposed method is much better and has significantly better scalability than the existing approaches with respect to all the evaluation parameters.

5 Conclusions

The paper has presented a compact design of the reversible fault tolerant n-to-2^n counter based on J-K flip flops. The representation of each gate is shown using transistors, which are further used in the design of the proposed circuit. The corresponding simulation results have also been presented. All the simulation results evidenced that the proposed fault tolerant circuits work correctly. The comparative results show that the proposed design is much more scalable than its counterparts [11, 13]. In addition, this paper has addressed the problem with the gate level quantum cost calculation in the reversible circuits, which is an interesting research work for future quantum circuits [3, 6].

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