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Design of a Compact Reversible Random Access Memory

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Abstract—**Conventional logic dissipates more power by losing bits of information whereas reversibility recovers bit loss from the unique input-output mapping. Thus reversible logic has become immensely popular research area and its applications have spread in various technologies. In this paper we have proposed the reversible logic synthesis of Random Access Memory with a newly proposed 3×3 reversible gate named as FS. This reversible design of Random Access Memory has less number of gates, garbage outputs and quantum cost compared with the existing ones. In the way of designing a reversible Random Access Memory we have proposed $n \times 2^n$ reversible decoder, reversible D flip-flop and write-enabled master-slave D flip-flop which have outperformed those described in the literature. Moreover we have proposed five lower bounds for designing reversible decoder as well as reversible Random Access Memory.**

Keywords- reversible logic; garbage output; flip-flop; quantum cost

I. INTRODUCTION

Reversible logic has spread its popularity in numerous technologies such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing[1],thermodynamics and nanotechnology over the last couple of years[2, 3, 4]. In the early 1960s R. Landauer demonstrated that losing bits of information causes loss of energy [5]. It is proved that the loss of each bit of information loses at least KT × ln2 joules of energy where K is the Boltzmann's constant and T is the temperature at which the system is operating [5]. Information is lost when an input cannot be recovered from its output or vice-versa. Reversible logic has the feature to generate one to one correspondence between its input and output [6,7,8]. As a result no information is lost in reversible logic and zero power dissipation would be achieved only if the network consists of reversible gates [9]. Synthesis of reversible logic is more complicated than irreversible one as it imposes many design constraints [6]. A reversible circuit therefore should have the following attributes [7]:

- Since garbage outputs are not used as primary outputs so any realization technique should keep garbage as minimum as possible.
- Each reversible gate has a particular quantum cost so any realization technique should keep the number of reversible gates as minimum as possible.
- Input lines that are either 0 or 1 known as constant inputs should be as minimum as possible.

Random Access Memory's (RAM) internal architecture can be viewed as a two dimensional array of memory cells. Each memory cell stores a single bit of data. In this paper we have proposed a reversible architecture of Random Access Memory with a newly proposed reversible gate and some proposed sequential circuits. With the help of theorems and lemmas the efficiency of reversible logic synthesis of RAM has also been proved in this paper.

The paper consists of the following sections: Section II describes about the reversible gate, some basic definition and quantum realization of some reversible circuits. Section III introduces the logic synthesis of reversible Random Access Memory and comparison with other existing researches. Finally the paper is concluded with the section IV.

II. BACKGROUND

In this section we have presented some definitions and basic idea on reversible logic for our future reference. Quantum realization of some popular reversible circuits has also been illustrated in this section.

A. A *Reversible Gate* is an $n \times n$ data stripe block which uniquely maps between input vector $I_v = (I_0, I_1, . . . , I_n)$ and output vector $O_v = (O_0, O_1, . . . , O_n)$ denoted as $I_v \leftrightarrow O_v$ [10].
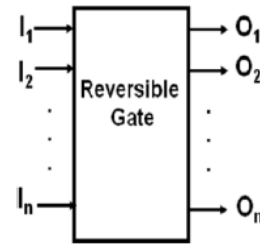

Figure 1.   A k × k Reversible Gate

B. Every gate output that is not used as input to other gates or as a primary output is known as *Garbage*.

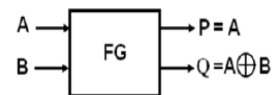

Figure 2.   A Reversible Gate with One Garbage Output

C. Every quantum circuit is built from 1×1 and 2×2 quantum primitives and its cost is calculated as a total sum of 2×2 gates used since 1×1 gate costs nothing i.e. zero. Basically the quantum primitives are matrix operation which is applied on qubits state. All the gates of the form 2×2 has equal quantum cost and the cost is unity i.e. 1 [11]. Since every reversible gate is a combination of 1×1 or 2×2 quantum gate, therefore the *Quantum Cost* of a reversible circuit calculates the total number of 2×2 gates used. The quantum cost of Feynman gate in Figure 2 is 1 and the quantum cost of Feynman Double gate in Figure 3 is 2.

D. The *Delay* of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the following two assumptions[11]:
Firstly, each gate performs the computation in one unit time. This means that every gate in the given circuit will take same amount of time for internal logic operations. Secondly, all inputs to the circuit are known before the computation begins. Which means that the internal structure and each operation of the gate is known before the calculation. From the above definition, the delay of the logic circuit of Figure 2 which consists of only one gate is obviously 1 as this is the only gate from its input to output line.

E. A *Fault Tolerant Gate* is a reversible gate which constantly preserves same parity between input and output, more specifically an $n \times n$ fault tolerant gate holds the following property: $I_0 \oplus I_1 \oplus I_2 \oplus \ldots \oplus I_{n-1} = O_0 \oplus O_1 \oplus O_2 \oplus \ldots \oplus O_{n-1}$ The circuit which consists of all fault tolerant gates must preserve the parity pattern in its input and output vectors.

F. Let I_v and O_v be the input and output vector of a 3×3 *Feynman Double Gate*, (F2G) [12] respectively, where $I_v = (A, B, C)$ and $O_v = (P=A, Q= A \oplus B, R= A \oplus C)$. The quantum cost of Feynman Double gate is 2 [11, 13] which has been shown is Figure 4.
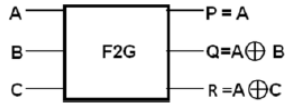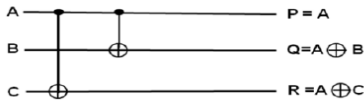

Figure 3.   A 3×3 Reversible Feynman Double Gate

Figure 4.   Quantum Realization of 3×3 Reversible Feynman Double Gate

G. Let I_v and O_v be the input and output vector of a 3×3 *Toffoli Gate* (TG) [14] respectively, where $I_v = (A, B, C)$ and $O_v = (P = A, Q = B, R = AB \oplus C)$. In Figure 6, V is the square root of NOT gate and V^+ is its hermitian. Thus $VV^+ = I$ (an identity matrix, describing just a quantum wire). The quantum cost of Toffoli gate is therefore 5 [11, 13].
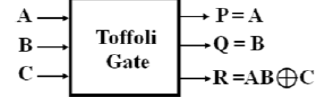

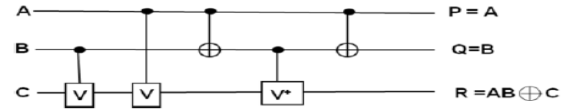Figure 5.   A 3×3 Reversible Toffoli Gate

Figure 6.   Quantum Realization of 3×3 Reversible Toffoli Gate

H. Let I_v and O_v be the input and output vector of a 3×3 *Fredkin Gate* [15] respectively, where $I_v = (A, B, C)$ and $O_v = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$. Quantum equivalent circuit of FRG has been shown in Figure 8. Each dotted rectangle in this circuit is equivalent to one 2×2 FG and so the cost is 1 for that particular case. Thus the quantum cost of Fredkin gate turns out to be 5 like Toffoli gate [11].
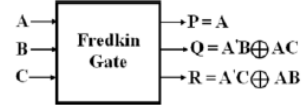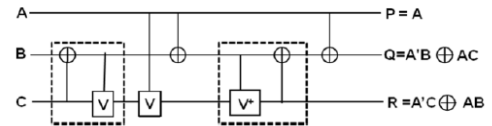

Figure 7.   A 3×3 Reversible Fredkin Gate

Figure 8.   Quantum Realization of 3×3 Reversible Fredkin Gate

III.   PROPOSED REVERSIBLE RANDOM ACCESS MEMORY

In this section we have proposed a compact and improved version of reversible Random Access Memory in comparison with the existing design of [16] and [17]. In the process of proposing this better design we also have proposed a 3×3 reversible FS gate which has been described with its quantum realization in the section III A. With the proposed gate a compact $n \times 2^n$ decoder has been realized in section III B. As flip-flop is an essential and core part of RAM for bit storage we have successfully managed to realize a compact version of D flip-flop and write-enabled master-slave D flip-flop. The designs are described in the section III C and III D respectively.

Figure 11. Proposed Design of 2×2^2 Reversible Decoder

A. Proposed 3×3 Reversible Gate

A new 3×3 reversible gate is proposed in this section of the paper which is known as FS gate. The reversibility of the gate is shown in Table I. The quantum equivalent circuit of reversible FS gate has been realized in Figure 10 where template matching technique [18] has been used to calculate the overall cost and each block has been marked from 1 to 6 where block 5 and 6 don't incur any cost.
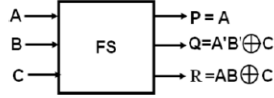

Figure 9. A 3×3 Reversible FS Gate

TABLE I. TRUTH TABLE FOR THE 3×3 FS GATE

A	B	C	P	Q	R
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	1	0
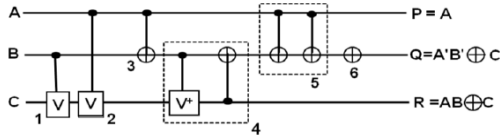
Figure 10. Quantum Realization of 3×3 Reversible FS Gate

Lemma I: A 3×3 reversible FS gate with the following outputs P = A, Q = A'B'⊕C and R = AB⊕C has the minimum quantum cost i.e. 4.

Proof: In Figure 10, the quantum equivalent circuit of a 3×3 reversible FS gate has been shown, where each of the blocks marked as 1 to 4 has quantum cost 1 and blocks 5 and 6 don't have any quantum cost i.e. 0. So the total quantum cost of the FS gate is minimum i.e. 4.

B. Proposed Design of Reversible Decoder

In this section we have explored the use of the proposed gate to generate a reversible decoder. The proposed 2×2^2 reversible decoder as well as $n \times 2^n$ are more efficient than [16] and [19] in terms of quantum cost and garbage bits. Comparisons of the proposed decoders with the existing ones have also been shown in this section. We also have proposed an algorithm to construct an **n** input decoder in this section.

Two 3×3 FS gates and one Feynman gate have been used to produce a reversible implementation of a 2×2^2 decoder. A comparative result is shown in Table II.
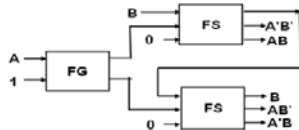

TABLE II. COMPARISON OF DIFFERENT 2×2^2 REVERSIBLE DECODER

	No. of Gates	No. of Garbage	Quantum Cost
Existing Circuit [16]	4	2	12
Existing Circuit [19]	3	1	11
Proposed Circuit	3	1	9

Algorithm I: $n \times 2^n$ Reversible Decoder

1. Take one **$(n-1) \times 2^{(n-1)}$** reversible decoder. Outputs of this block are considered to be of level L_{i-1}.

2. **For** each level L_i, where i = 3 to **n**
   Loop
   For j = 1 to 2^{i-1}
     Loop
   i.   Take one FS gate F_j
   ii.   **If** j = 1 then
   iii. $F_j [I_1]$ = n_{th} input of the decoder
   iv.   **Else**
   v. $F_j [I_1]$ = $F_{j-1} [O_1]$
   vi.   **End if**
   vii. $F_j [I_2]$ = j_{th} output from L_{i-1}
   viii. $F_j [I_3]$ = 0
       End Loop
     End Loop
3. **End**

Figure 12 shows 3×2^3 reversible decoder whereas the realization of an **$n \times 2^n$** reversible decoder has been shown in Figure 13 according to the Algorithm I.
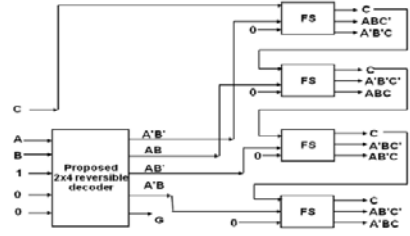

Figure 12. Proposed Design of 3×2^3 Reversible Decoder
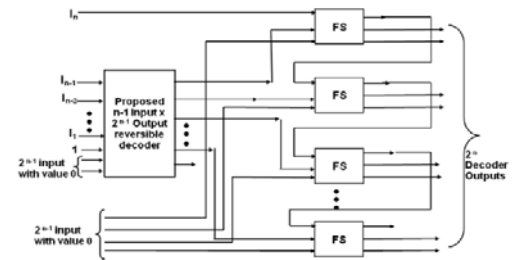

Figure 13. Proposed Design of **$n \times 2^n$** Reversible Decoder

Lemma II: An **$n \times 2^n$** reversible decoder can be realized with at least 2^{n-1} number of reversible gates.

Proof: According to Figure 11, a 2×2^2 reversible decoder can be realized with $2^2-1=3$ reversible gates using one Feynman gate and two FS gates. In the same way 3×2^3

decoder has $2^3 - 1 = 7$ gates. Thus, we can say that an $n \times 2^n$ reversible decoder can be realized with at least 2^{n-1} reversible gates.

Lemma III: An $n \times 2^n$ reversible decoder generates at least $n-1$ garbage outputs.

Proof: A 2×2^2 reversible decoder generates $2-1 = 1$ garbage output using Algorithm I. In the same way, a 3×2^3 decoder generates $3-1 = 2$ garbages. Hence an $n \times 2^n$ decoder can be realized with at least $n-1$ garbage outputs.

C. Proposed Design of Reversible D Flip-Flop

In this section we have proposed a reversible D flip-flop which can be used to store bits of data in a reversible memory. One FRG and one F2G have been used to design the D flip-flop which is shown in Figure 14. A comparative result of different D flip-flops has been shown in Table III.
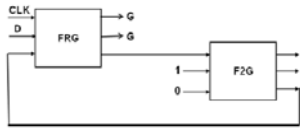

Figure 14. Proposed Design of Reversible D Flip-Flop

TABLE III.   COMPARISON OF DIFFERENT REVERSIBLE D FLIP-FLOP

	No. of Gates	No. of Garbage	Quantum Cost
Existing Circuit [16]	3	3	15
Existing Circuit [19]	3	2	7
Existing Circuit [20]	2	2	10
Proposed Circuit	2	2	7

D. Proposed Design of Write-Enabled Master-Slave D Flip-Flop

Since data is both read from and write into Random Access Memory, every flip-flop should be able to work on two modes: read and write [17]. So in the design of reversible Random Access Memory a write-enabled master-slave D flip-flop is a necessary component. In this section, Figure 15 has shown the compact design of write-enabled master-slave D flip-flop which consists of three Fredkin gates and four Feynman Double gates.
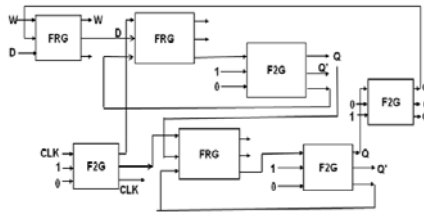

Figure 15. Proposed Design of Reversible Write-EnabledMaster-Slave D Flip-Flop

TABLE IV.   COMPARISON OF DIFFERENT REVERSIBLE WRITE-ENABLED MASTER-SLAVE D FLIP-FLOP

	No. of Gates	No. of Garbage	Quantum Cost
Existing Circuit [16]	9	9	38

Existing Circuit [17]	7	7	25
Proposed Circuit	7	6	23

E. Proposed Reversible Random Access Memory

We have proposed the reversible design of Random Access Memory in this section. A RAM is a two dimensional array of flip-flops. There are 2^n rows where each row contains m flip-flops. Each time only one of the 2^n output lines of the decoder is active which selects one row of FFs of the RAM. Whether a read or a write operation is performed depends on the W input. The algorithm of a reversible RAM is given in Algorithm II. Figure 16 shows the implementation of Algorithm II to realize the $m \times 2^n$ bit RAM.

Algorithm II: $m \times 2^n$ bit Reversible RAM
1. Take one $n \times 2^n$ reversible decoder
2. **For** each row $i = 1$ to 2^n, in RAM
    Loop
    i.   Take one Toffoli gate T_i
    ii.   **If** $i = 1$ then
    iii. $T_i [I_1]$ = Write Input (either 0 or 1)
    iv.   **Else**
    v. $T_i [I_1] = T_{i-1} [O_1]$
    vi.   **End if**
    vii. $T_i [I_2] = i_{th}$ output of the decoder
    viii. $T_i [I_3] = 0$
    ix.   **For** each $j = 1$ to m
    Loop
    x.   Take one reversible write-enabled master-slave D flip-flop FF_j
    xi. $FF_j [D] = D_j$, primary data input of the RAM
    xii.   **If** $j = 1$ then
    xiii. $FF_j [CP] = T_j [O_2]$
    xiv. $FF_j [W] = T_j [O_3]$
    xv.   **Else**
    xvi. $FF_j [CP] = CP$ output FF_{j-1}
    xvii. $FF_j [W] = W$ output FF_{j-1}
    xviii.   **End if**
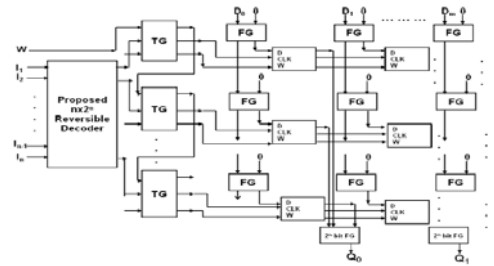   **End loop**
    End loop
3. **End**

Figure 16. F Proposed Design of Reversible RAM

F. Comparison of the Complexity of the Proposed Circuit with Existing Designs

In Table V, we have shown the number of gates, number of garbage outputs and quantum cost with respect to the existing designs.

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TABLE V.   COMPARISON OF DIFFERENT REVERSIBLE RANDOM ACCESS MEMORY

	No. of Gates	No. of Garbages	Quantum Cost
Existing Circuit [16]	$2^n (10m+2)$	$2^n(10m+2)+n+1*$	$88m+6.2^n -10$
Existing Circuit [17]	$2^n (8m+2)$	$2^n(8m+2)+n+1*$	$62m+6.2^n -10$
Proposed Circuit	$2^n (8m+2)-1$	$2^n(7m+3)+n$	$58m+4.2^n-7$

* CP (Clock Pulse) was not considered as garbage output generated from the master-slave D flip-flop at the last column in the design of reversible RAM.

Theorem I: Let gt_r be the number of gates required to realize an $m \times 2^n$ bit reversible RAM where n be the number of selection bits and m be the number of data bits in the reversible RAM. Then
$$gt_r \geq 2^n (8m+2) -1$$
Proof: The decoder part of a reversible RAM requires 2^{n-1} gates. And in the $m \times 2^n$ reversible RAM, there are $m \times 2^n$ write-enabled master-slave D flip-flops, where each flip-flop has 7 gates. In addition the RAM requires 2^n Toffoli gates and $m.2^n$ Feynman gates for AND and copy operations respectively. Therefore,
$$gt_r \geq 2^n -1 + 7.m.2^n + 2^n + m . 2^n$$
$$So, gt_r \geq 2^n (8m+2) -1$$

Theorem II: Let n be the number of selection bits and m be the number of data bits in the reversible Random Access Memory. Let, gar_r be the number of garbage outputs generated from the reversible RAM. Then
$$gar_r \geq 2^n (7m+3) +n$$
Proof: According to Lemma III, a reversible RAM generates $n-1$ garbages from its decoder. There are m numbers of Feynman gates at the last row in the design of the RAM, where each Feynman gate generates 1 garbage. Again there are 2^n rows in the last column in the design of the RAM, where each row requires a master-slave D flip-flop which generates 3 garbages. Moreover the write-enabled master-slave D flip-flop generates 6 garbages according to Table IV and Toffoli gate at the last row generates 1 garbage output. Again $m (2^n -1)$ garbage outputs are generated from the 2^n bit FG shown in Figure 16. Therefore,
$$gar_r \geq n -1 + m + 1 + 3.2^n +6. m. 2^n + m (2^n -1)$$
$$So, gar_r \geq 2^n (7m+3) + n$$

IV.   CONCLUSION

In this paper we have presented a compact design of reversible Random Access Memory. While developing the reversible design we have proposed a 3×3 reversible gate and some sequential circuits. It has been established with the help of comparison, lemmas and theorems that the proposed designs are better than the existing ones. Since reversible RAM can be used in various reversible circuits for data storage such as Field Programmable Gate Array (FPGA), reversible central processing unit design and quantum computers etc so we believe that our work may find its future use in numerous applications [1, 2, 3, 4].