East West University
Department of Computer Science and Engineering
Course Outline

Course Information

Course: CSE540 Synthesis and Optimization of Logic Circuits

Credit and Teaching Scheme:

	Theory	Laboratory	Total
Credit	3	0	3
Contact Hours	3 Hours/Week for 13 Weeks	0 Hours/Week for 13 Weeks	3 Hours/Week for 13 Weeks

Prerequisite: CSE207 Data Structures

Instructor Information

Instructor: Md. Shamsujjoha
Senior Lecturer, Department of Computer Science and Engineering
&
Assistant Proctor, East West University
Office: Room # 646
Tel. No.: 09666775577 (hunting) ext. 107
E-mail: dishacse@yahoo.com
URL: http://www.ewubd.edu/~msj/
TA: TBA

Class Routine and Office Hour

Day	11.50-01.20	01.30-03.00	03.10-04.40	04.50-06.50
Saturday	CSE 540 (1) Room: 637			
Sunday	CSE 245 (1) Room: 336	Office Hour	Office Hour	CSE 245 (2) Lab Room: 529
Monday	CSE 245 (2) Room: 638	Office Hour	CSE 245 (3) Room: 359	Office Hour
Tuesday	CSE 245 (1) Room: 530	Office Hour	Office Hour	Office Hour
Wednesday	CSE 245 (2) Room: 217	Office Hour	CSE 245 (3) Room: 359	CSE 245 (1) Lab Room: 638
Thursday				CSE 245 (3) Lab Room: 637

Course Objective

After successfully completing the course, students will be able to, Represent Boolean functions using binary decision diagrams and other canonical representations. Solve covering and satisfiability problems. Employ heuristic and exact two-level logic minimization techniques and understand testability properties of two-level logic circuits. Employ multi-level logic synthesis and optimization techniques targeting both area and speed and understand techniques targeting both area and testability properties of multi-level circuits. Employ sequential logic synthesis techniques including state minimization, state encoding and retiming. Employ technology mapping techniques for mapping circuits to a target library optimizing both area and speed. Employ high-level synthesis techniques including scheduling and allocation for architectural synthesis of circuits. Employ sequential logic synthesis techniques including state minimization, state encoding and retiming. Employ technology mapping techniques for mapping circuits to a target library optimizing both area and speed. Employ high-level synthesis techniques including scheduling and allocation for architectural synthesis of circuits.

Course Topics, Teaching-Learning Method, and Assessment Scheme

- Digital logic and integrated circuits.
- Design process and technology styles.
- Prerequisites review: Combinational and sequential circuit design.
- Data-path circuit design and optimization using polynomial algebra.
- Basic theory: set and graph concepts.
- Timing analysis and functional simulation.
- Formal verification
- Boolean algebras. Relations. Lattices. Algebra of Boolean functions.
- Cofactors. Boole/Shannon theorem. Binary decision diagrams (BDDs).
- Two-level optimization. Cube representation. Unate functions.
- Multilevel optimization. Algebraic division methods.
- Finite-state machines and sequential circuit optimization., Contemporary topics.

Assignments

Course Topic	Teaching-Learning Method	Exam (Mark)
Assignments with reports and presentations*	Individual, complex algorithm design and evaluation.	Assignment (10)

Overall Assessment Scheme

	Assessment Area Mark
Assessment Area	
Class Participation	5
Class Test/Quizzes	10
Midterm Exam - I	20
Midterm Exam -II	20
Final Exam	20
Assignments	10
Case Study, Presentation, Project Report	15
Total Mark	**100**

Teaching Materials/Equipment

Text Book:

- G. D. Micheli. Synthesis and Optimization of Digital Circuits, 1st edition, McGraw. Hill.

Reference Book(s):

- Hachtel, Gary D., and Fabio Somenzi. Logic Synthesis and Verification Algorithms, 1st ed. Boston, MA.: Springer.
- Md. Mozammel Huq Azad Khan, Digital Logic Design, Bangladesh University Grants Commission, Dhaka, Bangladesh.
- Ronald J. Tocci, Neal Widmer, Greg Moss, Digital Systems: Principles and Applications, 11th edition, Pearson.

Course Website:

- http://groups.yahoo.com/group/cse_msj
  - CSE-540

Project and Assignment Description:

Project and Assignment description will be provided.

Grading System

Marks (%)	Letter Grade	Grade Point	Marks (%)	Letter Grade	Grade Point
97-100	A+	4.00	73-76	C+	2.30
90-96	A	4.00	70-72	C	2.00
87-89	A-	3.70	67-69	C-	1.70
83-86	B+	3.30	63-66	D+	1.30
80-82	B	3.00	60-62	D	1.00
77-79	B-	2.70	Below 60	F	0.00

Exam Dates

Section	Term I	Term II	Final
1	08 June 2018	13 July 2018	11 August 2018

Academic Code of Conduct

Academic Integrity:

Any form of cheating, plagiarism, personification, falsification of a document as well as any other form of dishonest behavior related to obtaining academic gain or the avoidance of evaluative exercises committed by a student is an academic offence under the Academic Code of Conduct and **may lead to severe penalties as decided by the Disciplinary Committee of the university.**

Special Instructions:

- **Late assignments suffer a penalty rate of 20% per day, up to 5 days (weekends count towards the 5 days).**
- Assignments that are more than 5 days late are penalized by 100%. Group-based assignment must be done in group of 3. **STRICTLY NO COPYING** from others.
- Students are expected to attend all classes and examinations. A student MUST have at least 80% class attendance to sit for the final exam.
- Students will not be allowed to enter into the classroom after 20 minutes of the starting time.
- For plagiarism, the grade will automatically become zero for that exam/assignment.
- Normally there will be **NO make-up exam**. However, in case of **severe illness, death of any family member, any family emergency, or any humanitarian ground**, if a student miss any exam, the student MUST get approval of makeup exam by written application to the Chairperson through the Course Instructor **within 48 hours** of the exam time. Proper supporting documents in favor of the reason of missing the exam have to be presented with the application.
- For **final exam**, there will be NO makeup exam. However, in case of **severe illness, death of any family member, any family emergency, or any humanitarian ground**, if a student miss the final exam, the student MUST get approval of **Incomplete Grade** by written application to the Chairperson through the Course Instructor **within 48 hours** of the final exam time. Proper supporting documents in favor of the reason of missing the final exam have to be presented with the application. **It is the responsibility of the student to arrange an Incomplete Exam within the deadline mentioned in the Academic Calendar in consultation with the Course Instructor**.
- All mobile phones MUST be turned to silent mode during class and exam period.
- There is **zero tolerance for cheating** in exam. Students caught with cheat sheets in their possession, whether used or not; writing on the palm of hand, back of calculators, chairs or nearby walls; copying from cheat sheets or other cheat sources; copying from other examinee, etc. would be treated as cheating in the exam hall. The only penalty for cheating is **expulsion for several semesters as decided by the Disciplinary Committee of the university**.