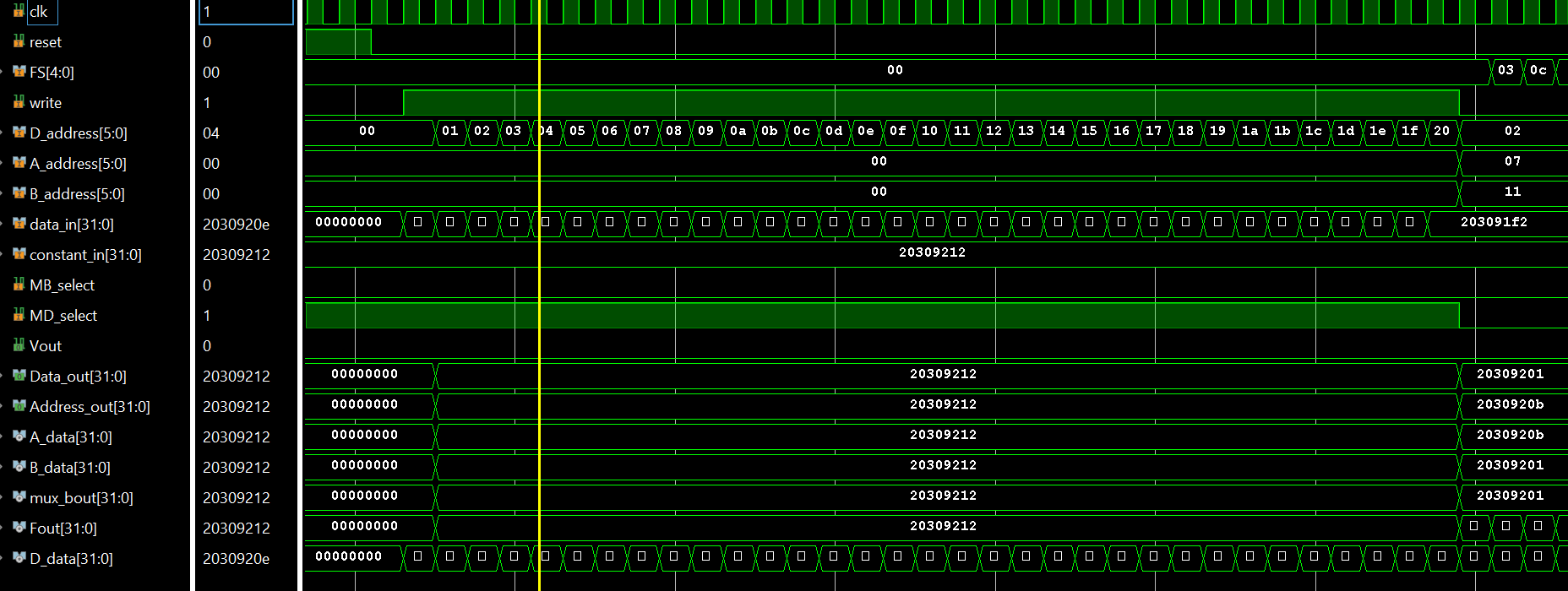
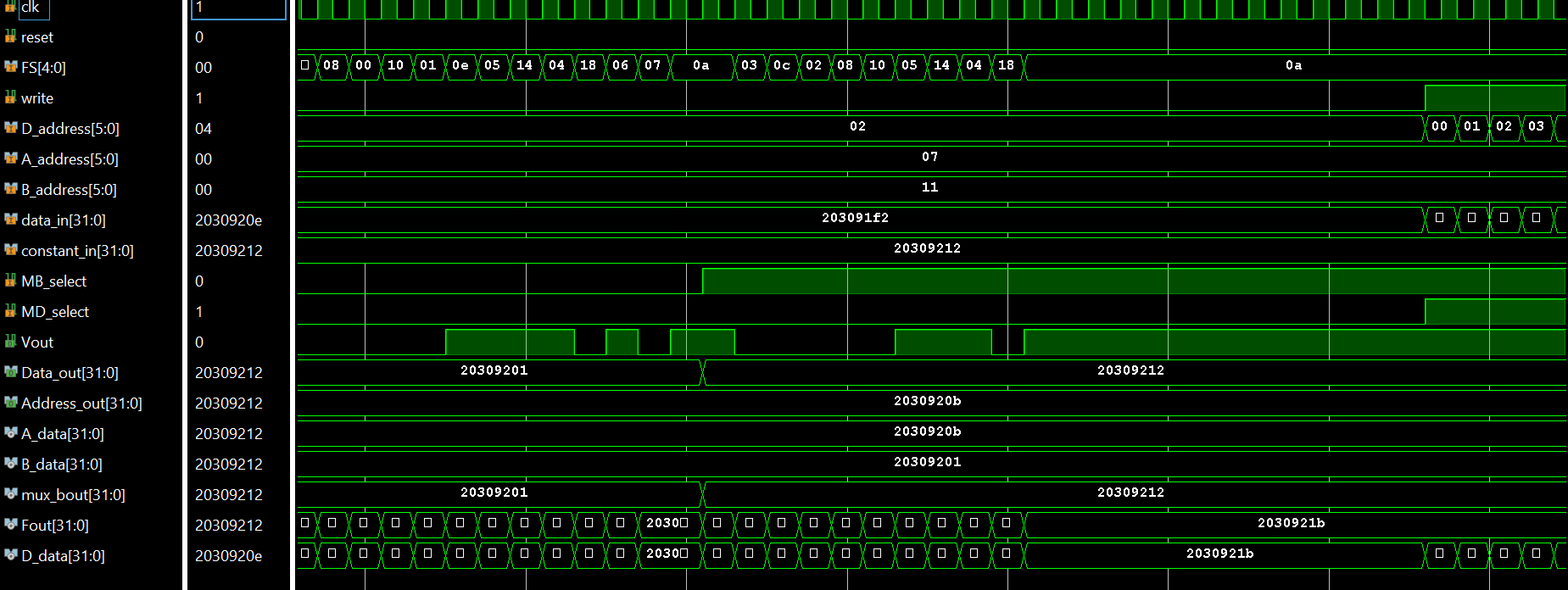
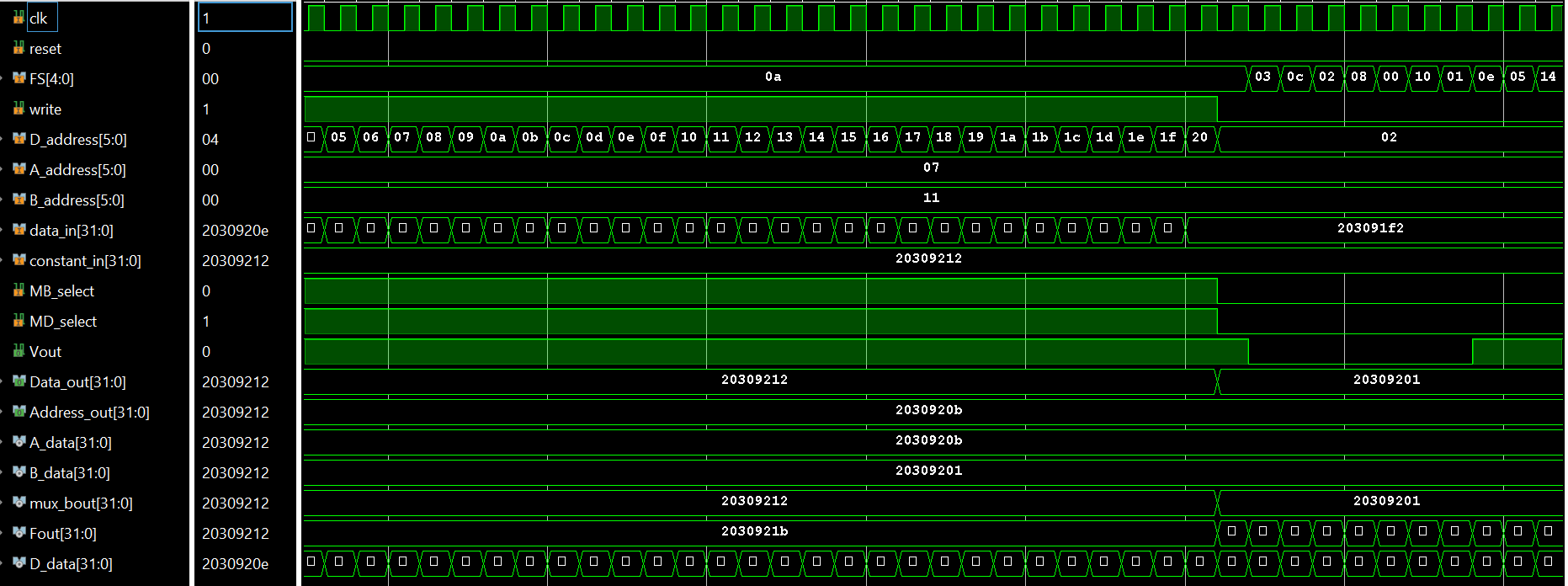
Datapath simulation



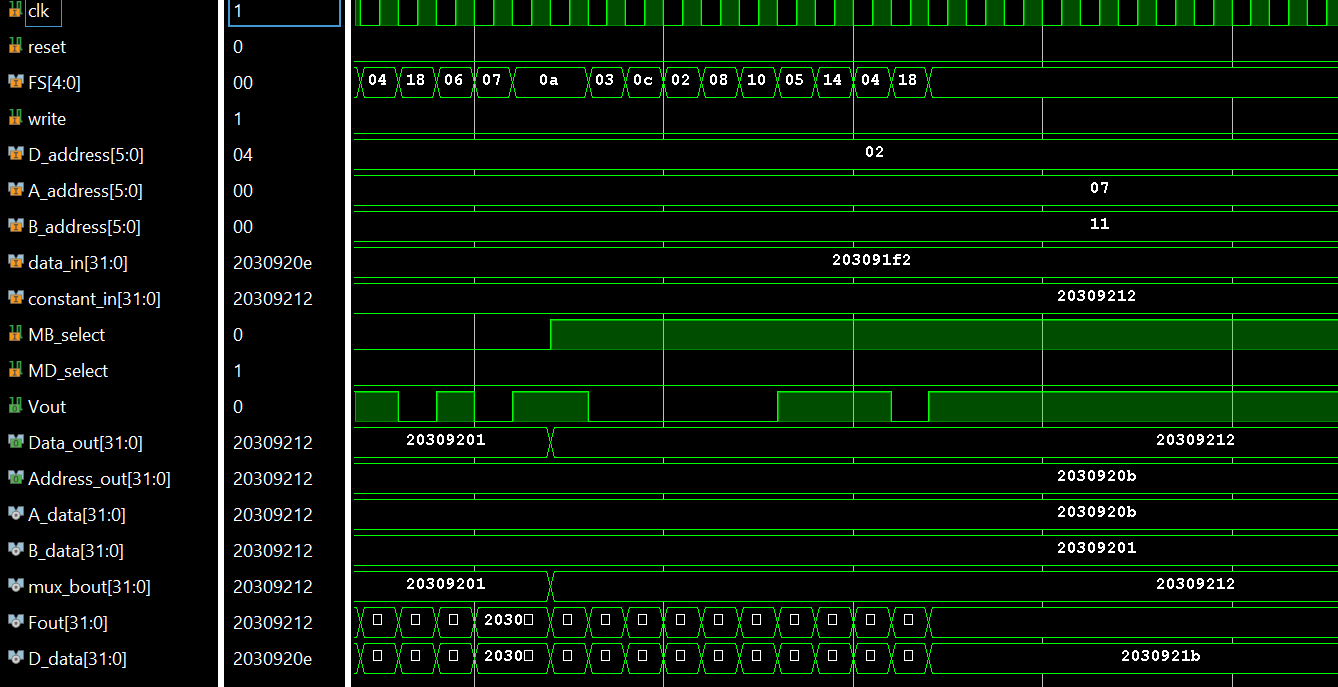
Further in time



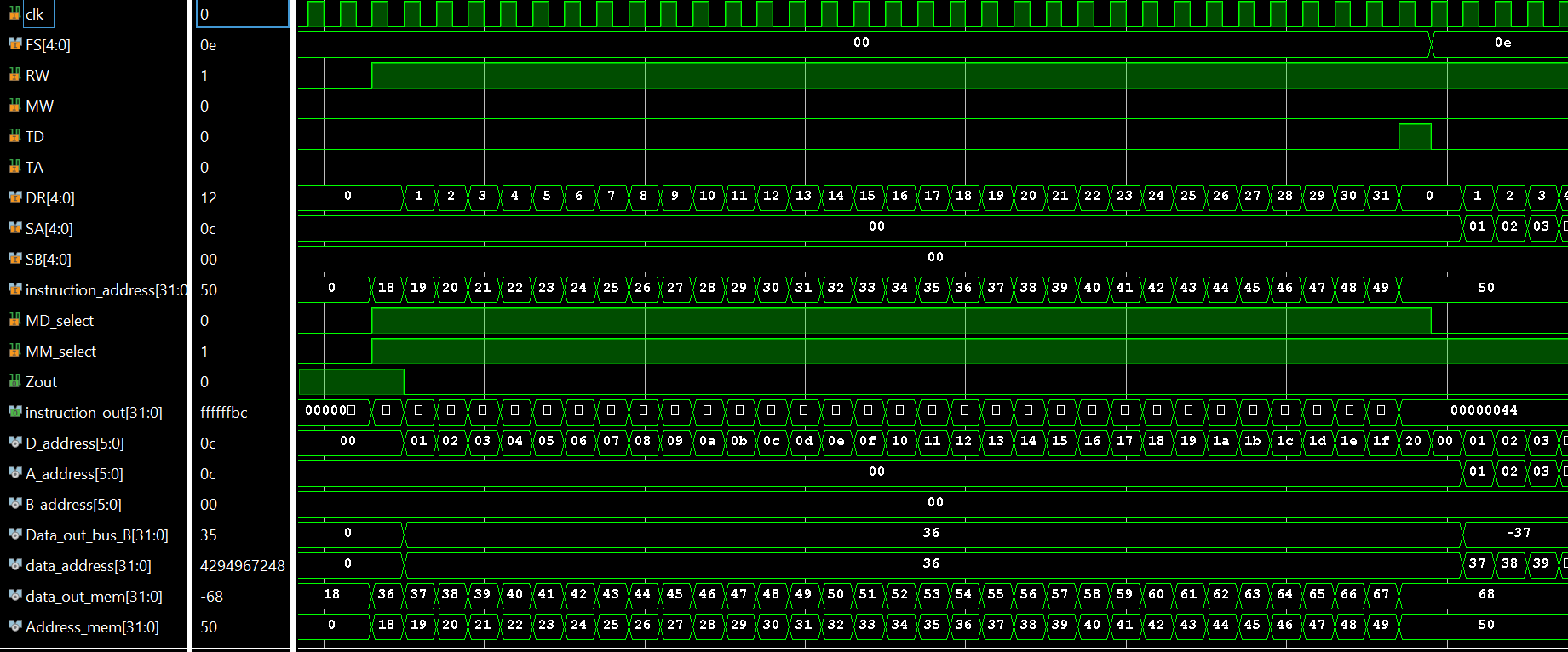
Further in time



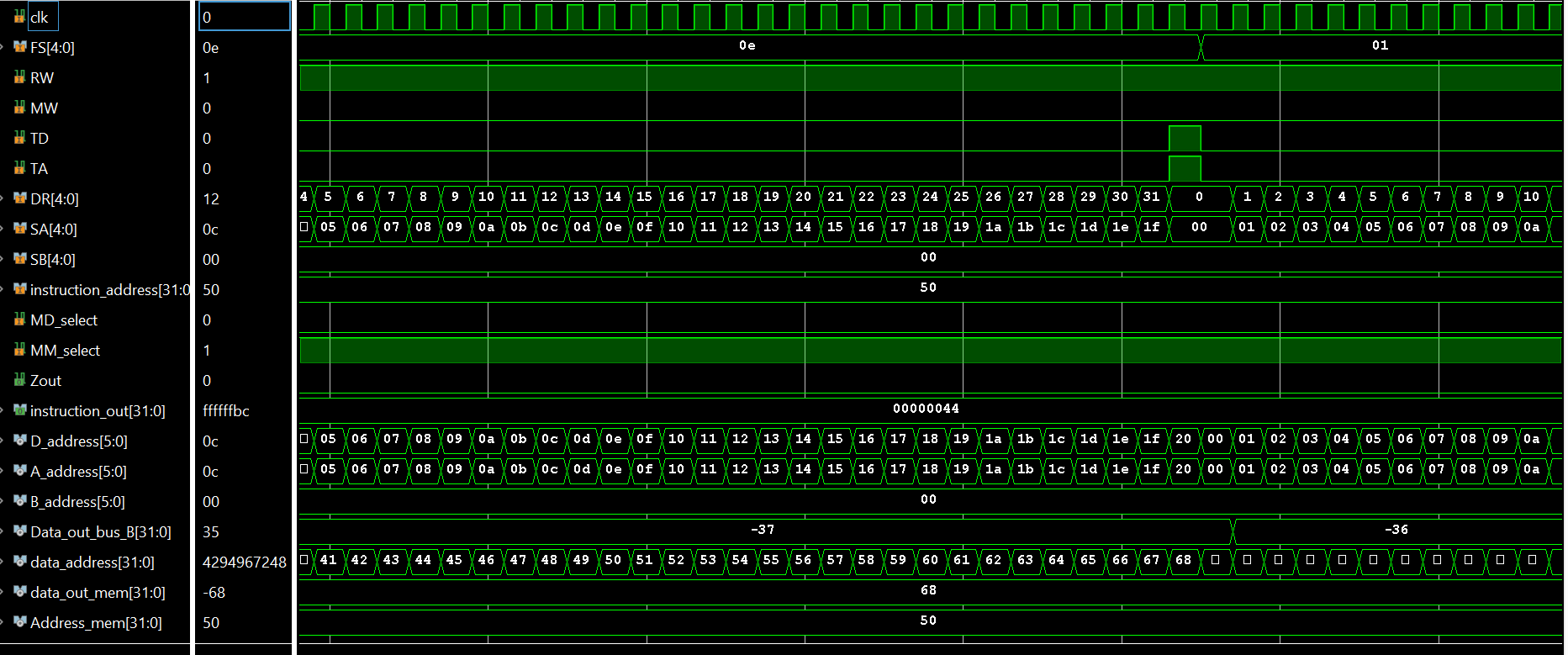
Futher in time



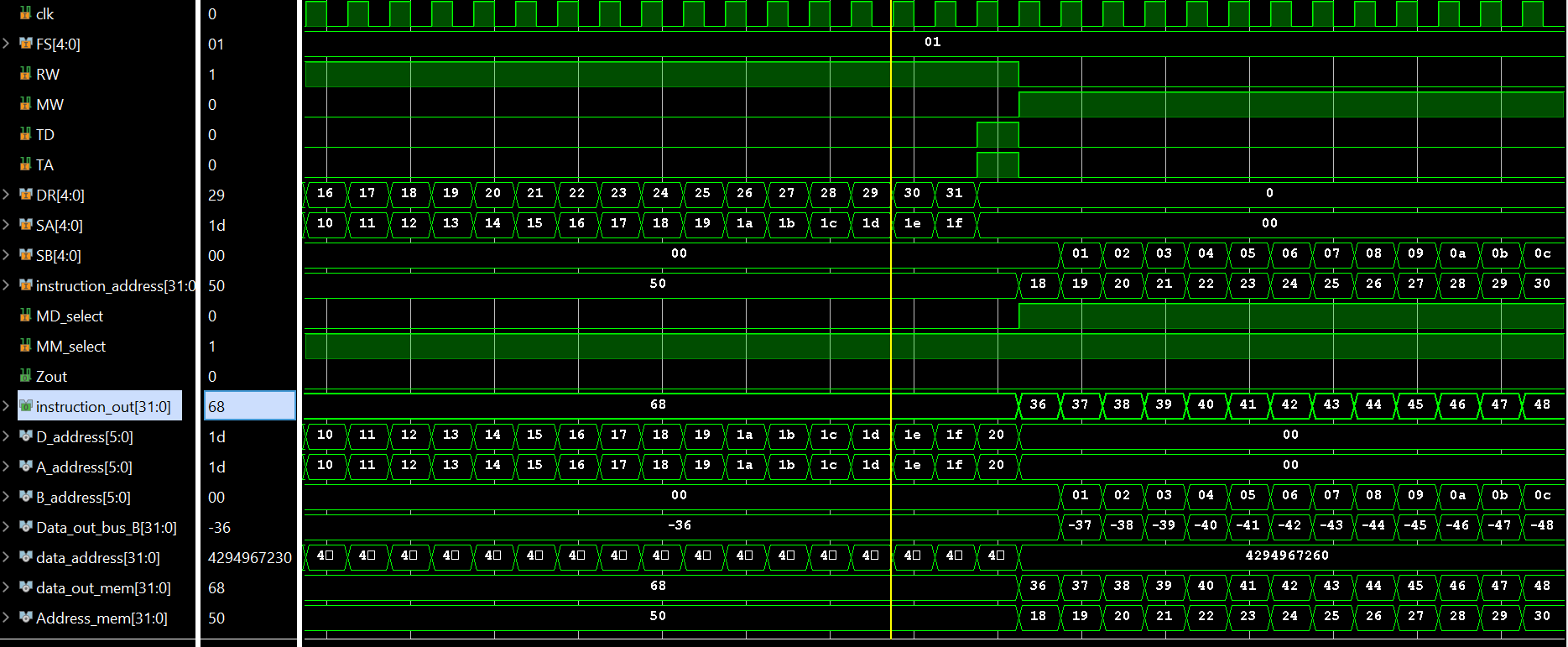
Microprocessor without control memory 2’s complement of data mem



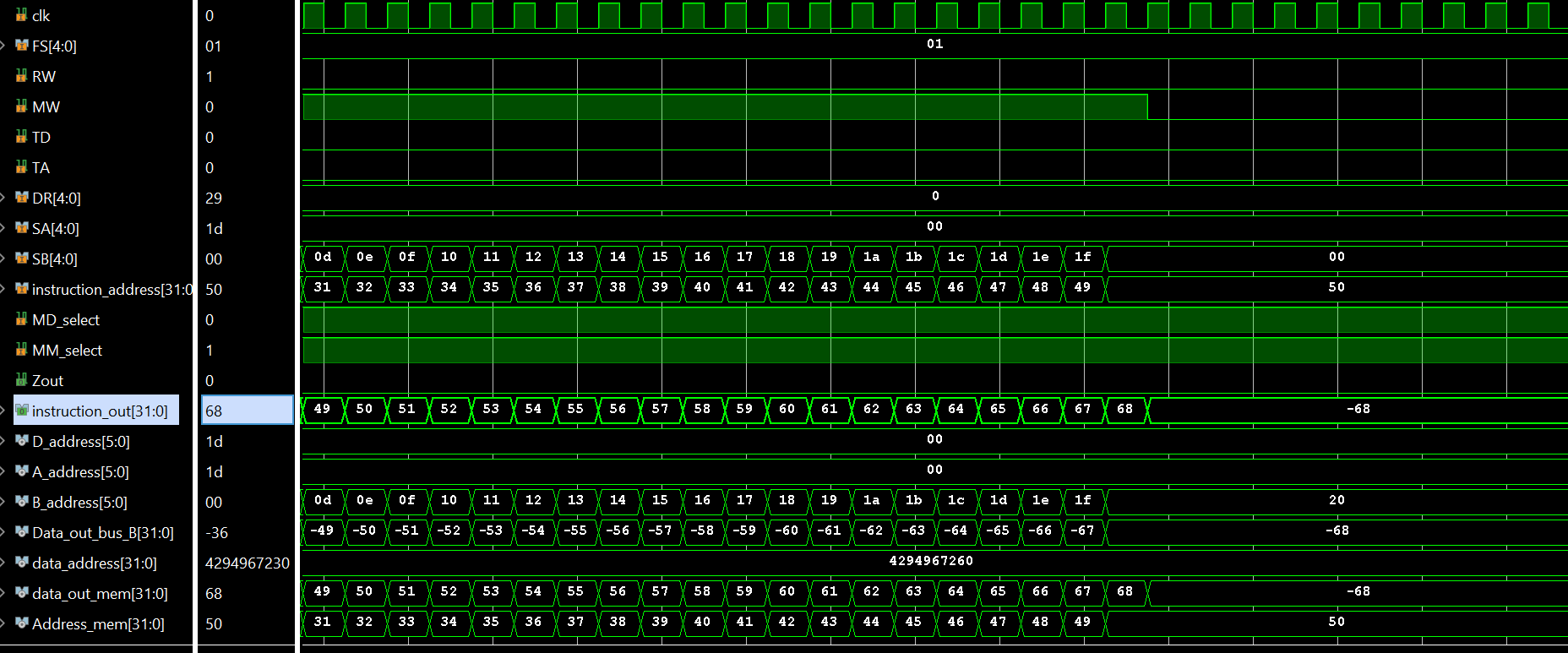
Further in time



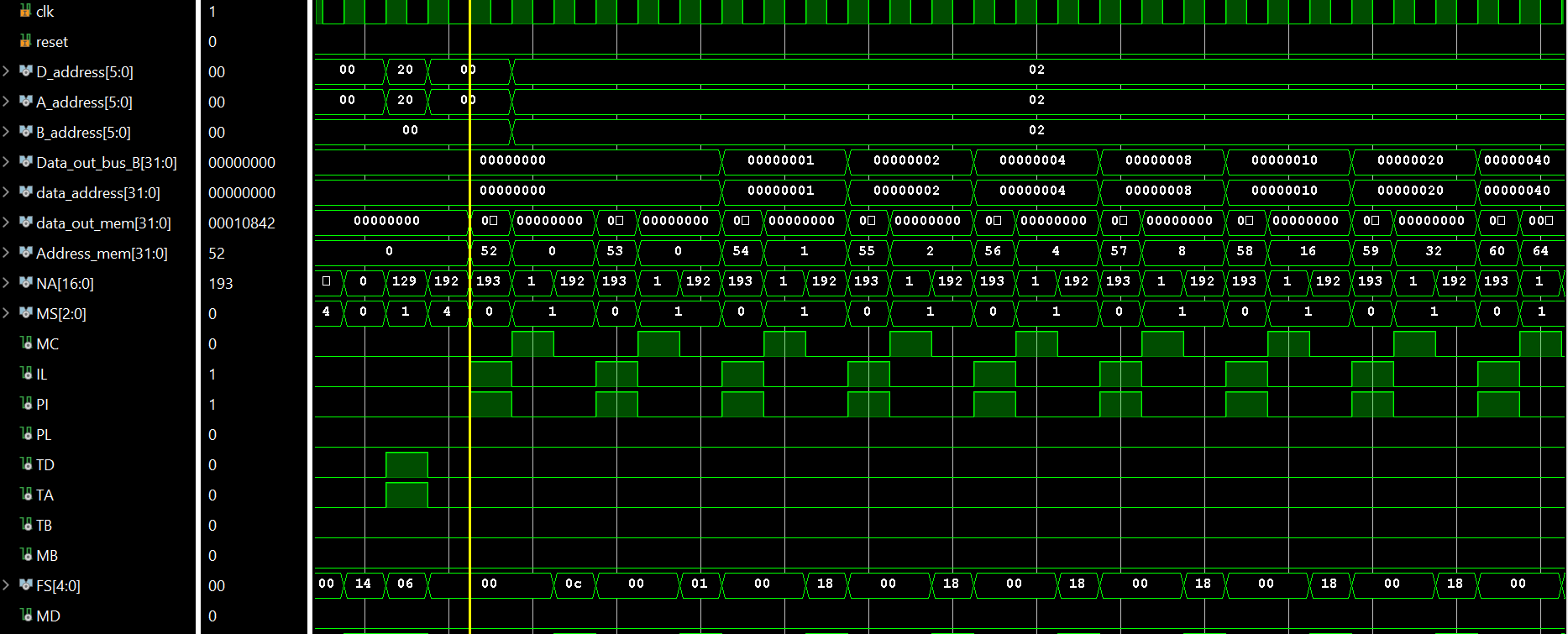
Further in time

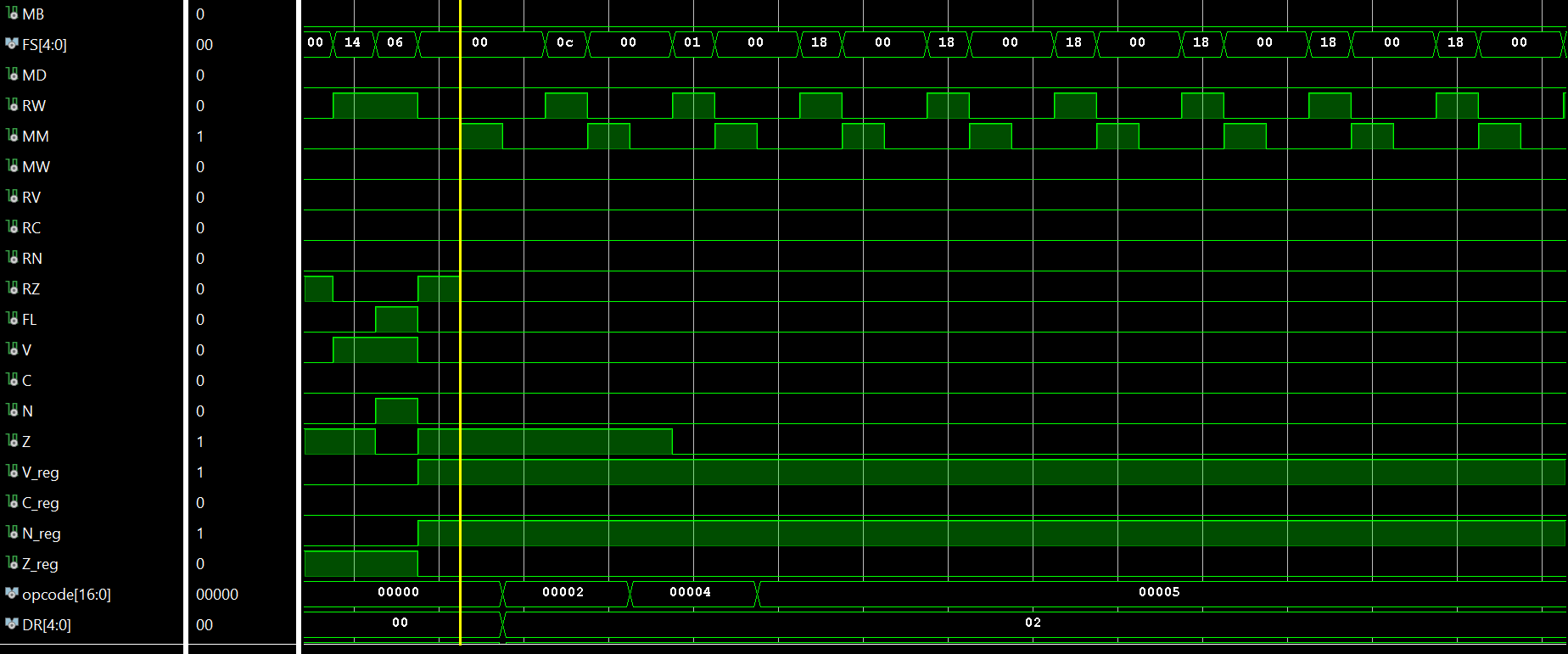


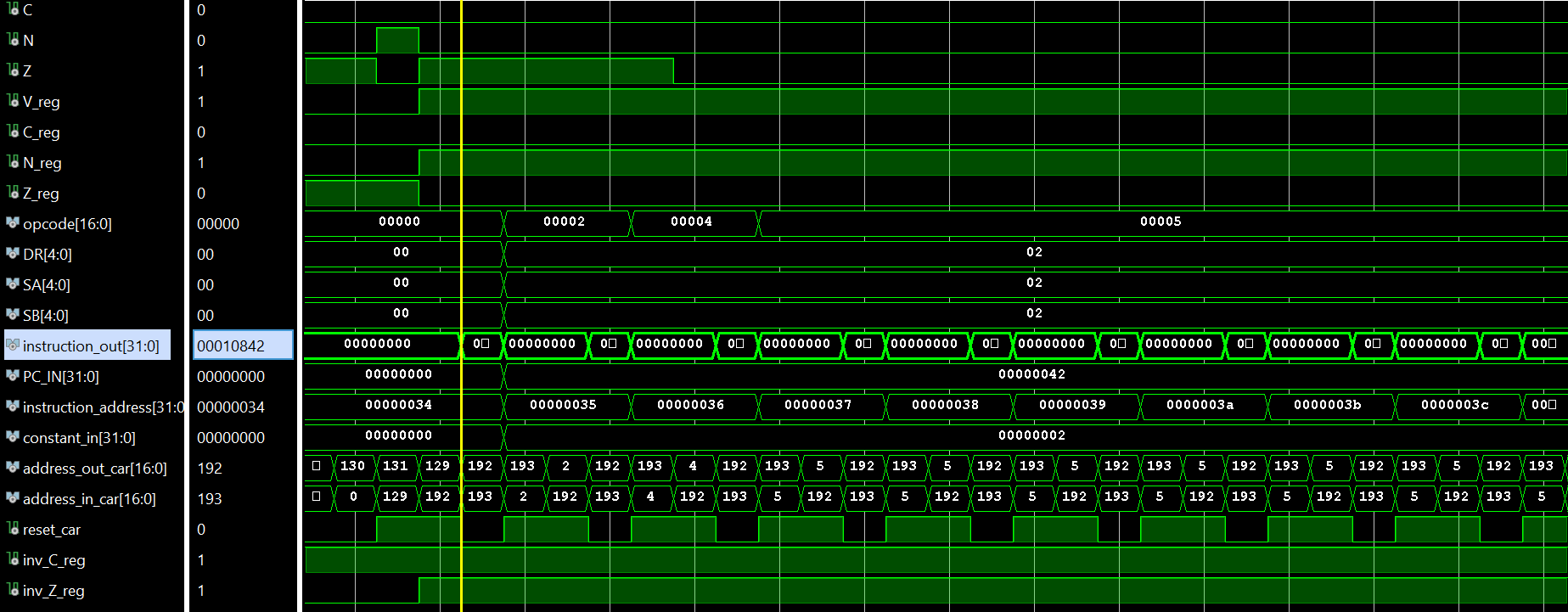
Further in time



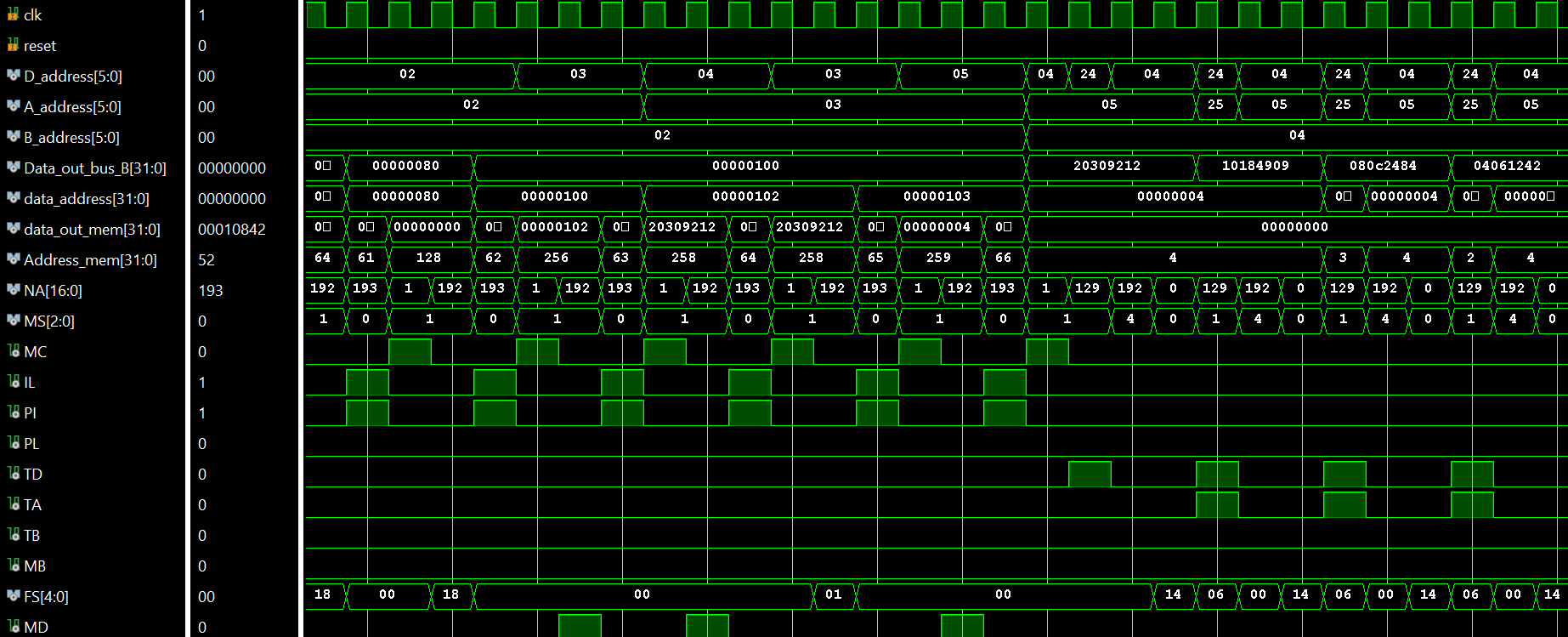
Microcode simulation, with control and main memory

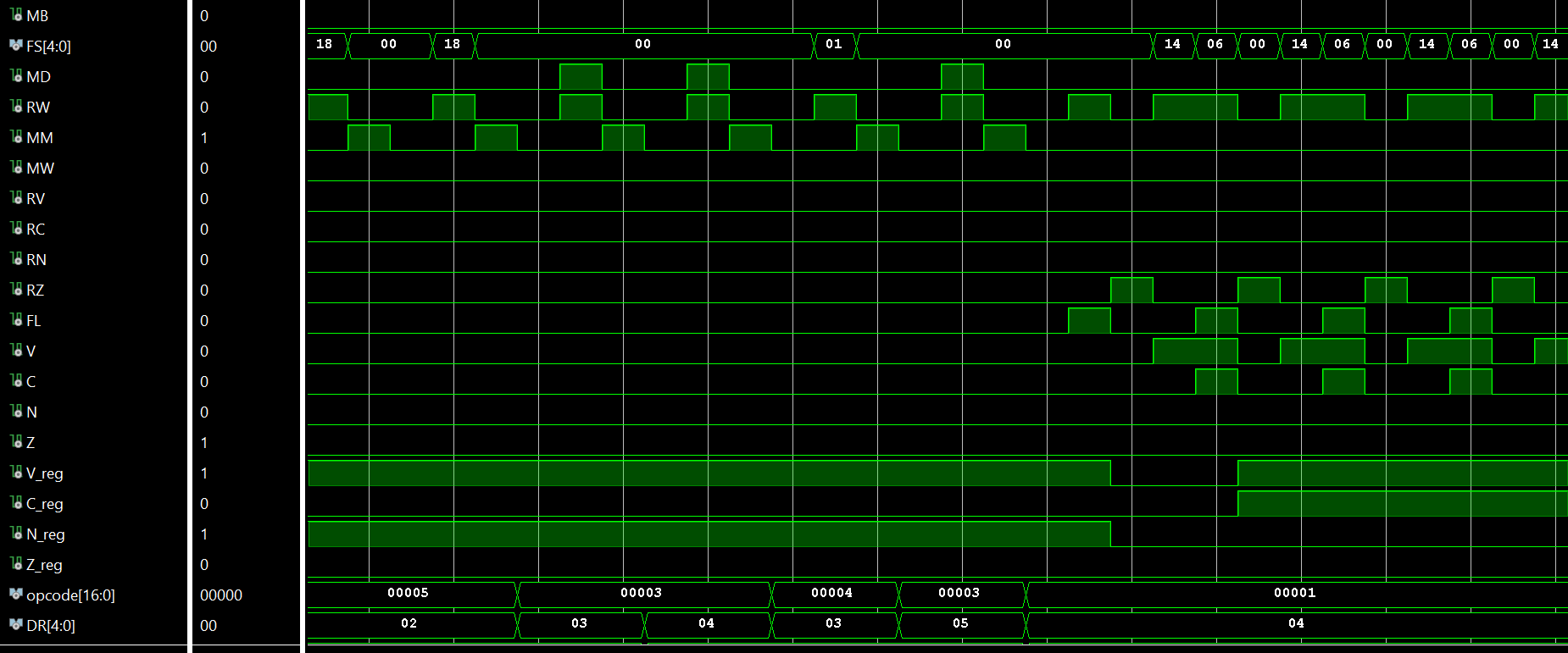


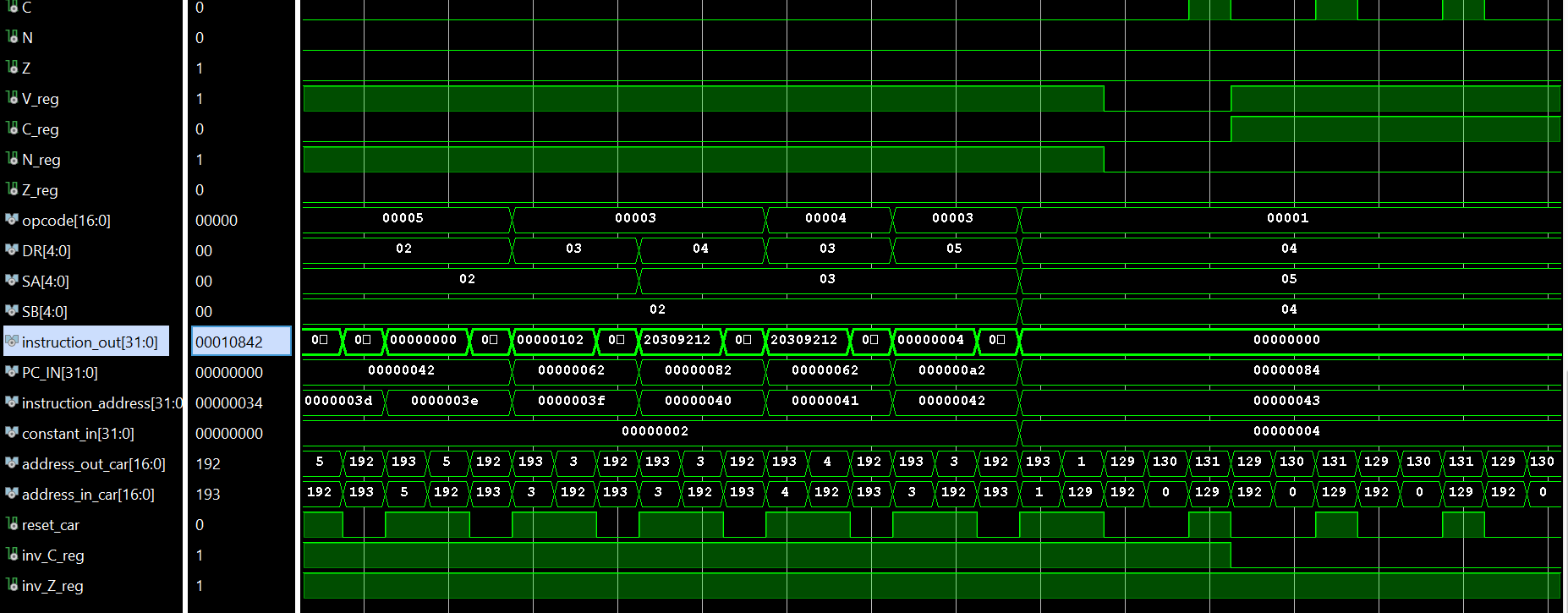




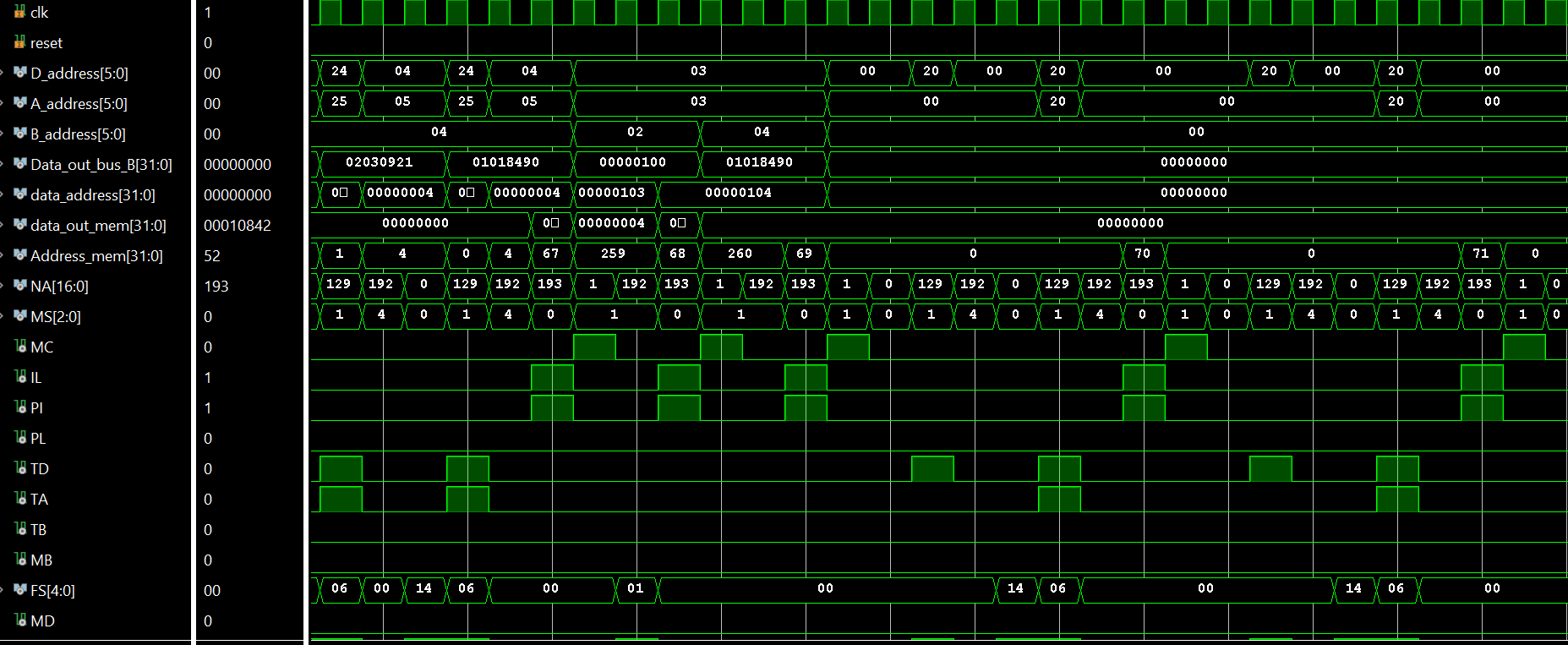
Further time

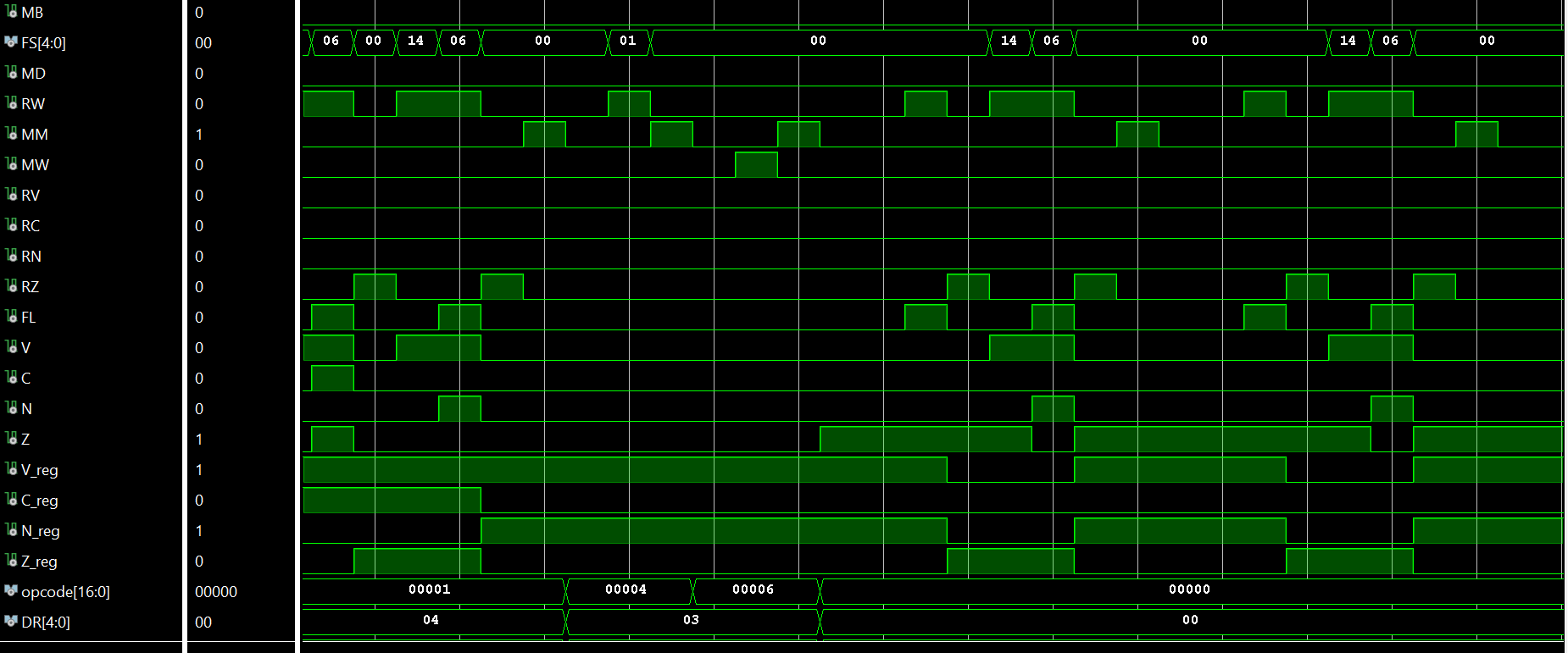


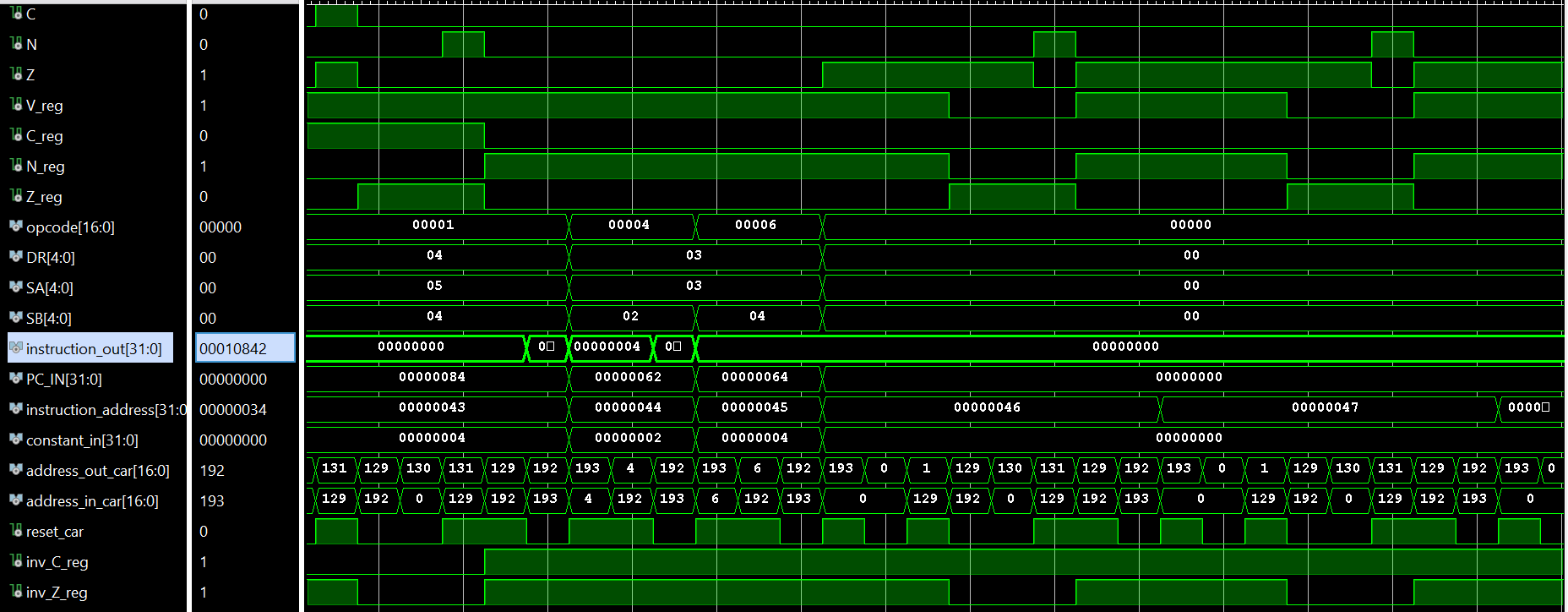




Further time







Carry look ahead adder

