MP2662

500mA Single Cell Li-ion Battery Charger with Power Path Management, 1mA Termination and <1µA Battery Leakage

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP2662 is a highly-integrated single-cell Li-Ion/Li-Polymer battery charger with system power path management, targeted at space limited portable applications. This device takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The charger section features pre-charge (PRE.C), fast current (CC) and constant voltage (CV) regulation, charge termination and auto-recharge.

The power path management function ensures continuous power to the system by automatically selecting the input, the battery or both to power the system. This section features a low drop-out regulator from input to system, and a 100mΩ switch from battery to system. Power path management separates charging current from system load, which allows proper charge termination and keeps the battery in full charge mode.

The MP2662 provides system short circuit protection function by limiting the current from input to system and battery to system. This feature is especially critical to prevent the Li-Ion battery from being damaged due to excessive high current. An on-chip battery UVLO will cut off the path between battery and system if battery voltage drops below a programmable battery UVLO threshold, which prevents the Li-Ion battery from being over discharged. An integrated I^2C control interface allows the MP2662 to program the charging parameters, such as: input current limit, input voltage regulation limit, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2662 is available in 9 pin 1.75mmx1.75mm WCSP package.

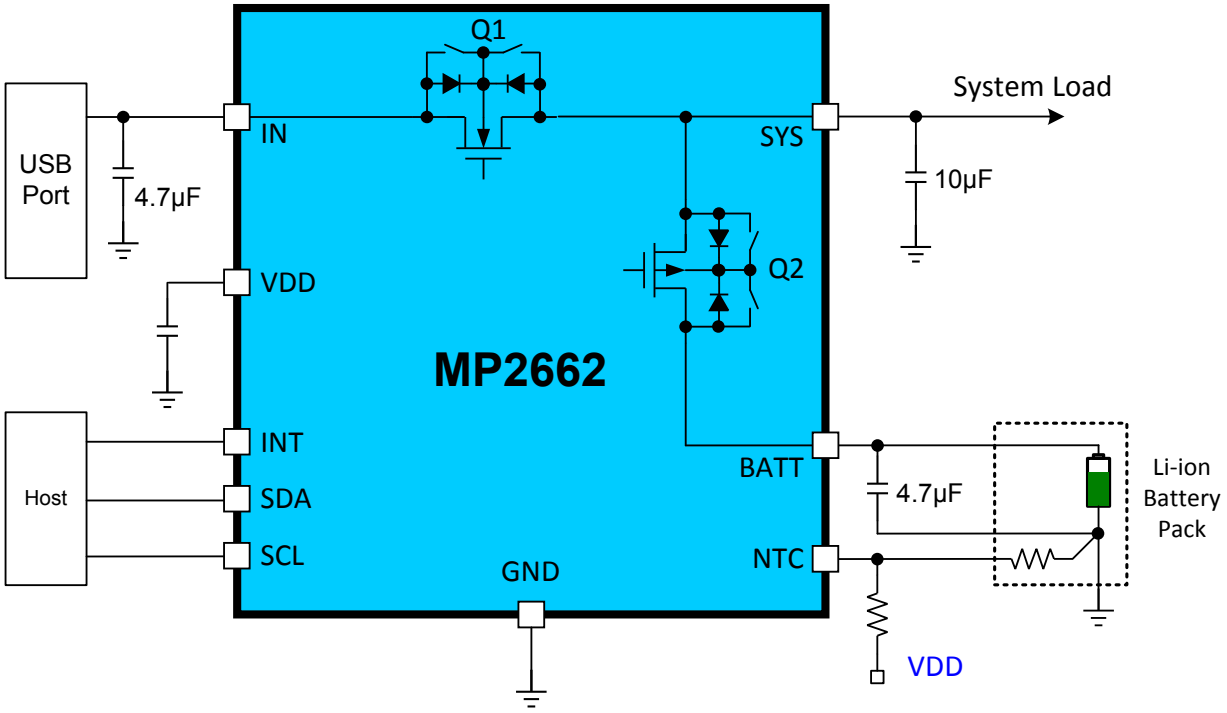
FEATURES

- Fully Autonomous Charger for Single-Cell Li-Ion/Polymer Batteries
- 21V Maximum Input Voltage Rating with Over-Voltage Protection
- ±0.5% Charging Voltage Accuracy
- I^2C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-in Robust Charging Protection Including Battery Temperature Monitor and Programmable Timer
- PCB Over Temperature Protection (PCB_OTP)
- System Reset Function
- Built-in Battery Disconnection Function
- Thermal Limiting Regulation on Chip
- Tiny WCSP1.75mmx1.75mm Package

APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smart Watches

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2662GC-xxxx**	WLCSP-9 (1.75mmx1.75mm)	*See Below*
EVKT-MP2662	Evaluation Kit	

*For Tape & Reel, add suffix –Z (e.g. MP2662GC-xxxx–Z)
**"xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Please contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

JAY
LLL

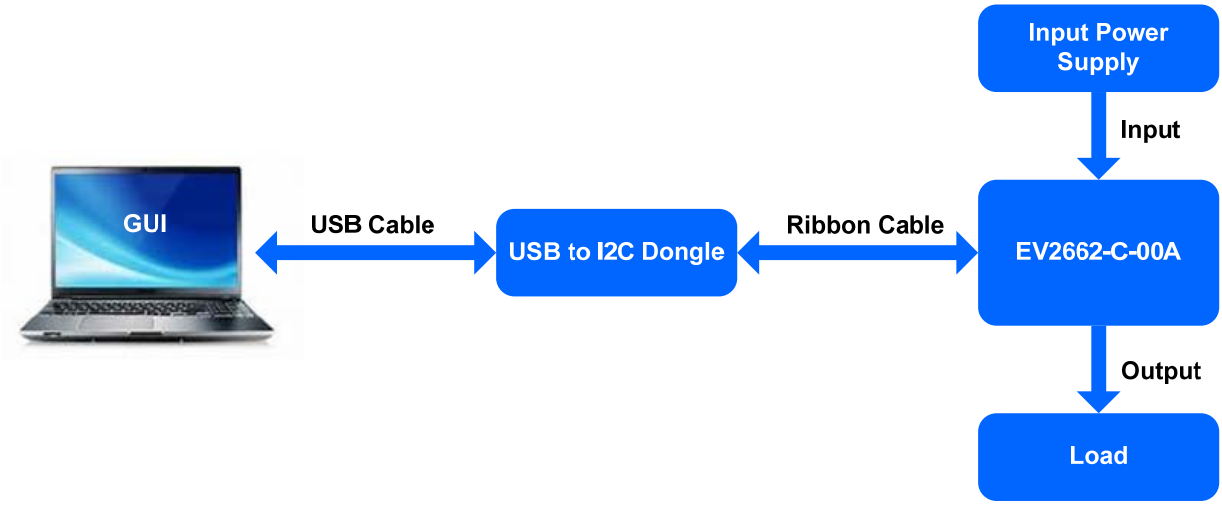
JA: Product code of MP2662GC
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP2662

EVKT-MP2662 Kit contents: (Items below can be ordered separately)

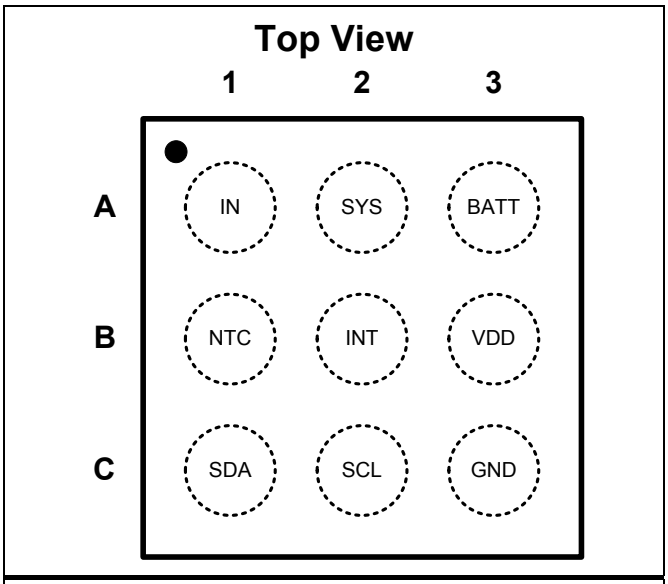
#	Part Number	Item	Quantity
1	EV2662-C-00A	MP2662 Evaluation Board	1
2	EVKT-USBI2C-02-Bag	Includes one USB to I2C dongle, one USB cable and one ribbon cable	1
3	Online resources	Includes datasheet, user guide, product brief and GUI	1

Order direct from MonolithicPower.com or our distributors.



EVKT-MP2662 Evaluation Kit Set-Up

PACKAGE REFERENCE



WLCSP-9 (1.75mmx1.75mm)

PIN FUNCTIONS

Package Pin #	Name	I/O	Description
A1	IN	Power	Input Power Pin. Place a ceramic capacitor from IN to PGND as close as possible to IC.
A2	SYS	Power	System power supply. Place a ceramic capacitor from SYS to PGND as close as possible to IC.
A3	BATT	Power	Battery Pin. Place a ceramic capacitor from BATT to PGND as close as possible to IC.
B1	NTC	I	Temperature Sense Input. Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VDD to NTC to GND. Charge suspends when either NTC pin is out of range.
B2	INT	O	Interrupt output. The INT pin can send charging status and fault interrupt to the host. This pin is also used to disconnect the system from the battery, pull this pin from high to low for >16s, the battery FET is off and it will turn on automatically after >4s whatever the INT state is.
B3	VDD	I	Internal control power supply pin. Connect a 1μF ceramic cap from this pin to GND. No external load is allowed.
C1	SDA	I/O	I²C Interface data. Connect SDA to the logic rail through a 10kOhm resistor.
C2	SCL	I/O	I²C Interface clock. Connect SCL to the logic rail through a 10kOhm resistor.
C3	GND	Power	Ground

ABSOLUTE MAXIMUM RATINGS (1)

IN ..... -0.3V to +21V
SYS ..... -0.3V to +5.3V (5.5V for 500µs)
All Other Pins to GND ..... -0.3V to +6V
Continuous Power Dissipation (T_A=+25°C)(2) 0.88W
Junction Temperature ..... 150°C
Lead Temperature (Solder) ..... 260°C
Storage Temperature…. ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage (VIN)…….4.35V to 5.5V (USB Input)
I_{IN} ..... Up to 500mA
I_{BATT} ..... Up to 3.2A(5)
I_{CHG} ..... Up to 456mA
V_{BATT_REG} ..... Up to 4.545V
Operating Junct. Temp. (T_J) ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

WLCSP-9 (1.75mmx1.75mm) 114 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Guaranteed by design.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT}=3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input Under-voltage Lock-out Threshold	V_{IN_UVLO}	Input falling	3.63	3.73	3.83	V
Input Under-voltage Lock-out Threshold Hysteresis		Input rising		170		mV
Input Over-voltage Protection Threshold	V_{IN_OVP}	Input rising threshold	5.85	6	6.15	V
Input Over-voltage Protection Threshold Hysteresis				350		mV
Input vs. Battery Voltage Headroom Threshold	V_{HDRM}	Input rising vs. battery	80	130	170	mV
Input vs. Battery Voltage Headroom Threshold Hysteresis				90		mV
BATT Input Voltage(5)	V_{BATT}				4.5	V
Battery Under-voltage Lockout Threshold	V_{BATT_UVLO}	BATT voltage falling, REG01[2:0]=000	2.3	2.4	2.5	V
		BATT voltage falling, REG01[2:0]=100	2.66	2.76	2.86	
		BATT voltage falling, REG01[2:0]=111	2.93	3.03	3.13	
BATT Under Voltage Threshold Hysteresis		V_{BATT_UVLO}=2.76V		190		mV
Battery Over-voltage Protection Threshold	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		130		mV
Battery Over-voltage Protection Hysteresis				60		
Power Path Management						
Regulated System Output Voltage Accuracy	$V_{SYS\_REG\_ACC}$	V_{IN} =5.5V, R_{SYS}=100Ω, I_{CHG}=0A, REG07[3:0]=0000, V_{SYS_REG}=4.2V	-2		2	%
		V_{IN} =5.5V, R_{SYS}=100Ω, I_{CHG}=0A, REG07[3:0]=1001, V_{SYS_REG}=4.65V	-2		2	%
		V_{IN} =5.5V, R_{SYS}=100Ω, I_{CHG}=0A, REG07[3:0]=1111, V_{SYS_REG}=4.95V	-2		2	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT}=3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Current Limit	I_{IN_LIM}	REG00[3:0]=0000,I_{IN_LIM}=50mA	30	40	50	mA
		REG00[3:0]=0011,I_{IN_LIM}=140mA	112	126	140	
		REG00[3:0]=1001,I_{IN_LIM}=320mA	275	300	325	
		REG00[3:0]=1111,I_{IN_LIM}=500mA	440	470	500	
Input Minimum Voltage Regulation	V_{IN_MIN}	REG00[7:4]=0000, V_{IN_REG} =3.88V	3.68	3.88	4.18	V
		REG00[7:4]=1001, V_{IN_REG} =4.60V	4.40	4.60	4.75	
		REG00[7:4]=1111, V_{IN_REG} =5.08V	4.88	5.08	5.35	
IN to SYS Switch On Resistance	R_{ON_Q1}	V_{IN}=4.5V, I_{SYS}=100mA		290		mΩ
Input Quiescent Current	I_{IN_Q}	V_{IN}=5.5V, EN_HIZ=0, CE=L, Charge enable, I_{CHG} = 0A, I_{SYS} = 0A		1.9		mA
		V_{IN}=5.5V, EN_HIZ=0, CE=H, Charge disabled		1.7		
Battery Quiescent Current	I_{BATT_Q}	V_{IN}=5V, CE=L, I_{SYS}=0A, charge done, V_{BATT}=4.35V		43		μA
		V_{IN}=GND, CE=H, I_{SYS} = 0A, V_{BATT}=4.35V, disable PCB_OTP function, not include the current from external NTC resistor		6.5	7.5	
		V_{IN}=GND, CE=H, I_{SYS} = 0A, V_{BATT}=4.35V, enable PCB_OTP function, not include the current from external NTC resistor		14.5	21	
		V_{IN}=GND, CE=H, I_{SYS} = 0A, V_{BATT}=4.35V, enable PCB_OTP function, not include the current from external NTC resistor, enable watchdog		22.5		
		V_{BATT}=4.5V, V_{IN}=V_{SYS}=GND, FET_DIS=1, shipping mode			350	nA
BFET On Resistance	R_{ON_Q2}	V_{IN} < 2V, V_{BATT}=3.5V, I_{SYS}=100mA		100		mΩ
BFET Discharge Current Limit	I_{DSCHG}	REG03[7:4]=0001, I_{DSCHG}=400mA	370	490	585	mA
		REG03[7:4]=1001, I_{DSCHG}=2000mA		2400(5)		
SYS Reverse to BATT Switch Leakage		V_{SYS}=4.65V, V_{IN}=5V, V_{BATT}=GND, EN_HIZ=1, CE=H, Charge disabled			100	nA
Ideal Diode Forward Voltage in Supplement Mode	V_{FWD}	50mA discharge current		30		mV
Shipping mode						
Enter Shipping Mode Deglitch Time	t_{SMEN_DGL}	REG06[5] is set from 0 to 1; REG09[7:6]=00		1		s

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT}=3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Exit Shipping Mode by INT or V_{IN} Plug In	t_{SMEX_DGL}	INT is pulled low		2		s
Auto-Reset Mode						
Reset by INT	t_{RST_DGL}	REG01H[7:6] = 00		8		s
		REG01H[7:6] = 10		16		
BFET Off Lasting Time	t_{RST_DUR}	REG01H[5] = 0		2		s
		REG01H[5] = 1		4		
Battery Charger						
Battery Charge Voltage Regulation	V_{BATT_REG}	REG04[7:2] = 000000, V_{BATT_REG} = 3.6V	3.582	3.6	3.618	V
		REG04[7:2] = 101000, V_{BATT_REG} = 4.2V	4.179	4.2	4.221	
		REG04[7:2] = 110010, V_{BATT_REG} = 4.38V	4.358	4.38	4.4	
		REG04[7:2] = 111110, V_{BATT_REG} = 4.53V	4.522	4.53	4.568	
Fast Charge Current	I_{CC}	REG02[5:0]=000000, I_{CC}=8mA	6.9	8	8.5	mA
		REG02[5:0]=001011, I_{CC}=96mA	89	96	103	
		REG02[5:0]=100000, I_{CC}=264mA	251	264	285	
		REG02[5:0]=111000, I_{CC}=456mA	420	456	484	
Junction Temperature Regulation(5)	T_{J_REG}	Thermal_Limit=120ºC		120		ºC
Pre-charge Current	I_{PRE}	I_{PRE} = I_{TERM}	1		31	mA
Charge Termination Current Threshold	I_{TERM}	REG03[3:0]=0000, I_{TERM}=1mA	0.8	0.93	1.05	mA
		REG03[3:0]=0001, I_{TERM}=3mA	2.7	3	3.3	
		REG03[3:0]=0101, I_{TERM}=11mA	10	11	12	
		REG03[3:0]=0101, I_{TERM}=31mA	28	31	34	
Termination Deglitch Time	t_{TERM_DGL}			3.2		s
Pre-charge to Fast Charge Threshold	V_{BATT_PRE}	V_{BATT} Rising, REG04[1]=1, V_{BATT_PRE}=3.0V	2.9	3.0	3.1	V
Pre-charge to Fast Charge Threshold Hysteresis				90		mV
Battery Auto-recharge Voltage Threshold	V_{RECH}	Below V_{BATT_REG}, REG04[0] = 0	60	100	140	mV
		Below V_{BATT_REG}, REG04[0] = 1	160	200	240	
Battery Auto-recharge Deglitch Time	t_{RECH_DGL}			200		ms
Thermal Protection						
Thermal Shutdown Threshold(5)	T_{J_SHDN}			150		ºC

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

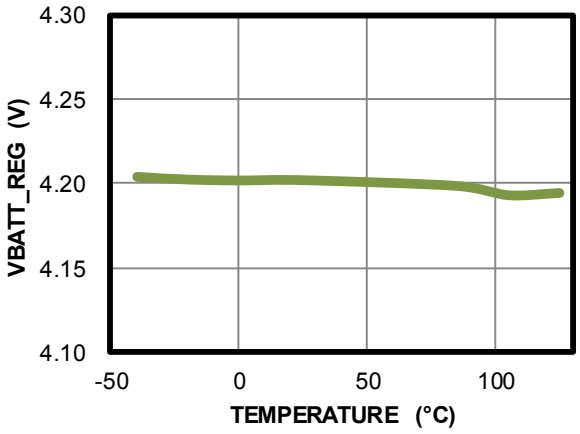
Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Shutdown Hysteresis(5)				20		ºC
NTC pin Output Current	I_{NTC}	CE = L, NTC = 3V	-1	0	1	µA
NTC Cold Temp Rising Threshold	V_{COLD}	As percentage of V_{DD}	63	65	67	%
NTC Cold Temp Rising Threshold Hysteresis				60		mV
NTC Hot Temp Falling Threshold	V_{HOT}	As percentage of V_{DD}	31	33	35	%
NTC Hot Temp Falling Threshold Hysteresis				70		mV
NTC Hot Temp Falling Threshold for PCB_OTP	V_{HOT_PCB}	As percentage of V_{DD}	30	32	35	%
NTC Hot Temp Falling Threshold Hysteresis for PCB_OTP				90		mV
Logic IO Pin Characteristics						
Low Logic Voltage Threshold	V_L				0.4	V
High Logic Voltage Threshold	V_H		1.3			V
I²C Interface(SDA, SCL)						
Input High Threshold Level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input Low Threshold Level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output Low Threshold Level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C Clock Frequency	F_{SCL}				400	kHz
Clock Frequency and Watchdog Timer						
Clock Frequency	F_{CLK}			131		kHz
Watchdog Timer	t_{WDT}	REG05[6:5] = 11		160		s

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM}=500mA, I_{CC}=128mA, V_{IN_MIN}=4.6V, unless otherwise noted.

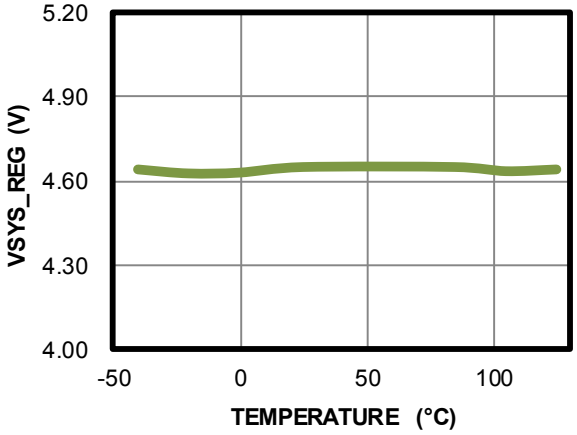
Battery Regulation Voltage vs. Temperature

V_{BATT_REG}=4.2V

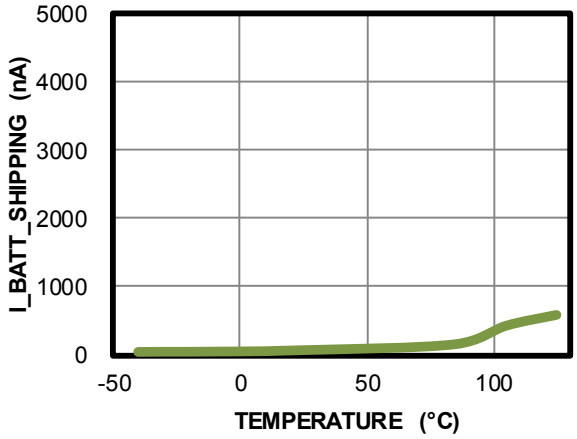


System Regulation Voltage vs. Temperature

V_{SYS_REG}=4.65V

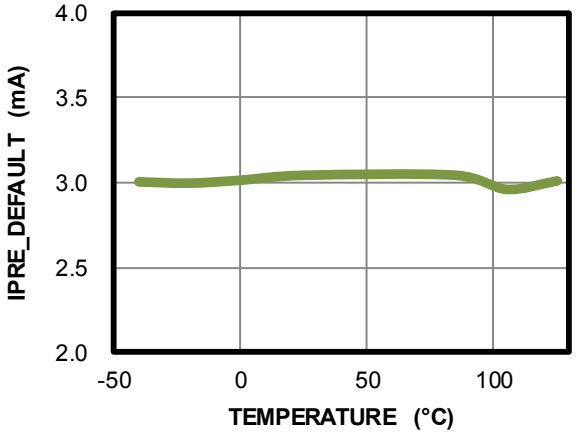


Battery Current under Shipping mode vs. Temperature



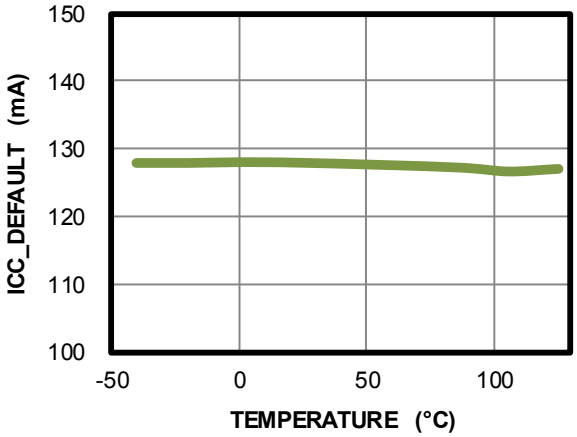
Pre-Charge Current vs. Temperature

I_{PRE}=3mA



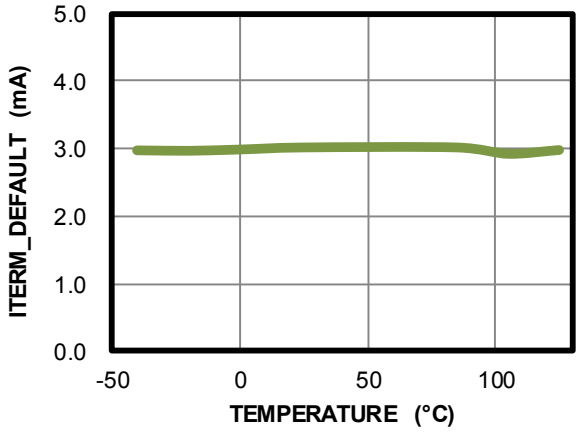
Fast Charge Current vs. Temperature

I_{CC}=128mA



Battery Termination Current vs. Temperature

I_{TERM}=3mA

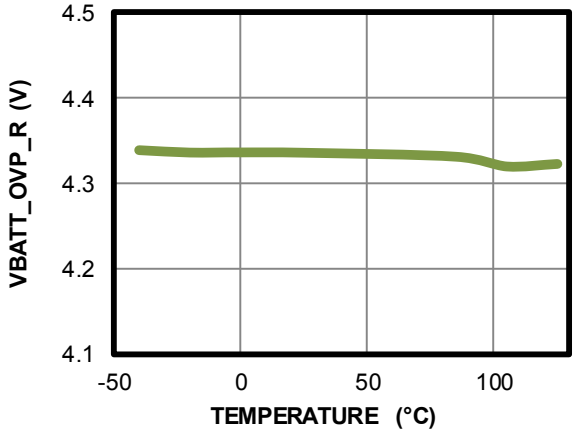


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM}=500mA, I_{CC}=128mA, V_{IN_MIN}=4.6V, unless otherwise noted.

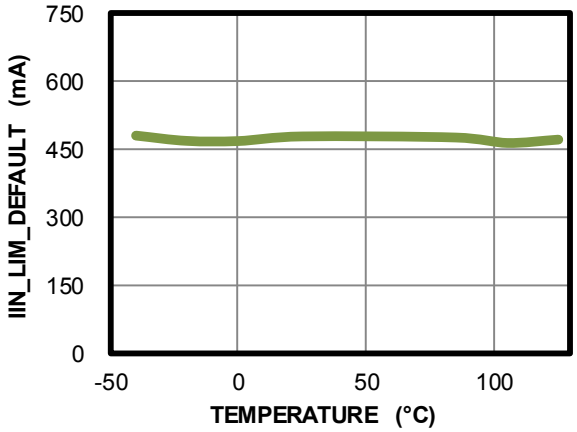
Battery OVP Voltage vs. Temperature

V_{BATT_REG}=4.2V



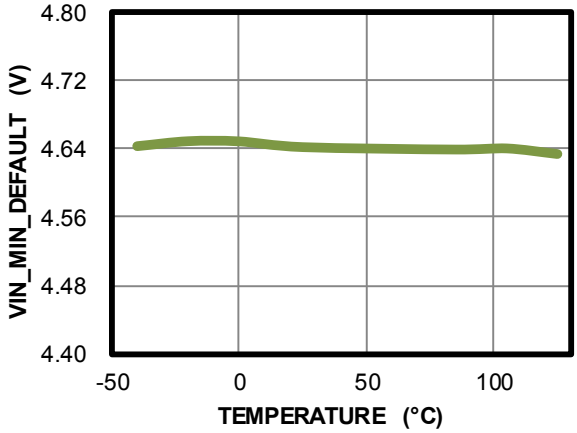
Input Current Limit vs. Temperature

I_{IN_LIM}=500mA



Input Minimum Voltage vs. Temperature

V_{IN_MIN}=4.60V

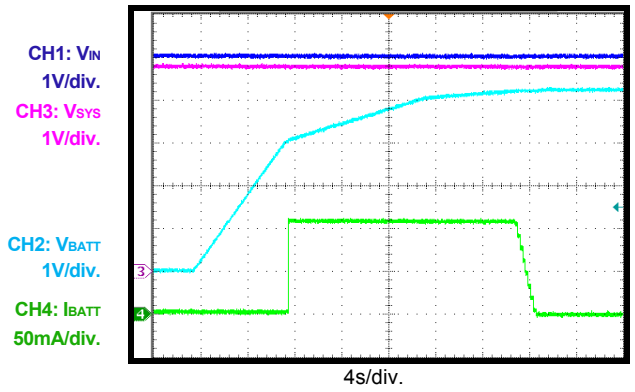


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM}=500mA, I_{CC}=128mA, V_{IN_MIN}=4.6V, unless otherwise noted.

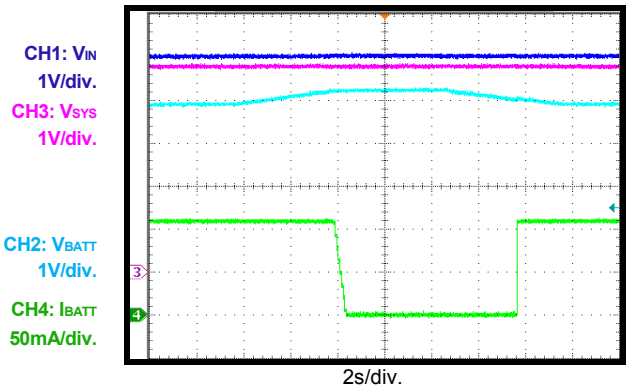
Battery Charge Curve

I_{SYS}=0A



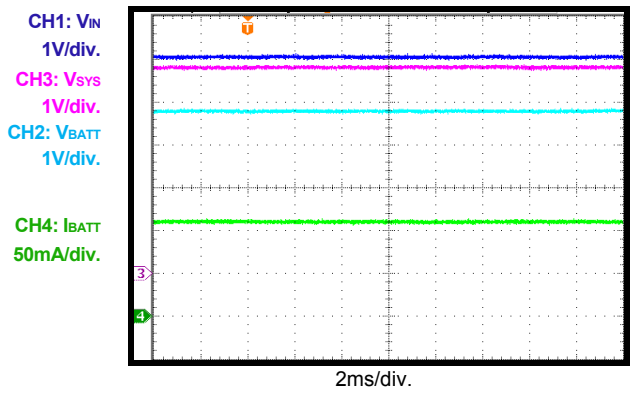
Auto Recharge

I_{SYS}=0A



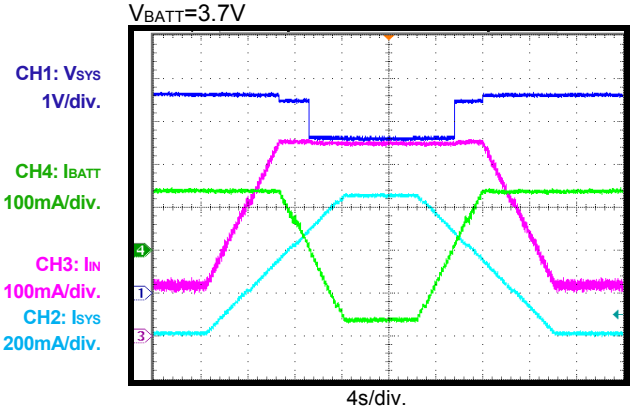
CC Charge Steady State

V_{BATT}=3.7V, I_{SYS}=0A



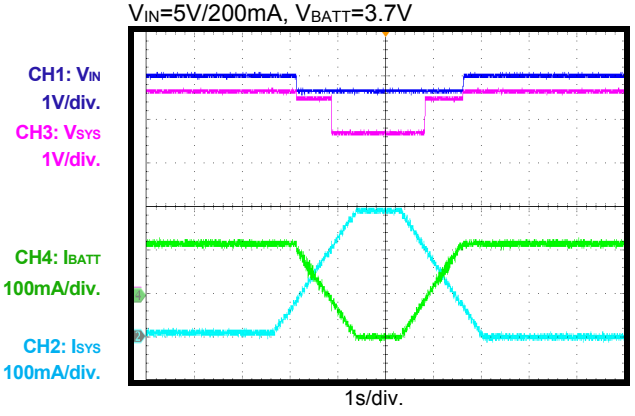
Input Current Limit based PPM

V_{BATT}=3.7V



Input Voltage Regulation based PPM

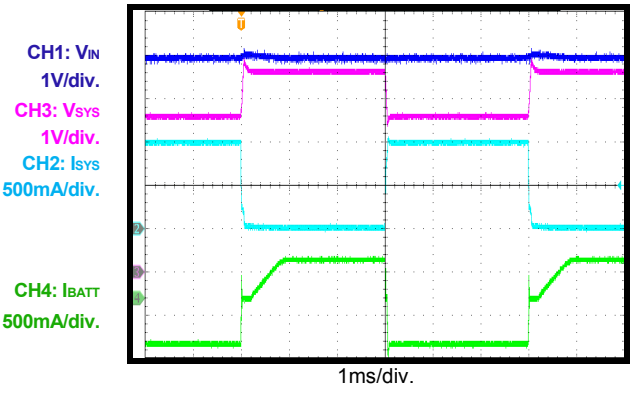
V_{IN}=5V/200mA, V_{BATT}=3.7V



SYS Load Transient

V_{IN}=5V, V_{BATT}=3.7V, I_{CC}=456mA

I_{SYS}=0A-1A

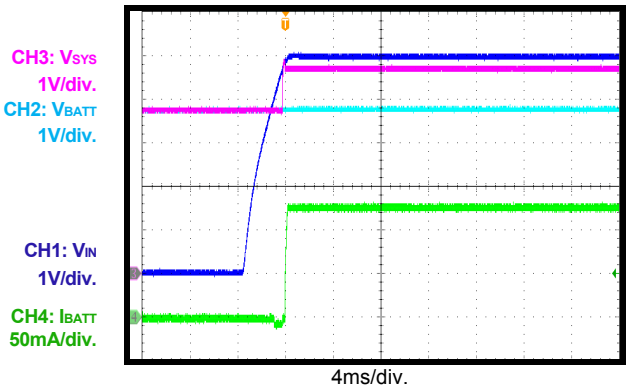


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM}=500mA, I_{CC}=128mA, V_{IN_MIN}=4.6V, unless otherwise noted.

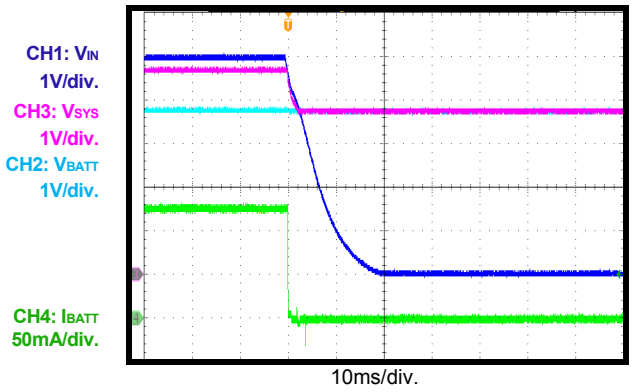
Power On

V_{BATT}=3.7V, I_{SYS}=0A



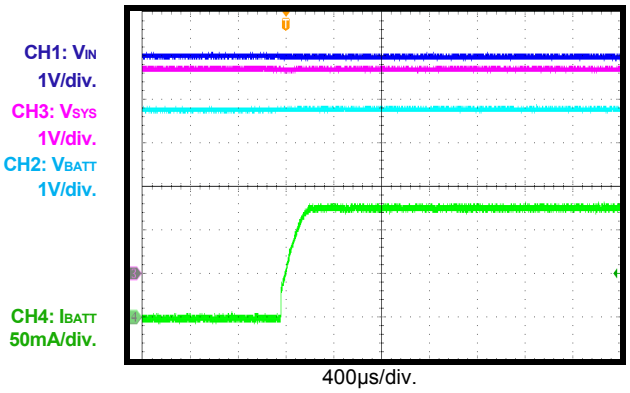
Power Off

V_{BATT}=3.7V, I_{SYS}=0A



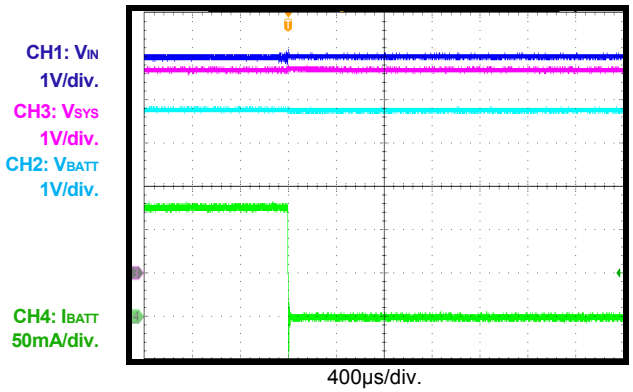
Charge Enable

V_{BATT}=3.7V, I_{SYS}=0A



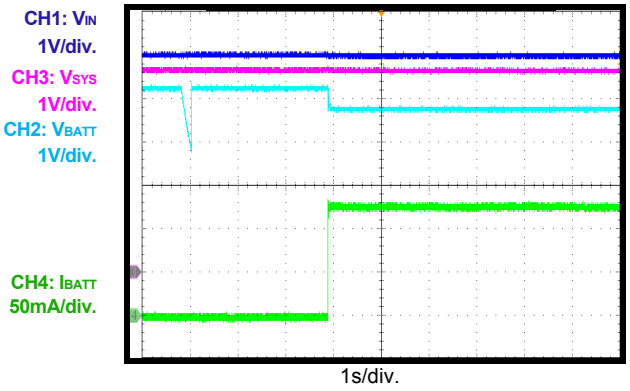
Charge Disable

V_{BATT}=3.7V, I_{SYS}=0A



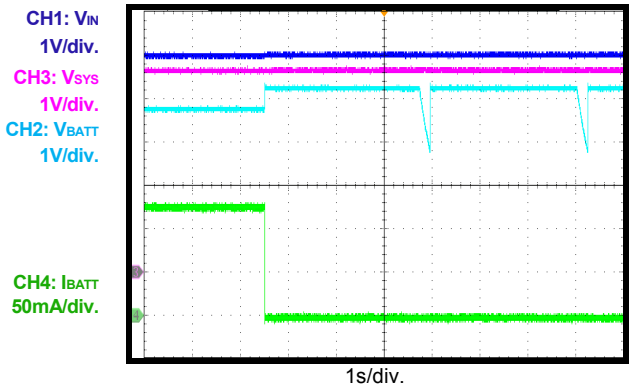
BATT Insertion

V_{BATT}=3.7V, I_{SYS}=0A



BATT Removal

V_{BATT}=3.7V, I_{SYS}=0A

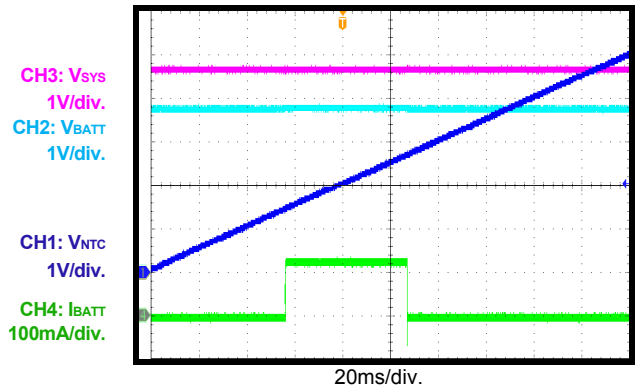


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM}=500mA, I_{CC}=128mA, V_{IN_MIN}=4.6V, unless otherwise noted.

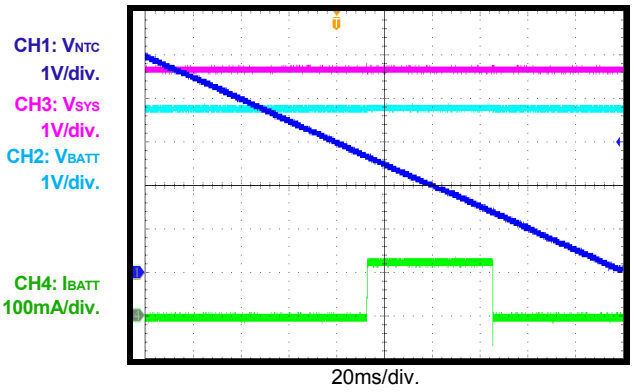
NTC Rising

V_{BATT}=3.7V, I_{SYS}=0A, PCB_OTP Disable



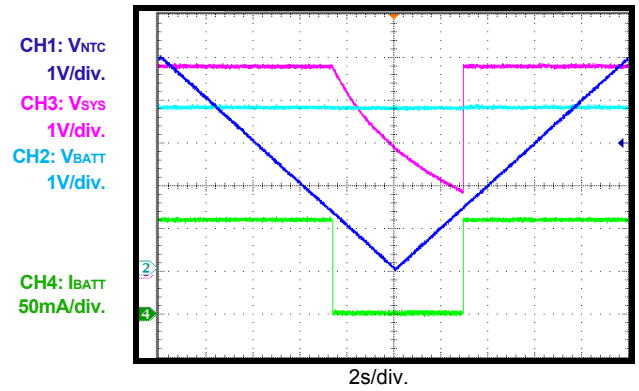
NTC Falling

V_{BATT}=3.7V, I_{SYS}=0A, PCB_OTP Disable



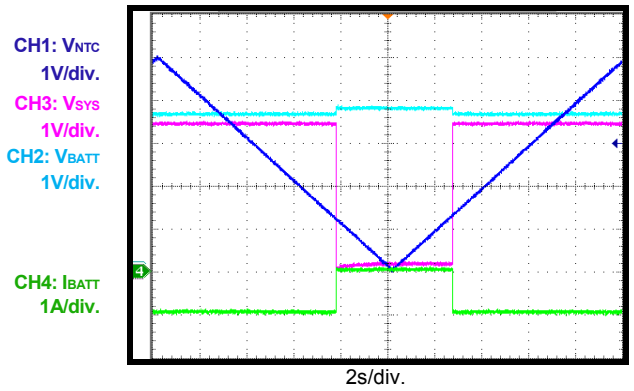
PCB_OTP @ Charge Mode

V_{BATT}=3.7V, I_{SYS}=0A



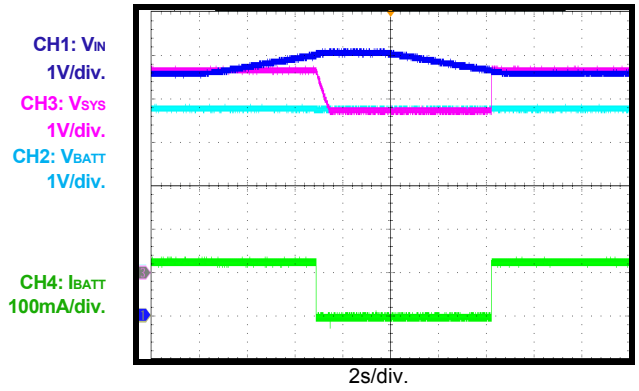
PCB_OTP @ Discharge Mode

V_{IN}=0V, V_{BATT}=3.7V, I_{SYS}=1A



Vin OVP Operation

V_{BATT}=3.7V, I_{SYS}=0A



FUNCTION BLOCK DIAGRAM

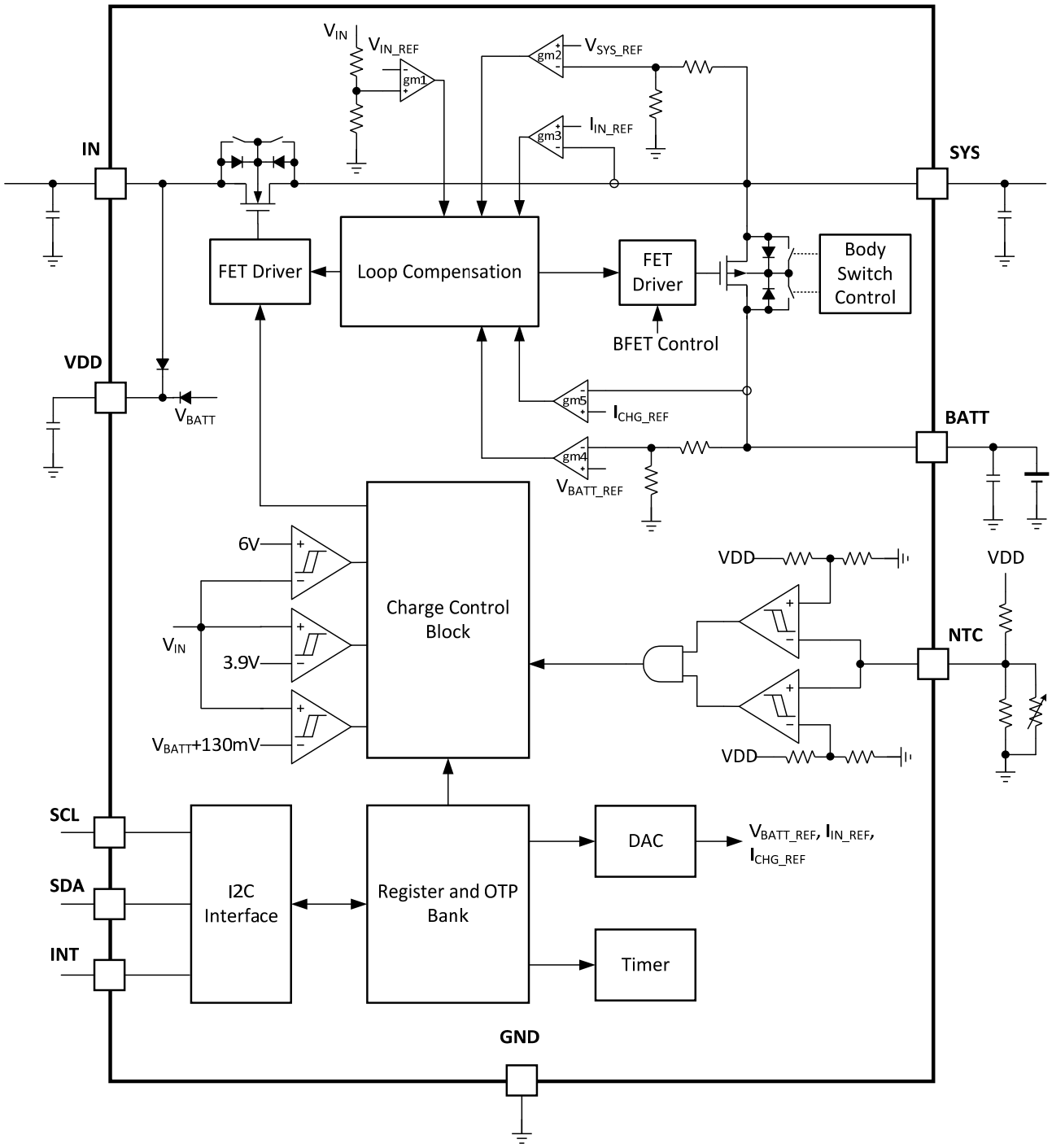


Figure 1: Functional Block Diagram

OPERATION

Introduction

MP2662 is an I²C controlled single-cell Li-ion or Li-polymer battery charger with complete power path management function. The full charge function features constant current pre-charge, constant current fast charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. The system load requirement always has priority to charge current, when the input power is limited due to input current limit or input voltage limit, the IC will automatically reduce charge current until the battery supplement the system load.

The IC integrates a 200mΩ LDO FET between IN and SYS, and a 100mΩ battery FET between SYS and BATT pin.

In charging mode, the on-chip 100mΩ battery FET works as a full-featured linear charger with pre charge, fast charge and constant voltage charge, charge termination, auto recharge, NTC monitor, built-in timer control, and thermal protection. The charge current can be programmed via I²C interface. The IC adjusts the charge current when the die temperature exceeds the thermal regulation threshold (default at 120°C).

In supplement mode, the 100mΩ battery FET is turned on to connect the battery to the system load when the input power is not enough to power the system load. When the input is removed, the 100mΩ battery FET is also fully turned on allowing the battery to power up the system.

The system load is satisfied in priority then the remaining current is used to charge the smart power path management battery. The IC will reduce charging current or even use power from the battery to satisfy the system load when its demand is over the input power capacity.

Figure 2 shows the power path management structure for MP2662.

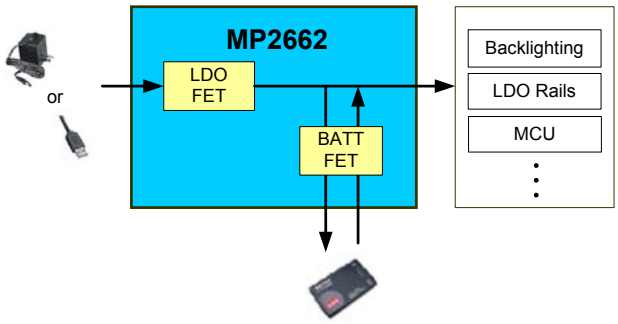


Figure 2: Power Path Management Structure

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of IN and BATT. When IN or BATT rises above the respective UVLO threshold, the sleep comparator, battery depletion comparator and the battery FET driver are active. I²C interface is ready for communication and all the registers are reset to the default value. The host can access all the registers.

Input OVP and UVLO

The MP2662 has input OVP threshold and input UVLO threshold. Once the input voltage is out of normal input voltage range, the Q1 (LDO FET) will be turned off immediately.

When the input voltage is identified as a good source, there is a 200µs immunity timer active. If the input power is good until the 200µs expires, system will start up. Otherwise, the Q1 will keep off.

Figure 3 depicts the operation profile.

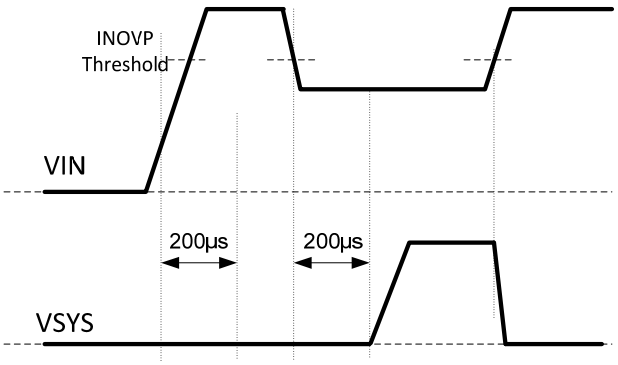


Figure 3: Input Power Detection Operation Profile

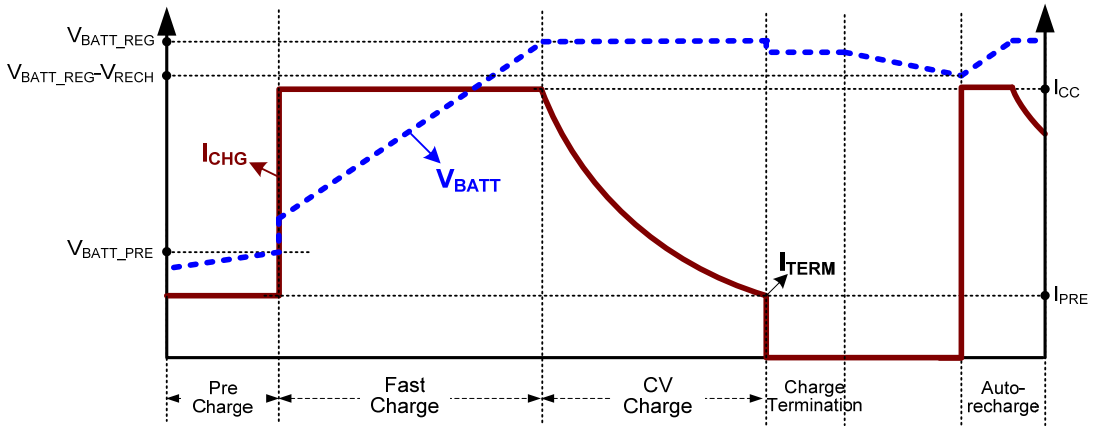


Figure 4: Battery Charge Profile

Power Path Management

The IC employs the pass-through power path structure with the battery FET (Q2) decoupling the system from the battery, which allows the separate control between the system and the battery. The system is given the priority to start up even with a deeply-discharged or missed battery. So when the input power is available even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDO FET.

As depicted in Figure 1, the direct power structure composes of a frond-end LDO FET between IN and SYS pin, and a battery FET between SYS and BATT pin. LDO FET and battery FET can be controlled by I²C.

Table 1: FET Control by I²C

FET On/Off Changed By Control	HIZ Mode and Charge Control	
	SET EN_HIZ to 1	SET CEB to 1
LDO FET	OFF	x
Battery FET (Charging)	x	OFF
Battery FET (Discharging)	x	x

Note: x=Don't Care

For the system voltage control,

(1) When the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}.

(2) When the input voltage is lower than V_{SYS_REG}, the LDO FET is fully on with input current limit.

V_{SYS_REG} can be programmed through REG07H Bit [3:0].

Battery Charge Profile

The IC provides three main charging phases: pre-charge, fast-current charge and constant-voltage charge as shown in Figure 4.

Phase 1 (Pre-charge):
The IC is able to safely pre charge the deeply depleted battery until the battery voltage reaches pre charge to fast charge threshold V_{BATT_PRE}.
The pre charge current is also programmed through REG03H Bit [3:0]. If V_{BATT_PRE} is not reached before pre-charge timer (1hr) expires, the charge cycle is ceased and a corresponding timeout fault signal is asserted.

Phase 2 (Fast Charge)
When the battery voltage exceeds V_{BATT_PRE}, the IC enters into fast charge phase. The fast charge current can be programmable via REG02H Bit [5:0].

Phase 3 (Constant-voltage Charge)
When the battery voltage rises to the battery full voltage V_{BATT_REG} set via REG04H Bit [7:2], the charge mode changes from CC mode to CV mode, the charge current begins to decrease.

Assuming the termination function EN_TERM set via REG05H Bit [4] = 1, the charge cycle is considered as completed when following condition is valid:

1. The charge current I_{CHG} reaches the termination current threshold I_{TERM}, a 3.2s delay timer is initiated;
2. During 3.2s delay period, the I_{CHG} is always smaller than I_{TERM}+I_{TERM_HYS}.

The charge status is updated to charge done once the 3.2s delay timer expired.

The termination charge current threshold I_{TERM} can be programmed by the REG03H Bit [3:0].

Also, the charge current will be terminated when termination conditions are met if TERM_TMR set via REG05H Bit [0] = 0; otherwise the charge current keeps tapering off.

If EN_TERM = 0, the termination function is disabled and all above actions is invalid (see Table 2).

Table 2: Termination Function Selection Table

EN_TERM	TERM_TMR	After I_{BATT} reaches I_{TERM} in CV mode	
		Operation	Charge Status
0	x	Keep CV Charge	Charge
1	0	Charge Done	Charge Done
1	1	Keep CV Charge	Charge Done

Note: x=Don't Care

During the whole charging process, the actual charge current may be less than the register setting due to other loop regulations like dynamic power management (DPM) regulation (input voltage, input current), or thermal regulation.

A new charge cycle starts when the following conditions are valid:

- The input power is recycled, or
- Battery charging is enabled by I²C, or
- Auto-recharge kicks in

Under the following conditions:

- No thermistor fault at NTC
- No safety timer fault
- No battery over voltage event
- BATFET is not forced to turn off

Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged due to the system consumption or self-discharge. When the battery voltage is discharged below recharge threshold and V_{IN} is still in the operation range, the IC automatically starts another new charging cycle without the requirement of manually re-starting a charging cycle.
Only when EN_TERM = 1 and TERM_TMR = 0, the auto recharge function is valid.

Battery Over-Voltage Protection

The IC is designed with a built-in battery over voltage limit about 130mV higher than the V_{BATT_REG}. When the battery over voltage event occurs, the IC immediately suspends the charging and asserts a fault.

Input Current and Input Voltage Based Power Management

To meet the input source (USB usually) maximum current limit specification, the IC features the input current based power management by continuously monitoring the input current. The total input current limit can be programmed via the I²C to prevent the input source from over-loaded.

If the preset input current limit is higher than the rating of the input source, the back-up input voltage based power management also works to prevent the input source from being over-loaded. Either the input current limit or the input voltage limit is reached, the Q1 FET between IN and SYS will be regulated so that the total input power will be limited. As a result the system voltage drops, once the system declines to minimum value of the V_{SYS_REG}-135mV and V_{IN} – 345mV, the charge current will be reduced to prevent the system voltage from dropping further.

The voltage based dynamic power management (DPM) will regulate the input voltage to V_{IN_MIN} when the load is over the input power capacity.

The V_{IN_MIN} set via I²C should be at least 250mV higher than V_{BATT_REG} to make sure the stable operation of the regulator.

Battery Supplement Mode

As mentioned above, the charge current is reduced to keep the input current or input voltage in regulation when DPM happens. If the charge current is reduced to zero and the input source is still overloaded due to heavy system load, the system voltage starts to decrease. Once the system voltage falls 30mV below the battery voltage, the IC enters battery supplement mode and the ideal diode mode will be enabled. The battery FET is regulated to maintain the V_{BATT} – V_{SYS} at 22.5mV when I_{DSCHG} (supplement current)*R_{ON_BATT} is lower than 22.5mV, in the case the I_{DSCHG} *R_{ON_BATT} is higher than 22.5mV, the battery FET is fully turned on to keep ideal forward voltage. During system load decreasing, once V_{SYS} is higher than V_{BATT}+20mV, the ideal diode mode will be disabled. Figure 5 shows the dynamic power management and battery supplement mode operation profile.

When V_{IN} is not available, IC operates in discharge mode, the battery FET is always fully on to reduce the loss.

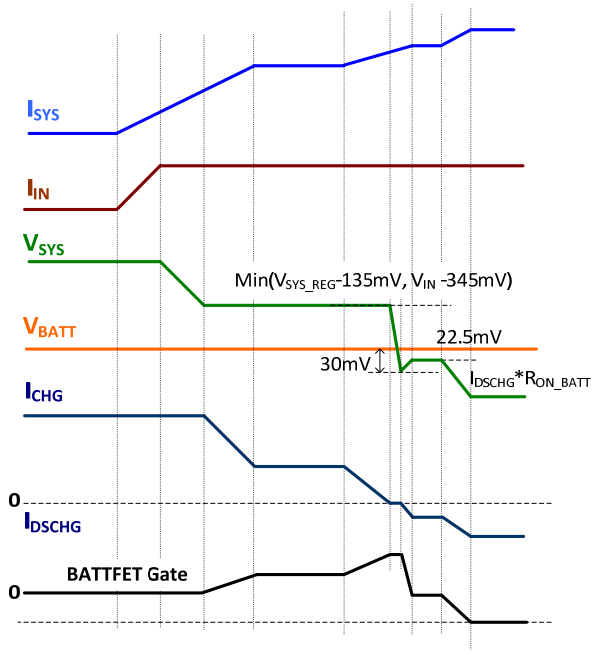


Figure 5: Dynamic Power Management and Battery Supplement Operation Profile

Battery Regulation Voltage

The battery voltage for the constant voltage regulation phase is V_{BATT_REG}. When V_{BATT_REG}= 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to +50°C.

Thermal Regulation and Thermal Shutdown

The IC continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches preset limit of T_{J_REG} (default 120 ºC), the IC starts to reduce the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60ºC to 120ºC help system design to meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via REG07H Bit [5:4].

When the junction temperature reaches 150ºC, both Q1 and Q2 are turned off.

NTC (Negative Temperature Coefficient) Temperature Sensor

The NTC pin allows the IC to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment of the battery. A resistor with appropriate value should be connected from VDD to NTC and the thermistor is connected from NTC to ground. The voltage on NTC pin is determined by the resistor divider whose divide ratio depends on temperature. The IC internally sets a pre-determined upper and lower bound of the divide ratio for NTC cold and NTC hot.

In MP2662, I²C default setting is the PCB_OTP; user can change the function through I²C:

Table 3 NTC Function Selection Table

I²C Control		Function
EN_NTC	EN_PCB_OTP	
0	x	Disable
1	1	NTC
1	0	PCB_OTP

Note: x=Don't Care

When PCB_OTP is selected, if the NTC pin voltage is lower than the NTC hot threshold, both the LDO FET and battery FET are off. The PCB_OTP fault also will set the NTC_FAULT status (REG09H Bit [1]) to 1 to show the fault.

The operation will resume once the NTC pin voltage is higher than the NTC hot threshold.

NTC function only works in charge mode. Once NTC pin voltage falls out of this divide ratio which means the temperature is outside the safe operating range, the IC will stop the charging and report it on status bits. Charging will automatically resume after the temperature falls back into the safe range.

Safety Timer

The IC provides both the pre-charge and fast charge safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 1 hour when battery voltage is lower than V_{BATT_PRE}. The fast charge safety timer starts when the battery enters fast charge. The user can program fast charge safety timer through I²C. The safety timer feature can be disabled via I²C.

The following actions restart the safety timer,

- A new charge cycle is kicked in.
- Write REG01H Bit [3] from 1 to 0 (charge enable)
- Write REG05H Bit [3] from 0 to 1 (safety timer enable)
- Write REG02H Bit [7] from 0 to 1 (software reset)

Host Mode and Default Mode

The IC is host-controlled device. After power on reset, the IC starts in the watchdog timer expiration state, or default mode. All the registers are in the default settings.

Watchdog timer works in both charge and discharge mode, when the watchdog timer out, most registers will be back to the default value (refer to the I2C REGISTER MAP). Be noted that, during both charge and discharge mode, when watchdog timer out, both the LDO FET and battery FET are turned off, and will be turned on automatically after t_{RST_DUR} which can be programmed by REG01H Bit [5].

And to save the quiescent current during discharge mode, the watchdog timer can be turned off during discharge mode only by set the REG05H Bit [7] to 0.

Any write to the IC transits it to host mode. All the charge parameters are programmable. If the watchdog timer (REG05H Bit [6:5]) is not disabled, the host has to reset the watchdog timer regularly by writing 1 to REG02H Bit [6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC goes back into default mode. The watchdog timer limit can also be programmed or disabled by host control.

When the REG05H Bit [6:5] is set to 00, then the watchdog timer is disabled under both charge mode and discharge mode no matter REG05H Bit [7] status is.

The operation could also be turned to default mode when one of the following conditions are valid:

- Refresh input without battery
- Re-insert battery with no V_{IN}
- Register Reset REG02H Bit [7] is reset

Battery Discharge Function

If battery is connected and the input source is missing, the battery FET is fully on when V_{BATT} is above the V_{BATT_UVLO} threshold. The 100mΩ battery FET minimizes the conduction loss during discharge. The quiescent current of the IC is as low as 6μA in this mode. The low on-resistance and low quiescent current help extend the running time of the battery.

Over Discharge Current Protection

The IC has the over discharge current protection in discharge mode and supplement mode. Once the I_{BATT} exceeds programmable discharge current limit (default at 2A), after 60us delay, the battery FET will be turned off and the part goes into hiccup mode as over current protection. The discharge current can be programmed high to 3.2A through the I²C. Besides, if the discharge current goes high to hit internal fixed current limit (about 3.7A), the battery FET will be turned off and starts the hiccup mode immediately.

Similarly, when the battery voltage falls below the programmable V_{BATT_UVLO} threshold (default at 2.76V), the battery FET will be turned off to prevent over discharge.

Table 4: Shipping Mode Control

Items	Enter Shipping Mode	Exit Shipping Mode	
	Set FET_DIS to 1	INT H to L for 2s	VIN Plug In
LDO FET	x	x	ON
Battery FET (Charging)	OFF	ON	ON (2s later)
Battery FET (Discharging)	OFF	ON	ON (2s later)

Note: x=Don't Care

System Short Circuit Protection

The MP2662 features SYS node short circuit protection for both IN to SYS path and BATT to SYS path.

The system voltage is continuously monitored, only if the V_{SYS} is lower than 1.5V, the system short circuit protection for both IN to SYS path and BATT to SYS path is active. And the I_{DSCHG} will be decreased to 1/2 of the original value.

1) IN to SYS path:

Once I_{IN} is found over the protection threshold, both the LDO FET and the BATT FET are turned off immediately. And the operation of the IC goes into the hiccup mode. Otherwise the max current limit is not hit, while the setting input current limit is reached, I_{IN} is regulated at I_{IN_LIM} the hiccup mode also starts after a 60us delay. The interval of the hiccup mode is 800us.

2) BATT to SYS path:

Once I_{BATT} is found over the 3.7A protection threshold, both the LDO FET and the BATT FET are turned off immediately and the operation of the IC goes into the hiccup mode. Besides, while the battery discharge current limit threshold is reached, the hiccup mode also starts after a 60us delay. The interval of the hiccup mode is 800us.

For details, please refer to flow chart in Figure 11.

Particularly, if the system short circuit happens when both input and battery are present, the protection mechanism of both paths will work, the faster one dominates the hiccup operation.

Interrupt to Host (INT)

The IC also has an alert mechanism which can output an interrupt signal via INT pin to notify the system on the operation by outputting a 256μs low state INT pulse. All of the below events will trigger the INT output,

- Good input source detected
- UVLO or input over voltage protection
- Charge completed
- Charging status change
- Any fault in REG09H (Watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the IC sends out INT pulse and latches the fault state in REG09H. After the IC quit the fault state, the fault bit could be released to 0 after the host reads REG09H. The NTC fault is not latched and always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set, which means, even the event which causes the INT signal happened, user can just keep INT high when the INT signal is not acceptable in the application, via setting the INT control Bit in REG06H Bit [4:0].

Battery Disconnection Function

In the application that the battery is not removable, it's essential to disconnect the battery from the system for shipping mode in stock or to allow the reset of the system power during the application. MP2662 provides both shipping mode (shown in Table 4) and system reset mode for different applications.

The IC has a register bit FET_DIS for battery disconnection control. If this bit is set to 1, MP2662 enters shipping mode after a delay time, which can be programmed by REG09H Bit [7:6], the battery FET turns off and the FET_DIS bit refresh to 0 after the battery FET is off. Pulling down INT pin or plug in the input adapter for 2s, the part can wake up from shipping mode.

The IC can also reuse INT pin to cut off the path from battery to system under the condition need to reset the system manually. Once the logic at INT set to low for more than t_{RST_DGL} which can be programmed by REG01H Bit [7:6], the battery is disconnected from the system by turning off the battery FET, the off state lasts for t_{RST_DUR} which can be programmed by REG01H Bit [5], then the battery FET will be automatically turned on and system is powered by the battery again. During the off period, the INT pin is not limit to be high or low.

So, the IC can reset the system by controlling the INT pin. This system reset function shown in Figure 6.

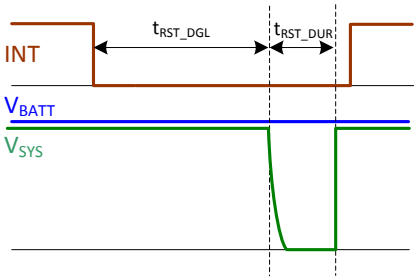


Figure 6: System Reset Function Operation Profile

I²C REGISTER MAP

IC Address: 07H (Reserved some trim options)

Register Name	Address	R/W	Description	Default
REG00	0x00	R/W	Input Source control register	1001 1111
REG01	0x01	R/W	Power on configuration register	1010 1100
REG02	0x02	R/W	Charge Current Control Register	0000 1111
REG03	0x03	R/W	Dis-charge/ Termination Current	1001 0001
REG04	0x04	R/W	Charge Voltage Control Register	1010 0011
REG05	0x05	R/W	Charge Termination/Timer Control Register	0011 1010
REG06	0x06	R/W	Miscellaneous Operation Control Register	1100 0000
REG07	0x07	R/W	System Voltage Regulation Register	0011 1001
REG08	0x08	R	System Status Register	0100 0000
REG09	0x09	R	Fault Register	0000 0000
REG0A	0x0A	NA	Address Register	1110 0000

REG 00H (DEFAULT: 1001 1111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{IN_MIN} [3]	1	Y	N	R/W	640mV	Offset: 3.88V Range: 3.88V – 5.08V Default: 4.60V (1001)
6	V_{IN_MIN} [2]	0	Y	N	R/W	320mV	
5	V_{IN_MIN} [1]	0	Y	N	R/W	160mV	
4	V_{IN_MIN} [0]	1	Y	N	R/W	80mV	
3	I_{IN_LIM} [3]	1	Y	N	R/W	240mA	Offset: 50mA Range: 50mA -500mA Default: 500mA (1111)
2	I_{IN_LIM} [2]	1	Y	N	R/W	120mA	
1	I_{IN_LIM} [1]	1	Y	N	R/W	60mA	
0	I_{IN_LIM} [0]	1	Y	N	R/W	30mA	

REG 01H (DEFAULT: 1010 1100)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{RST_DGL}[1]	1	Y	Y	R/W	00 – 8s; 01 – 12s; 10 – 16s; 11 – 20s	Pull INT low time period to disconnect the battery Default: 16s (10)
6	t_{RST_DGL} [0]	0	Y	Y	R/W		
5	t_{RST_DUR}	1	Y	Y	R/W	0 – 2s; 1 – 4s	Battery FET lasts off time before auto-on Default: 4s (1)
4	EN_HIZ(6)	0	Y	Y	R/W	0 – Disable; 1 – Enable	Default: Disable (0)
3	CEB	1	Y	Y	R/W	0 – Charge Enable; 1 – Charge Disabled	Charge configuration Default: charge disabled (1)
2	V_{BATT_UVLO} [2]	1	Y	Y	R/W	360mV	Battery UVLO Threshold Offset: 2.4V Range: 2.4V- 3.03V Default: 2.76V (100)
1	V_{BATT_UVLO} [1]	0	Y	Y	R/W	180mV	
0	V_{BATT_UVLO} [0]	0	Y	Y	R/W	90mV	

Notes:
6) This bit only controls the on and off of the LDO FET.

REG 02H (DEFAULT: 0000 1111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Register Reset	0	Y	N	R/W	0 – Keep current setting; 1 – Reset	Default: Keep current register setting (0)
6	I²C Watchdog Timer Reset	0	Y	Y	R/W	0 – Normal; 1 – Reset	Default: Normal(0)
5	I_{CC} [4]	0	Y	Y	R/W	256mA	Fast Charge Current Setting Offset: 8mA Range: 8mA (000000) – 456 (111000)mA Default: 128mA (001111)
4	I_{CC} [3]	0	Y	Y	R/W	128mA	
3	I_{CC} [2]	1	Y	Y	R/W	64mA	
2	I_{CC} [1]	1	Y	Y	R/W	32mA	
1	I_{CC} [0]	1	Y	Y	R/W	16mA	
0	I_{CC} [4]	1	Y	Y	R/W	8mA	

REG 03H (DEFAULT: 1001 0001)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I_{DSCHG}[3]	1	Y	Y	R/W	1600mA	BATT to SYS Discharge Current Limit Offset: 200mA Range: 400mA-3.2A Valid Range: 0001 - 1111 Default: 2000mA(1001)
6	I_{DSCHG}[2]	0	Y	Y	R/W	800mA	
5	I_{DSCHG}[1]	0	Y	Y	R/W	400mA	
4	I_{DSCHG}[0]	1	Y	Y	R/W	200mA	
3	I_{TERM} [3]	0	Y	Y	R/W	16mA	Termination Current Offset: 1mA Range: 1mA-31mA Default: 3mA(0001)
2	I_{TERM} [2]	0	Y	Y	R/W	8mA	
1	I_{TERM} [1]	0	Y	Y	R/W	4mA	
0	I_{TERM} [0]	1	Y	Y	R/W	2mA	

REG 04H (DEFAULT: 1010 0011)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_REG} [5]	1	Y	Y	R/W	480mV	Battery Regulation Voltage Offset: 3.60V Range: 3.60V – 4.545V Default: 4.2V (101000)
6	V_{BATT_REG} [4]	0	Y	Y	R/W	240mV	
5	V_{BATT_REG} [3]	1	Y	Y	R/W	120mV	
4	V_{BATT_REG} [2]	0	Y	Y	R/W	60mV	
3	V_{BATT_REG} [1]	0	Y	Y	R/W	30mV	
2	V_{BATT_REG} [0]	0	Y	Y	R/W	15mV	
1	V_{BATT_PRE}	1	Y	Y	R/W	0 – 2.8V; 1 – 3.0V	Pre-charge to Fast Charge Threshold Default: 3.0V (1)
0	V_{RECH}	1	Y	Y	R/W	0 – 100mV; 1 – 200mV	Battery Recharge Threshold (below V_{BATT_REG}) Default: 200mV (1)

REG 05H (DEFAULT: 0011 1010)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_WD_DISCHG	0	Y	N	R/W	0 – Disable; 1 – Enable	Watchdog Control in discharge mode Default: Disable (0)
6	WATCHDOG [1]	0	Y	N	R/W	00 – Disable Timer; 01 – 40s; 10 – 80s; 11 – 160s	I²C Watchdog Timer Limit Default: 40s (01) If Bit [6:5] = 00, then watchdog timer is disabled no matter Bit 7 is set or not.
5	WATCHDOG [0]	1	Y	N	R/W		
4	EN_TERM	1	Y	Y	R/W	0 – Disable; 1 – Enable	Termination Setting (control the termination is allowed or not) Default: Enable (1)
3	EN_TIMER	1	Y	Y	R/W	0 – Disable; 1 – Enable	Safety Timer Setting Default: Enable Timer (1)

2	CHG_TMR [1]	0	Y	Y	R/W	00 – 3hrs; 01 – 5hrs; 10 – 8hrs; 11 – 12hrs	Fast Charge Timer Default: 5hrs (01)
1	CHG_TMR [0]	1	Y	Y	R/W		
0	TERM_TMR	0	Y	Y	R/W	0 – Disable; 1 – Enable	Termination Timer Control (when TERM_TMR is enabled, the IC will not suspend the charge current after charge termination) Default: (0)

REG 06H (DEFAULT: 1100 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_NTC	1	Y	Y	R/W	0 – Disable; 1 – Enable	Default: Enable (1)
6	TMR2X_EN	1	Y	Y	R/W	0 – Disable 2X extended safety timer during PPM; 1 – Enable 2X extended safety timer during PPM	Default: Enable (1)
5	FET_DIS(7)	0	Y	N	R/W	0 – Enable; 1 – Turn Off	Default: Enable (0)
4	PG_INT_Control	0	Y	Y	R/W	0 – On; 1 – Off	Default: On (0)
3	EOC_INT_Control	0	Y	Y	R/W	0 – On; 1 – Off	Charge Completed INT Mask Control Default: On (0)
2	CHG STATUS_INT_Control	0	Y	Y	R/W	0 – On; 1 – Off	Charging Status Change INT Mask Control (charging status contain: not charging, pre charge and charge) Default: On (0)
1	NTC_INT_Control	0	Y	Y	R/W	0 – On; 1 – Off	Default: On (0)
0	BATTOVP_INT_Control	0	Y	Y	R/W	0 – On; 1 – Off	Default: On (0)

Notes:
7) This bit controls the on and off of the Battery FET include charge and discharge.

REG 07H (DEFAULT: 0011 1001)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_PCB_OTP	0	Y	Y	R/W	0 – Enable; 1 – Disable	PCB_OTP Enable Default: Enable (0)
6	EN_VINLOOP	0	Y	Y	R/W	0 – Enable; 1 – Disable	Default: Enable (0)
5	T_{J_REG} [1]	1	Y	Y	R/W	00 – 60ºC; 01 – 80 ºC; 10 – 100 ºC; 11 – 120ºC	Thermal Regulation Threshold Default: 120ºC (11)
4	T_{J_REG} [0]	1	Y	Y	R/W		
3	V_{SYS_REG} [3]	1	Y	N	R/W	400mV	System Voltage Regulation Offset: 4.2V Range: 4.2V – 4.95V Default: 4.65V (1001)
2	V_{SYS_REG} [2]	0	Y	N	R/W	200mV	
1	V_{SYS_REG} [1]	0	Y	N	R/W	100mV	
0	V_{SYS_REG} [0]	1	Y	N	R/W	50mV	

REG 08H (DEFAULT: 0100 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG_FAULT	0	NA	NA	R	0 – Normal; 1 – Watchdog timer expiration	Normal (0)
6	Rev [1]	1	NA	NA	R	00 – reserved; 01 – reserved; 10 – MP2662; 11 – reserved	Revision Number Default: (10)
5	Rev [0]	0	NA	NA	R		
4	CHG_STAT [1]	0	NA	NA	R	00 – Not Charging; 01 – Pre Charge; 10 – Charge; 11 – Charge Done	Not Charging (00)
3	CHG_STAT [0]	0	NA	NA	R		
2	PPM_STAT	0	NA	NA	R	0 – No PPM; 1 – IN PPM	No PPM (0)
1	PG_STAT	0	NA	NA	R	0 – Power Fail; 1 – Power Good	Not Power Good (0)
0	THERM_STAT	0	NA	NA	R	0 – No Thermal Regulation; 1 – In Thermal Regulation	Normal (0)

REG 09H (DEFAULT: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_SHIPPING_DGL[1]	0	Y	N	R/W	00 – 1s; 01 – 2s; 10 – 4s; 11 – 8s	Enter shipping mode deglitch time Default: 1s (00)
6	EN_SHIPPING_DGL[0]	0	Y	N	R/W		
5	VIN_FAULT	0	NA	NA	R	0 – Normal; 1 – Input fault (OVP or bad source)	Normal (0)
4	THEM_SD	0	NA	NA	R	0 – Normal; 1 – Thermal Shutdown	Normal (0)
3	BAT_FAULT	0	NA	NA	R	0 – Normal; 1 – Battery OVP	Normal (0)
2	STMR_FAULT	0	NA	NA	R	0 – Normal; 1 – Safety Timer Expiration	Normal (0)
1	NTC_FAULT [1]	0	NA	NA	R	0 – Normal; 1 – NTC Hot	Normal (0)
0	NTC_FAULT [0]	0	NA	NA	R	0 – Normal; 1 – NTC Cold	Normal (0)

REG 0AH (DEFAULT: 1110 0000) (8)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	ADDR[2]	1	NA	NA	NA	001 – 01H; 010 – 02H; 011 – 03H; 100 – 04H; 101 – 05H; 110 – 06H; 111 – 07H	IC Address Default: 111 (07H)
6	ADDR[1]	1	NA	NA	NA		
5	ADDR[0]	1	NA	NA	NA		
4	Reserved	0	NA	NA	NA		
3	Reserved	0	NA	NA	NA		
2	Reserved	0	NA	NA	NA		
1	Reserved	0	NA	NA	NA		
0	Reserved	0	NA	NA	NA		

Notes:
8) This register is for OTP (One Time Program) only and not accessible.

OTP(9) MAP

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	N/A			I_{CC}: **8mA-456mA / 8mA** step				
0x03	N/A				I_{TERM}: **1mA-31mA/2mA step**			
0x04	V_{BATT_REG}: **3.6V-4.545V / 15mV** step						N/A	
0x05	N/A	WATCHDOG		N/A				
0x07	N/A	EN_VINLOOP	N/A					
0x0A	Address		N/A					

OTP(9) DEFAULT

OTP(9) Items	Default
I_{CC}	128mA
I_{TERM}	3mA
V_{BATT_REG}	4.2V
WATCHDOG	40s
EN_VINLOOP	Enable
Address	07H

Notes:
9) OTP is One Time Program.

STATE CONVERSION CHART

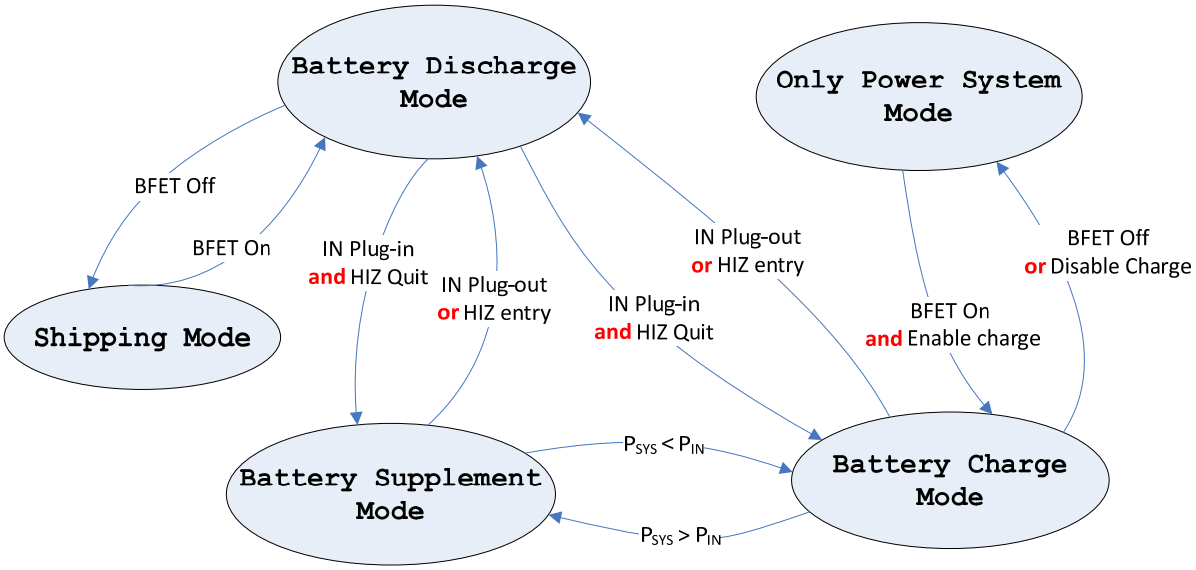


Figure 7: State Machine Conversion

CONTROL FLOW CHART

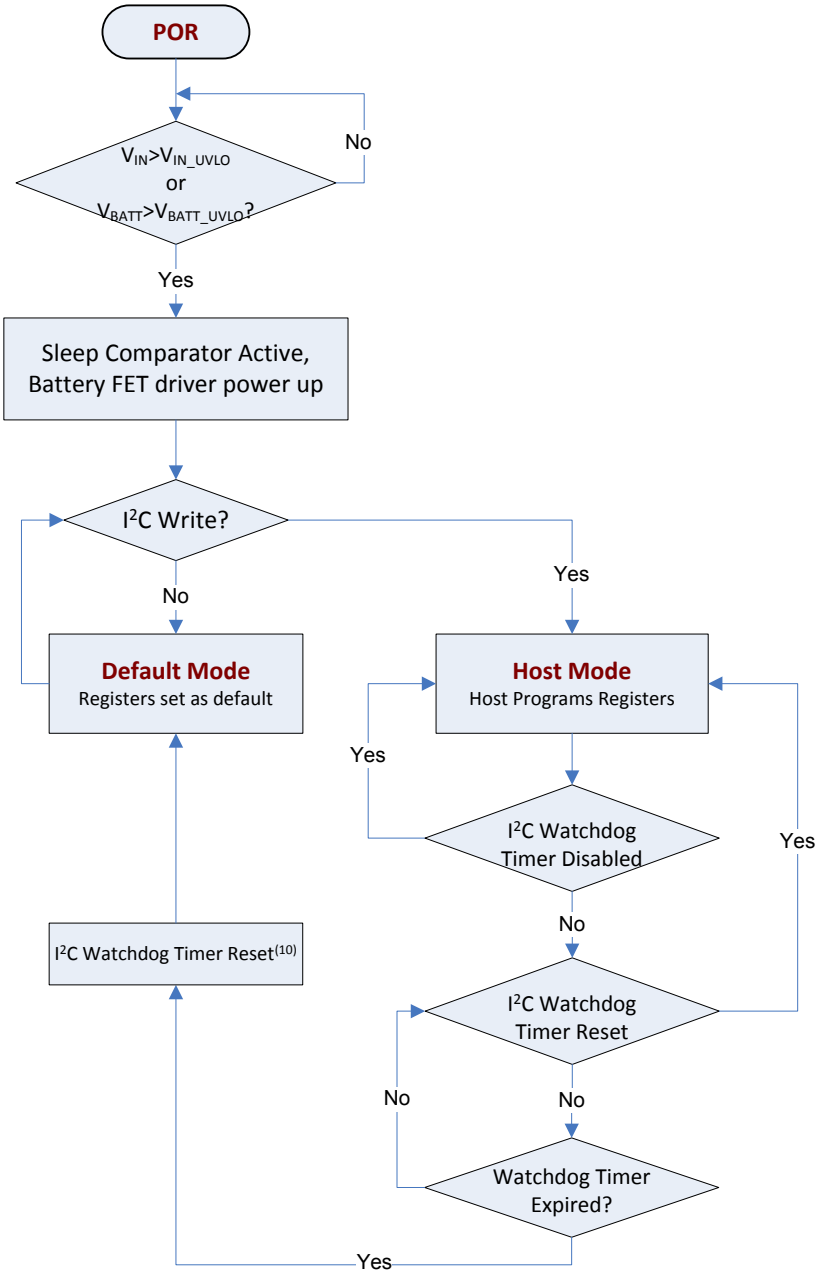


Figure 8: Default Mode and Host Mode Selection

Notes:
10) Once watchdog timer expired, the I²C watchdog timer reset is required, or the watchdog timer is not valid in the next time.

CONTROL FLOW CHART *(continued)*

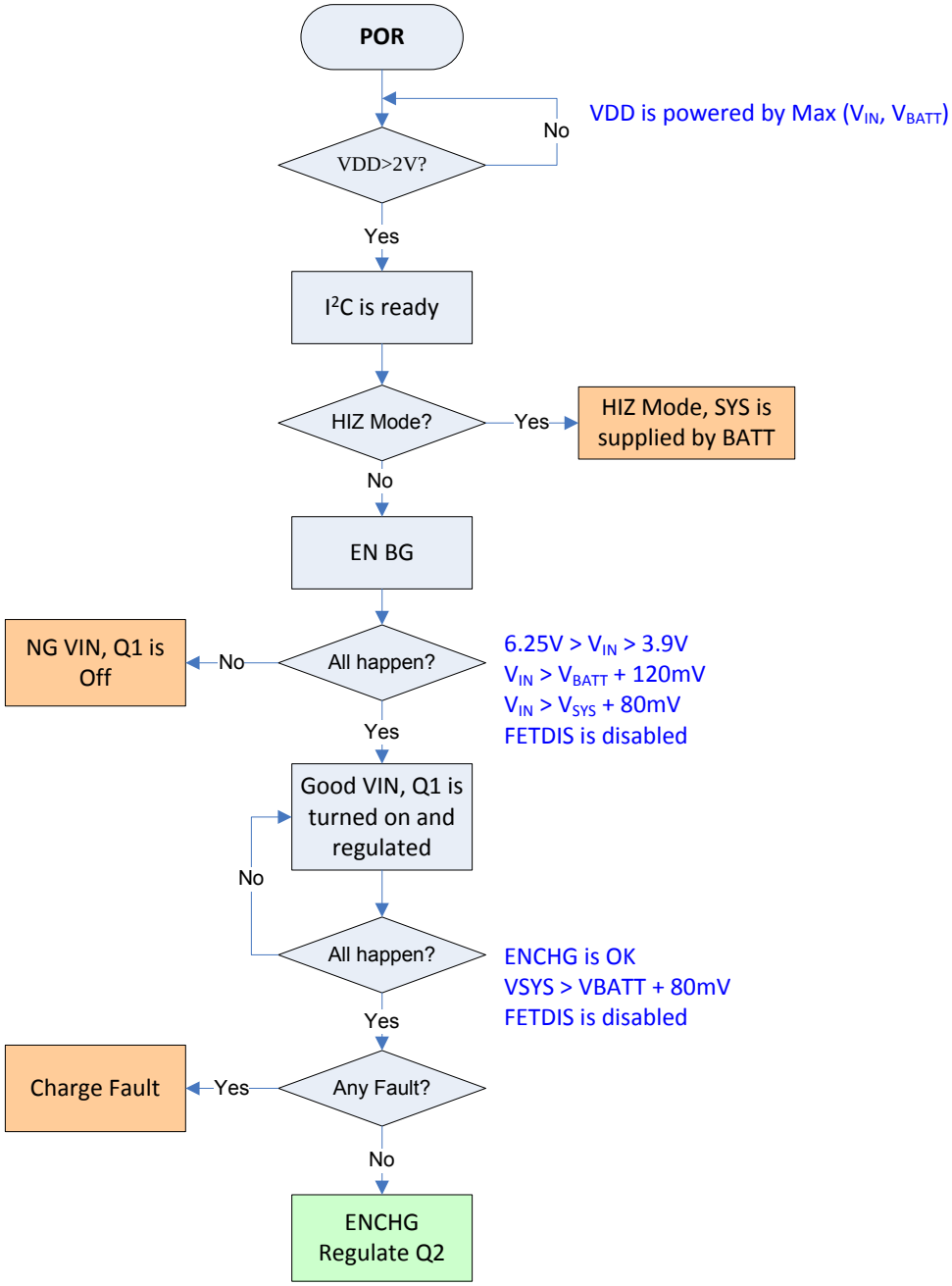


Figure 9: Input Power Start-up Flow Chart

CONTROL FLOW CHART *(continued)*

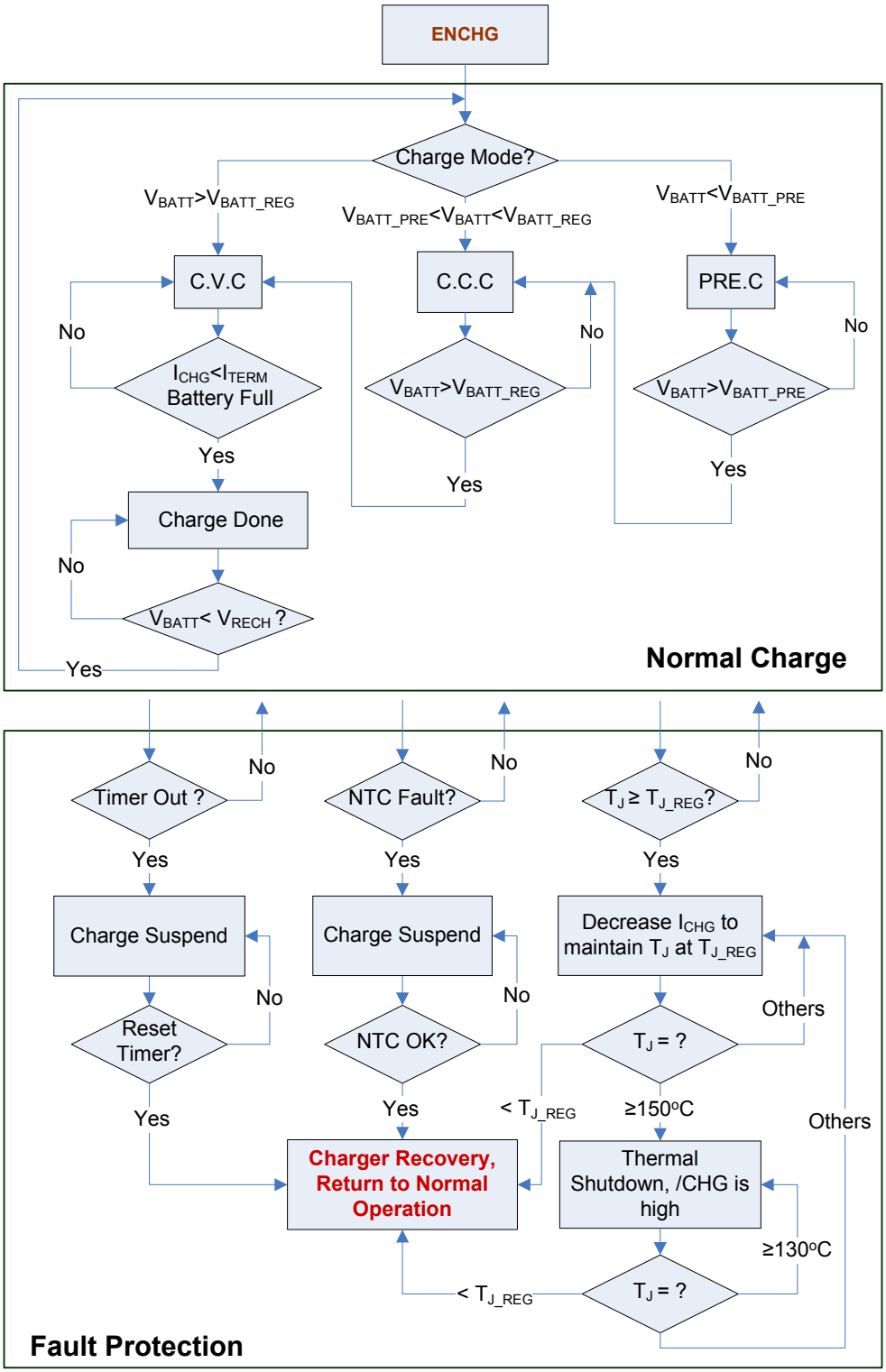


Figure 10: Charging Process

CONTROL FLOW CHART *(continued)*

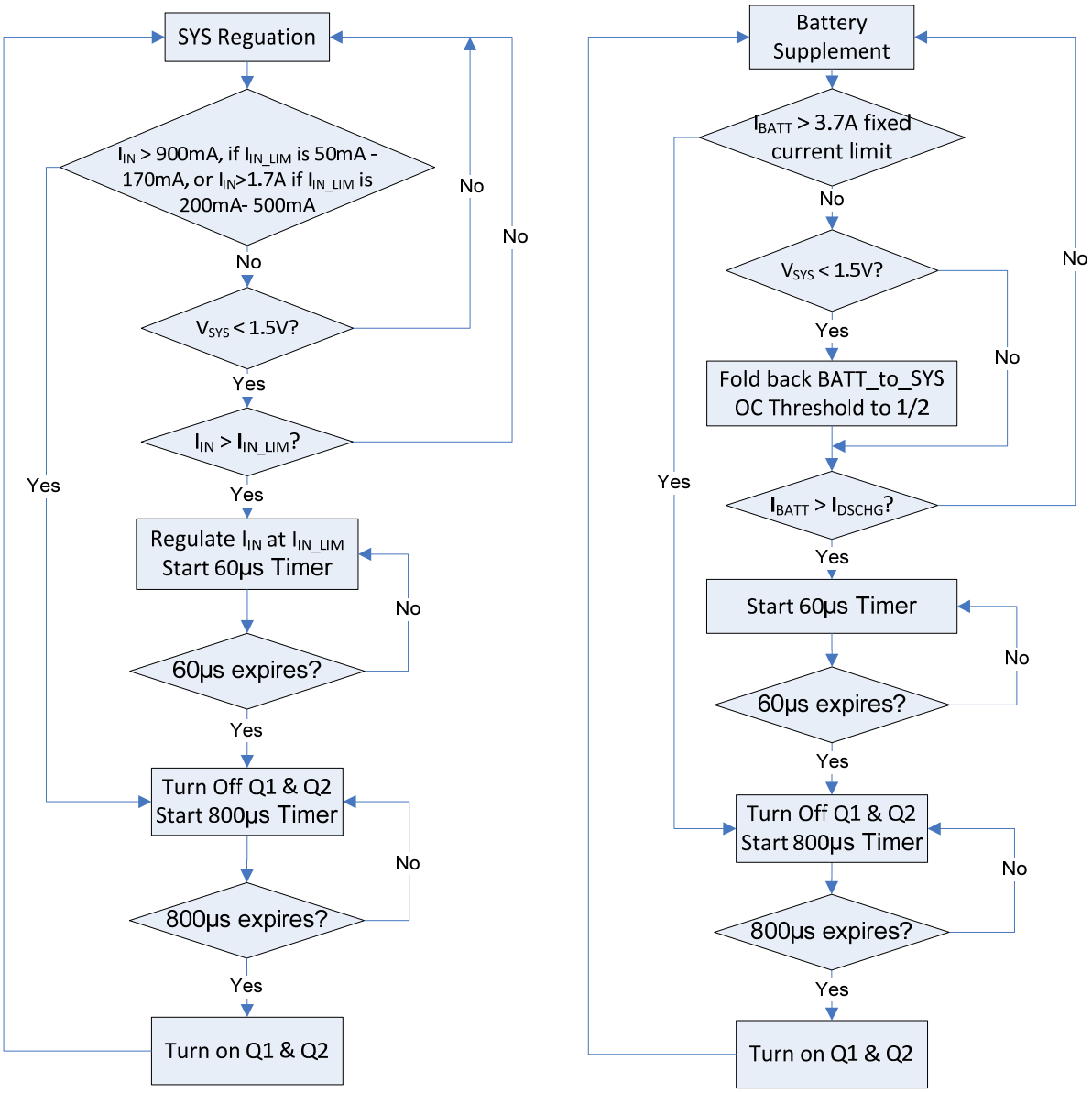


Figure 11: System Short Circuit Protection

APPLICATION INFORMATION

Resistor Choose for NTC Sensor

NTC pin uses a resistor divider from input source (VDD) to sense the battery temperature. The two resistors R_{T1} and R_{T2} allow the high temperature limit and low temperature limit to be programmed independently, as shown in Figure 12. In other words, the IC can fit most type of NTC resistor and different temperature operation range requirement with the two extra resistors.

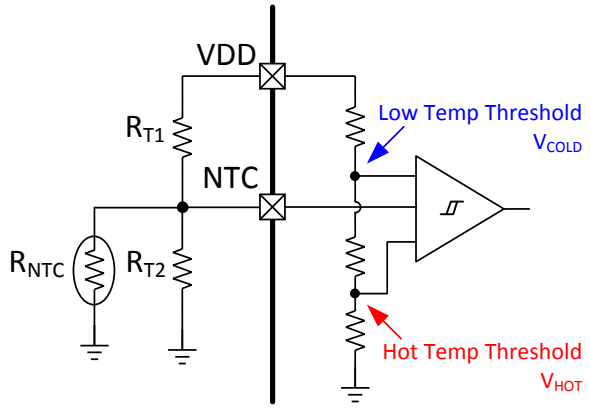


Figure 12: NTC Function Block

For a given NTC thermistor, R_{T1} and R_{T2} values depend on the type of the NTC resistor and can be calculated with Equation (1) and Equation (2):

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{T1} = \frac{1\text{-}V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where R_{NTCH} is the value of the NTC resistor at high temperature of the required temperature operation range, and R_{NTCL} is the value of the NTC resistor at low temperature.

For example, for thermistor NCP18XH103, R_{NTCL} is 27.219kΩ at 0°C, and R_{NTCH} is 4.161kΩ at 50°C. Using Equation (1) and Equation (2) to calculate R_{T1} = 7.44kΩ and R_{T2} = 30.79kΩ, assuming that the NTC window is between 0°C and 50°C and using the V_{COLD} and V_{HOT} values from the EC table.

External Capacitor Selection

Like most low-dropout regulators, the MP2662 requires external capacitors for regulator stability and voltage spike immunity. The device is specifically designed for portable applications requiring minimum board space and smallest components, these capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitor is required for stability, at least, a 4.7μF capacitor has to be connected between IN to GND for stable operation over full load current range. Basically, it is OK to have more output capacitance than input, as long as the input is at least 4.7μF.

Output Capacitor

The IC is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor (dielectric types X5R or X7R) >10μF is suitable in the MP2662 application circuit. For this device, the output capacitor should be connected between SYS pin and GND pin with thick trace and small loop area.

BATT to GND Capacitor

The capacitor from BATT pin to GND is also necessary for MP2662. A ceramic capacitor (dielectric types X5R or X7R) >4.7μF is suitable for the MP2662 application circuit.

VDD to GND Capacitor

The capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 1μF.

PCB Layout Guide

1) Put the external capacitors as close to the IC as possible to make sure the smallest input inductance and the ground impedance.

2) The PCB trace to connect the capacitor between VDD and GND is very important, and it should be put very close to the IC.

3) The GND for the I²C wire should be clean, and it should not be very close to the GND.

4) I²C wire should be put in parallel.

TYPICAL APPLICATION CIRCUITS

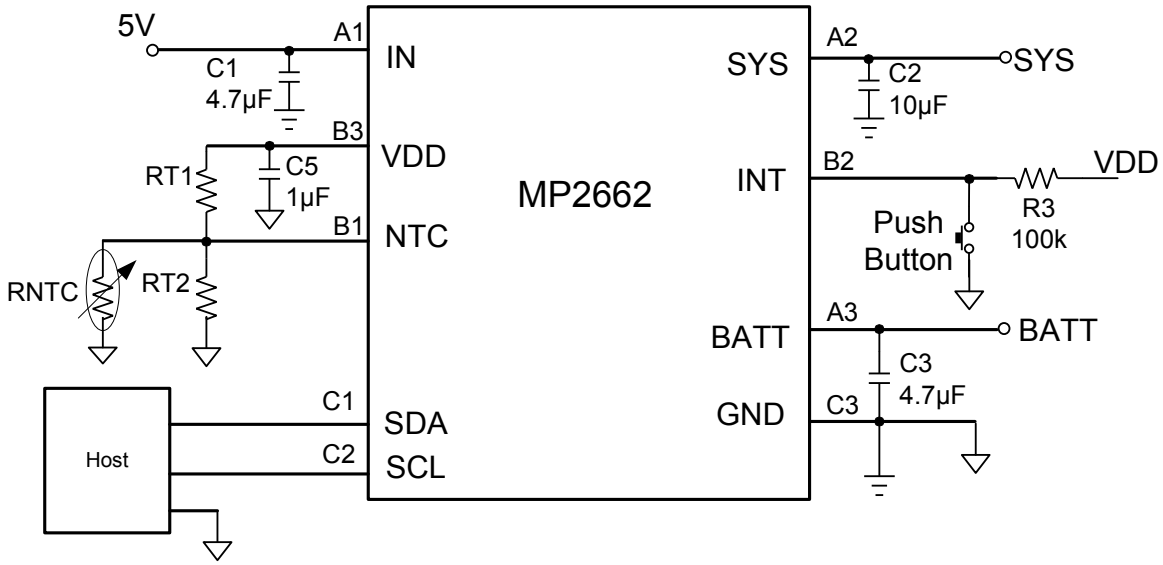


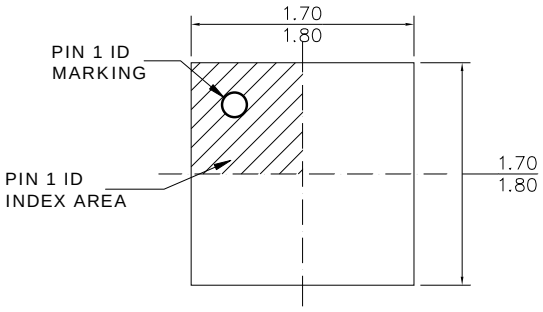
Figure 13: MP2662 Typical Application Circuit with 5V Input

Table 5: The Key BOM of Figure 13

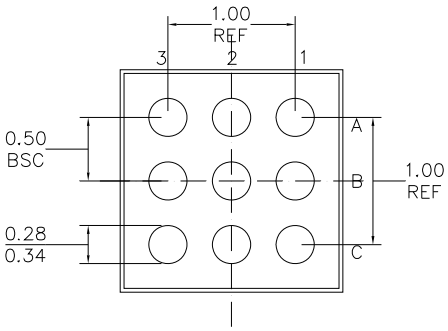
Qty	Ref	Value	Description	Package	Manufacture
2	C1, C3	4.7µF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
1	C2	10µF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	C5	1µF	Ceramic Capacitor;16V; X5R or X7R	0603	Any

PACKAGE INFORMATION

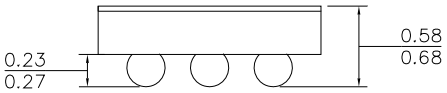
WLCSP-9 (1.75mmx1.75mm)



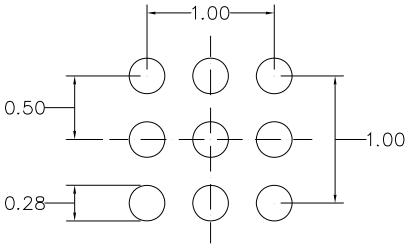
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.