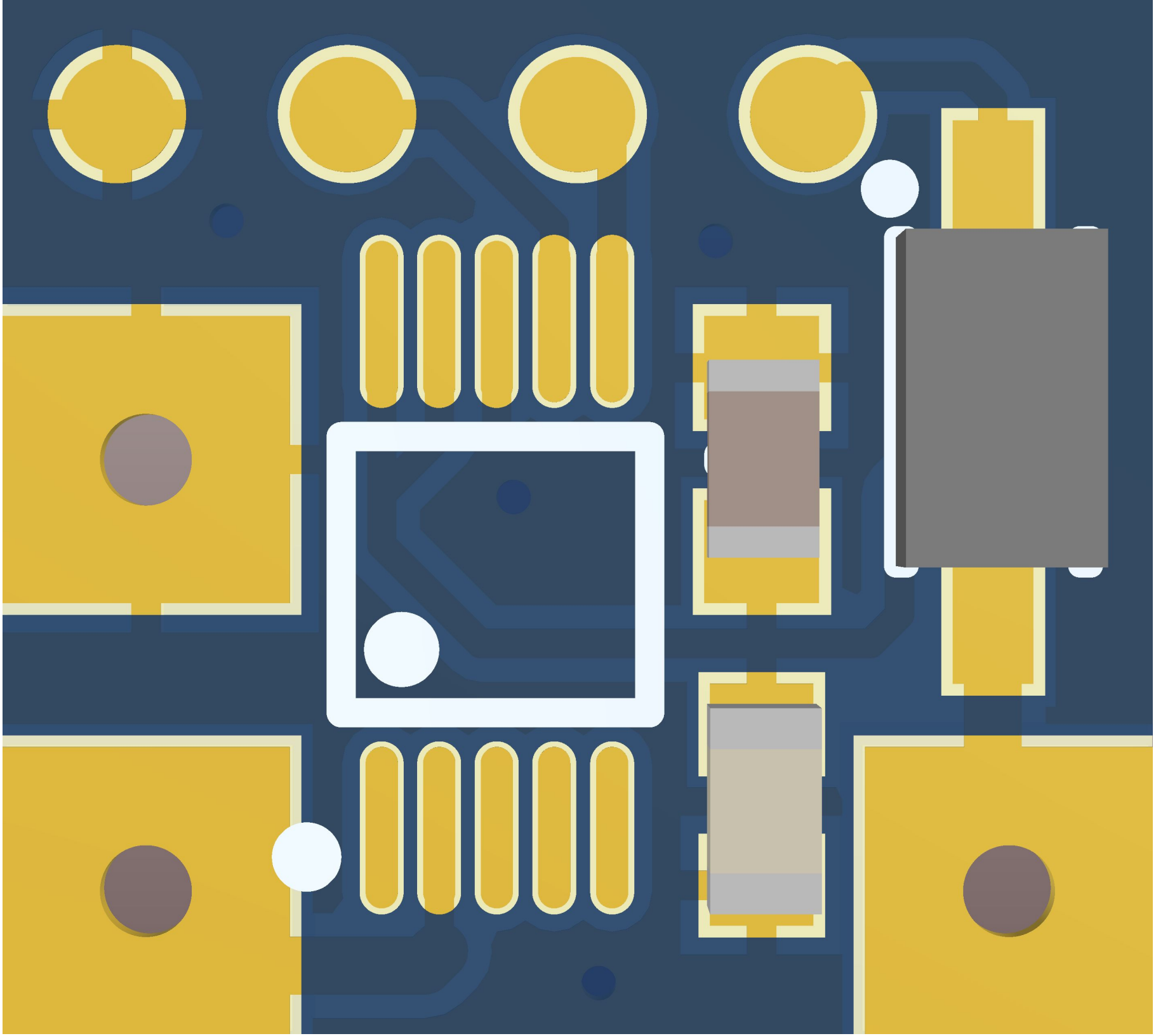
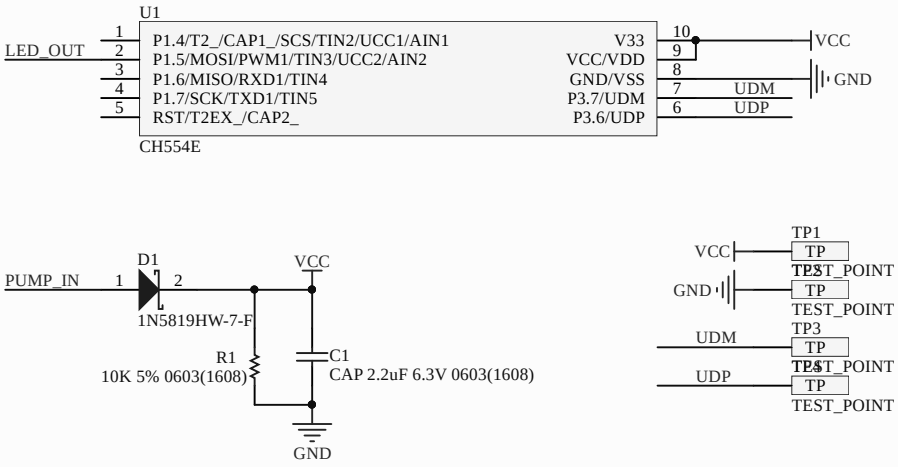
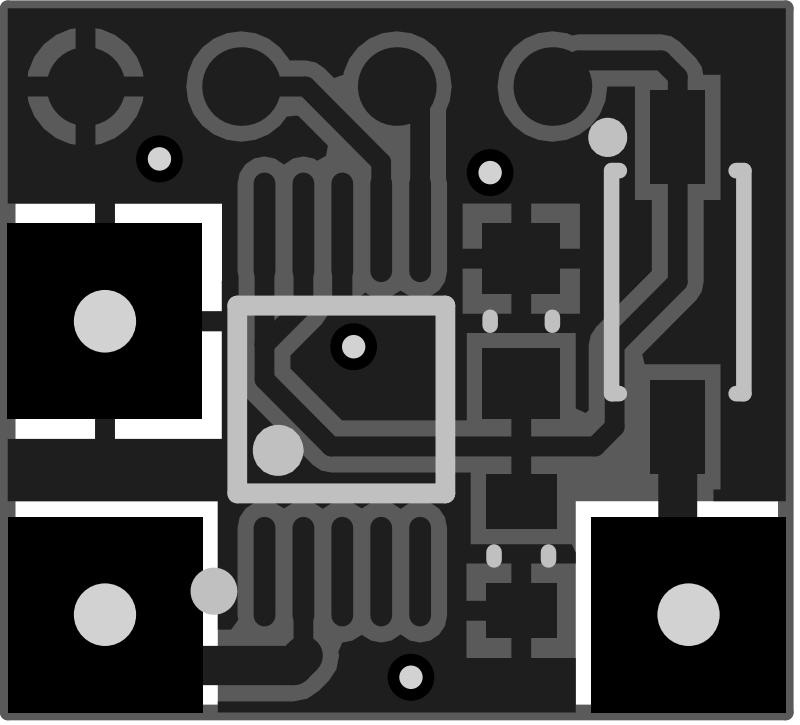




Title: *		
Project: PCB_Project1.PrjPCB		Revision: *
Date: 7/27/2018	Time: 5:05:16 PM	Sheet * of *



Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Blinkinlabs-Repos\solpix 2018\PCB1.PcbDoc

Warnings 0
Rule Violations 35

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=1mm) (Preferred=0.5mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	10
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	21
Silk to Silk (Clearance=0.254mm) (All),(All)	4
Net Antennae (Tolerance=0mm) (All)	0
Room Sheet1 (Bounding Region = (168.8mm, 48.8mm, 181mm, 59.8mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	35

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad C1-1(6.6mm,1.3mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad C1-2(6.6mm,2.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-1(3.3mm,1.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-10(3.3mm,6.2mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-2(3.8mm,1.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-3(4.3mm,1.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-4(4.8mm,1.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-6(5.3mm,6.2mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-7(4.8mm,6.2mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.118mm < 0.254mm) Between Pad U1-8(4.3mm,6.2mm) on Top Layer And Pac

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Arc (2.65mm,1.55mm) on Top Overlay And Pac
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Arc (2.65mm,1.55mm) on Top Overlay And Pac
Silk To Solder Mask Clearance Constraint: (0.227mm < 0.254mm) Between Arc (7.711mm,7.35mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-1(6.6mm,1.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-1(6.6mm,1.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-2(6.6mm,2.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad C1-2(6.6mm,2.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-1(6.6mm,5.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R1-1(6.6mm,5.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-2(6.6mm,4.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R1-2(6.6mm,4.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Pad U1-1(3.3mm,1.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-10(3.3mm,6.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Pad U1-2(3.8mm,1.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Pad U1-3(4.3mm,1.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Pad U1-4(4.8mm,1.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Pad U1-5(5.3mm,1.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-6(5.3mm,6.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-7(4.8mm,6.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-8(4.3mm,6.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad U1-9(3.8mm,6.2mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.223mm < 0.254mm) Between Text "BLON

KIN

LUBS" (9.4mm,3.1mm) on Bottom Overlay And Track (3.9mm,3.1mm)(3.9mm,8.6mm) on Bottom Ove

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.207mm < 0.254mm) Between Text "BLON

KIN

LUBS" (9.4mm,3.1mm) on Bottom Overlay And Track (3.9mm,3.1mm)(9.4mm,3.1mm) on Bottom Ove

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "BLON

KIN

LUBS" (9.4mm,3.1mm) on Bottom Overlay And Track (3.9mm,8.6mm)(9.4mm,8.6mm) on Bottom Ove

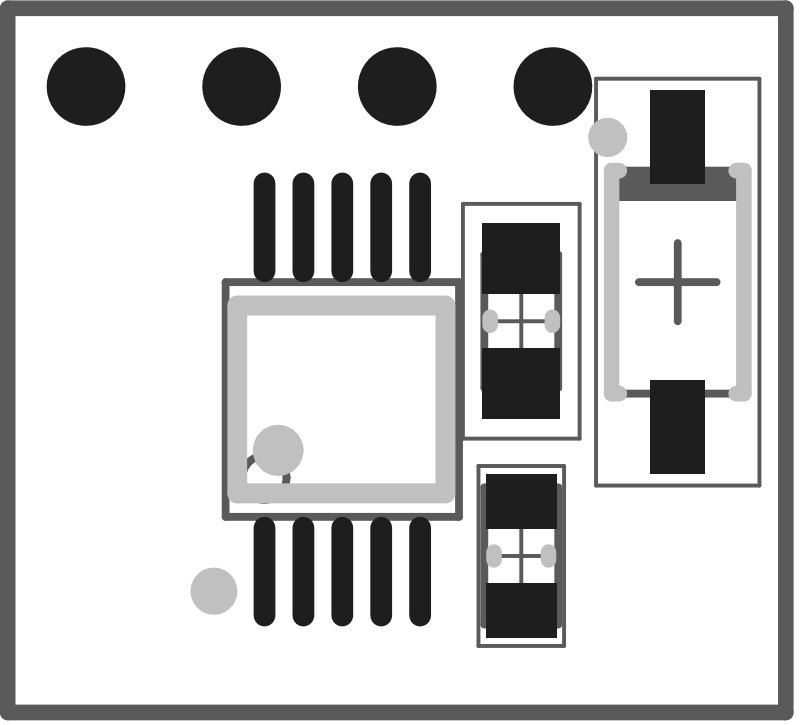
Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.253mm < 0.254mm) Between Text "BLON

KIN

LUBS" (9.4mm,3.1mm) on Bottom Overlay And Track (9.4mm,3.1mm)(9.4mm,8.6mm) on Bottom Ove

Electrical Rules Check Report

Class	Document	Message
Error	Sheet1.SchDoc	Net LED_OUT has only one pin (Pin U1-2)
Error	Sheet1.SchDoc	Net PUMP_IN has only one pin (Pin D1-1)



BLON
KIN
LUBS