Volume 1, Issue 1, February 1, 2016

TC-CCPS Newsletter

IEEE Technical Committee on Cybernetic for CPS

Founding Editorial

The continuous scaling of integrated circuit (IC) technologies has been driving the semiconductor industry for several decades. Nowadays, even though the scaling of mainstream CMOS technologies is starting to slow down, the field of VLSI circuits and systems continues its remarkable growth with numerous opportunities along two complementary avenues: (1) development of post-silicon devices, circuits and systems (e.g., carbon nanotube, graphene, memristor, etc.), and (2) discovery of emerging application domains (e.g., biomedical electronics, internet of things, etc.). The VLSI Circuits and Systems Letter, published twice a year, aims to report recent advances in VLSI technology, education and opportunities and, consequently, grow the research and education activities in the area.

This letter is affiliated with the Technical Committee on VLSI (TCVLSI) under the IEEE Computer Society. TCVLSI covers the design methodologies for advanced VLSI circuit and systems, including digital circuits and systems, analog and radio-frequency circuits, as well as mixed-signal circuits and systems. The emphasis of TCVLSI falls on integrating the design, computer-aided design, fabrication, application, and business aspects of VLSI while encompassing both hardware and software.

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1 Introduction and Motivation

In very large scale integrated (VLSI) circuit design, shrinking transistor feature size using advanced lithography techniques has been a holy grail for the whole semiconductor industry. However, the gap between the manufacturing capability and the design expectation becomes more and more critical for sub-28*nm* technology nodes Under the constraint of 193*nm* wavelength lithography, advanced circuit designs are vulnerable to many reliability issues, such as open/shorts, performance degradation, or parametric yield loss. There are several lithography techniques to overcome these issues [1]. In emerging technology node and the near future, multiple patterning lithography (MPL) has become the most viable lithography technique. Generally speaking, MPL consists of two different manufacturing processes: litho-etch type and self-aligned patterning type. In the longer future (for the logic node beyond 14*nm*), there are several next generation lithography options, such as extreme ultra violet (EUV), electron beam lithography (EBL), directed self-assembly (DSA), and nanoimprint lithography (NIL).

However, so far most of the DFM research are merely providing ad hoc solutions. That is, one specific work is targeting at one particular lithography constraint, and one work is hard to be re-used by another one where a new lithography constraint is involved. Therefore, CAD vendors may have to prepare a bunch of technical supports to these emerging design challenges. Recently there is a trend that different lithography techniques may combined to provide better printability. Due to such trend, in the near future, the situation may be even worse that more and more CAD tools and design supports are required.

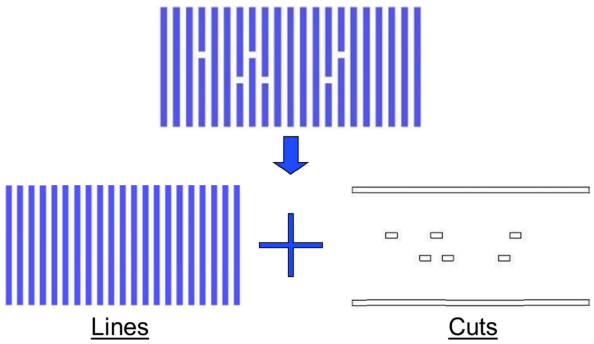

Figure 1: Regular design can be decomposed into lines and cuts [2].

Extreme regular design is a promising solution for DFM community to resolve the diverse design challenges [3]. Fig. 1 gives an example of such extreme regular layout [2], where we can see that the layout can be decomposed into line patterns and cut patterns. The benefit of such regularity is twofold. On the one hand, although various resolution enhancement techniques (RET) are utilized, random geometrical configurations are still hard to implement due to lithography limitation. Extreme regular style is able to improve the manufacturability and achieve manageable post-layout processing complexity. As shown in Fig. 1, the regular layout is the ease of splitting into line patterns and cut patterns. This allows independent process optimization of the line patterns and cut patterns. On the other hand, extreme regular design is naturally friendly to different emerging lithography techniques. For example, the cut patterns can be easily manufactured using EBL, DSA, or MPL.

References

[1] D. Z. Pan, B. Yu, and J.-R. Gao, "Design for manufacturing with emerging nanolithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 10, pp. 1453–1472, 2013.

[2] M. C. Smayling, "1D design style implications for mask making and CEBL," in *Proceedings of SPIE*, vol. 8880, 2013.

[3] L. Liebmann, V. Gerousis, P. Gutwin, M. Zhang, G. Han, and B. Cline, "Demonstrating production quality multiple exposure patterning aware routing for the 10nm node," in *Proceedings of SPIE*, vol. 9053, 2014.

The second news item

Author Name

References

[1] D. Z. Pan, B. Yu, and J.-R. Gao, "Design for manufacturing with emerging nanolithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 10, pp. 1453–1472, 2013.

[2] B. Yu, J.-R. Gao, D. Ding, Y. Ban, J.-S. Yang, K. Yuan, M. Cho, and D. Z. Pan, "Dealing with IC manufacturability in extreme scaling," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2012, pp. 240–242.

Technical Activities

Call for Contributions