VLSI Circuits and Systems Letter

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Editorial

The VLSI Circuits and Systems Letter is affiliated with the Technical Committee on VLSI (TCVLSI) under the IEEE Computer Society. It aims to report recent advances in VLSI technology, education and opportunities and, consequently, grow the research and education activities in the area. The letter, published twice a year, covers the design methodologies for advanced VLSI circuit and systems, including digital circuits and systems, analog and radio-frequency circuits, as well as mixed-signal circuits and systems. The emphasis of TCVLSI falls on integrating the design, computer-aided design, fabrication, application, and business aspects of VLSI while encompassing both hardware and software.

TCVLSI sponsors a number of premium conferences and workshops, including, but not limited to, ASAP, ASYNC, ISVLSI, IWLS, SLIP, and ARITH. Emerging research topics and state-of-the-art advances on VLSI circuits and systems are reported at these events on a regular basis. Best paper awards are selected at these conferences to promote the high-quality research work each year. In addition to these research activities, TCVLSI also supports a variety of educational activities related to TCVLSI. Several student travel grants are sponsored by TCVLSI in the following meetings: ASAP 2015, ISVLSI 2015, IWLS 2015, and SLIP 2015. Funds are provided to compensate student travels to these meetings as well as attract more student participation. The organizing committees of these meetings undertake the task of selecting right candidates for these awards.

This issue of the VLSI Circuits and Systems Letter showcases the state-of-the-art developments covering several emerging areas: radiation-hardened circuit, design for manufacturability, hardware IP protection, mixed-signal design and internet of things (IoT). Professional articles are solicited from technical experts to provide an in-depth review of these areas. The articles can be found in the sections of "Features" and "Opinions". In the section of "Updates", upcoming conferences/workshops (including their call for papers), funding opportunities and job openings are summarized. Finally, a dedicated section of "Outreach and Community" discusses the approaches for outreach with several successful stories.

We would like to express our great appreciation to all Associate Editors (Mike Borowczak, Prasun Ghosal, Shiyan Hu, Helen Li, Anirban Sengupta and Yiyu Shi) for their dedicated effort and strong support in organizing this letter. The complete editorial board information is available at: http://www.tcvlsi.org/vlsi-circuits-and-systems-letter/editorial-board/. We are thankful to our web chair Mike Borowczak, for his professional service to make the letter publically available on the Internet. We wish to thank Saumya Bhadauria, Anirban Sengupta, Bei Yu, Elias Kougianos and Prasun Ghosal who have contributed their professional articles to this issue. We hope that you will have an enjoyable moment when reading the letter! The call for contributions for the next issue is available at the end of this issue and we encourage you to submit articles, news, etc. to an associate editor covering that scope.

Saraju Mohanty
Chair TCVLSI and Editor
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Features

Multi-Cycle Single Event Transient Fault Security Aware MO-DSE for Single loop CDFGs in HLS

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Abstract – Multi-cycle single event transient (SET) fault security aware multi-objective (MO)-DSE for single loop CDFGs during behavioral synthesis has not received significant attention in the literature yet. Solving the aforesaid problem in the context of Control Data Flow Graph (CDFG) is non-trivial as it involves simultaneous generation of an optimal combination of multi-cycle fault secured datapath and loop unrolling factor satisfying conflicting user constraints (such as hardware area and delay). This paper solves the aforementioned problems with the following specific contributions: (a) a novel multi-cycle SET fault security aware MO-DSE methodology that explores an optimal combination of transient fault secured double modular redundant (DMR) datapath configuration and loop UF for CDFG (b) multi-cycle fault secured conditions (c) maintains trade-off between hardware area and delay as user constraints during exploration process. Finally, the proposed approach when tested on standard benchmarks yielded optimal solution which minimizes the fitness function and satisfies user constraints, besides achieving significantly reduced cost (improved quality) of the final solution when compared to a recent fault secured approach.

1. Introduction

The availability of faster devices is a feature of future technologies that induces major concerns to the fault detection community. For those technologies, even particles with modest linear energy transfer (LET) values will produce transients lasting longer than the predicted cycle time of circuits. Therefore the technology evolution and LET of particle impact both plays a major role in inducing multi-cycle (k-cycle) transient fault (longer duration transient) in a device [1, 2]. Therefore, fault security should be considered early in the design cycle as design objective, besides traditional design objectives such as area and delay during DSE. However, for CDFGs, due to involvement of loop unrolling factor, exploring its optimized datapath structure (based on user constraints) which is k-cycle fault secured, is non-trivial.

2. Related Work

There have been few works so far that have focused on solving multi-cycle transient fault security aware DSE for single loop CDFGs during behavioral synthesis. For example fault security approaches [3-6] did not deal with loop based CDFGs as well as appropriate insertion of cuts to optimize delay overhead, besides ignoring DSE of k-cycle transient fault secured datapath and loop unrolling factor for CDFG. Authors in [3] only duplicated the data flow graph (DFG) and mapped the copy onto the same hardware with addition of extra hardware as needed to achieve fault security property. In [5], a concurrent error detection (CED) scheme is employed to detect and isolate the faults within a system (circuit) while it is in use. In [6] authors investigated a method for exploring the trade-off between the area and latency of the CED design in HLS. The approach sometimes used hardware redundancy or time redundancy or a combination of both to produce fault secure designs. In [4] involves partitioning of the CDFG into regions or sub graphs. The authors presented a hardware redundancy based CED approach which breaks the data dependences between the nodes. This is done to improve the sharing between normal and duplicate computations. The original and the duplicate computations which are represented by a region are performed on distinct hardware. However, the proposed approach is significantly different than the existing approaches [3-6] as demonstrated through the following novelties: (a) Ability to handle multi-cycle transient fault detection for any candidate design solution (b) Ability to handle user area-delay constraints during exploration of double modular redundant fault secured system (c) simultaneous/integrated exploration of fault secured datapath configuration and loop unrolling factor.

3. Proposed Methodology: DSE Of k-Cycle Fault Secured Datapath

A. Mapping Process

The proposed methodology is shown in Fig 1 while the mapping process for PSO [7]. Details of Fig 1 will be discussed later in section C.

A. Proposed Evaluation Models and Formulation

1) Definition: Given a CDFG, explore the design space and find an optimal solution which satisfies the conflicting

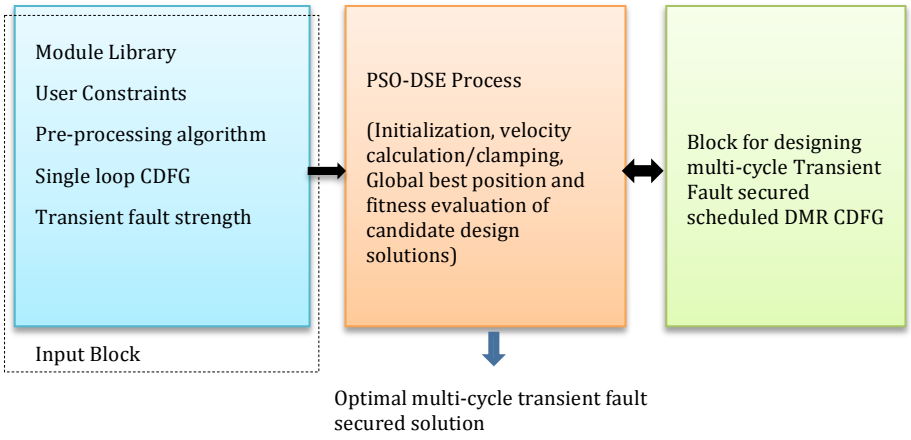

Fig. 1 Proposed Multi-cycle transient fault security Aware DSE during Behavioral Synthesis

user constraints and minimize the overall cost. The formulation is as follows:
Find: Optimal (X_i) = (R_x, UF_N)

With minimum hybrid Cost (A_T^{DMR}, T_E^{DMR})

Subjected to: $A_T^{DMR} <= A_{cons}$, $T_E^{DMR} <= T_{cons}$

and k_c transient fault constraint; (k_c: strength of the fault)

where, 'X_i' is a set comprising of resources combination and UF formally represented as:

$$X_i = (R_x, UF_N) = \{N(R_1), N(R_2), \ldots N(R_d) \ldots N(R_{D-1}), UF_N\}$$

where, '$N(R_d)$' is the number of instances of resource type 'R_d'; 'D-1' is the total number of resource types; UF_N is N^{th} unrolling factor; 'R_x' is an candidate resource combination; UF_N is an candidate UF; 'A_T^{DMR}' and 'T_E^{DMR}' are the area used by a fault secured Double Modular Redundant (DMR) system and execution delay of a fault secured DMR system respectively; 'A_{cons}' and 'T_{cons}' is area and execution time constraint specified by the user. (Note: X_i does not comprise of UF for DFGs).

2) Proposed Evaluation Models: In the proposed PSO-DSE, each particle position represents a resource set (R_x) in the design space..

a) Proposed Model for Execution Time: In order to describe the formulation of proposed execution time (T_E^{DMR}) (function of loop unrolling factor) for a CDFG, an example of loop unrolling is used shown in Fig. 2. Fig. 2(a) shows the original loop part of CDFG for FFT and Fig. 2(b) shows the same loop part unrolled twice. Fig. 3 shows As Soon As Possible (ASAP) scheduled CDFG DMR for FFT unrolled twice with resource constraint of 4(+), 2(*), 1(-) and 1(<); UF=2 and iteration count=4. It also shows the trailing loop part of the unrolled CDFG is not available for this case.
The generic execution delay model for a loop unrolled CDFG DMR is shown as follows [9]:

$$C_T^{DMR} = \left(C_{body}^{DMR} * \left[\frac{I}{UF} \right]^{floor} \right) + \left(I \bmod UF \right) * C_{first}^{DMR} \quad (1)$$

{Total CSs for unrolled loop} {Total CSs for sequential loop}

where, C_T^{DMR} is total CS required to execute the loop of CDFG DMR completely, C_{body}^{DMR} is the number of CS required to execute loop body of CDFG DMR once, 'I' is the maximum number of iteration (loop count), C_{first}^{DMR} is number of CS required to execute first iteration of the DMR CDFG. However, if the system design supports enough hardware instances such that sequential loops are possible to be fed to multiple hardware instances in parallel, then the total CSs for sequential loops from above eqn. (1) is: C_{first}^{DMR}. Finally, execution time for the system calculated as:

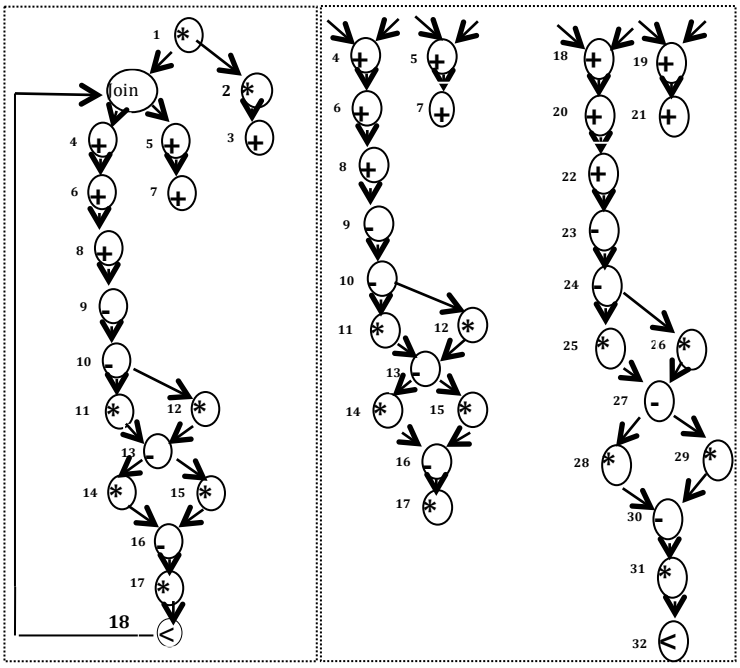

Fig 2(a) FFT loop Fig 2(b) FFT loop unrolled twice

$$T_E = \Delta * C_T^{DMR} \quad (2)$$

where, 'Δ' is the delay of one CS in nanoseconds.

b) *Area Model :* The total area consumed by a fault secured DMR system of a resource configuration and interconnect units (multiplexer and demultiplexer), denoted by 'A_T' is adopted from [1].

c) Proposed Fitness Function : A fitness function which is a normalized penalty function where the cost value obtained considers the constraints for area and execution time of DMR design is proposed as follows [9]:

$$C_f(x_i) = \varphi_1 \frac{A_T^{DMR} - A_{cons}}{A_{\max}^{DMR}} + \varphi_2 \frac{T_E^{DMR} - T_{cons}}{T_{\max}^{DMR}} \quad (3)$$

φ_1 , φ_2 = User defined weights for area and execution time which lies between 0 and 1. $C_f(x_i)$= Cost of particle

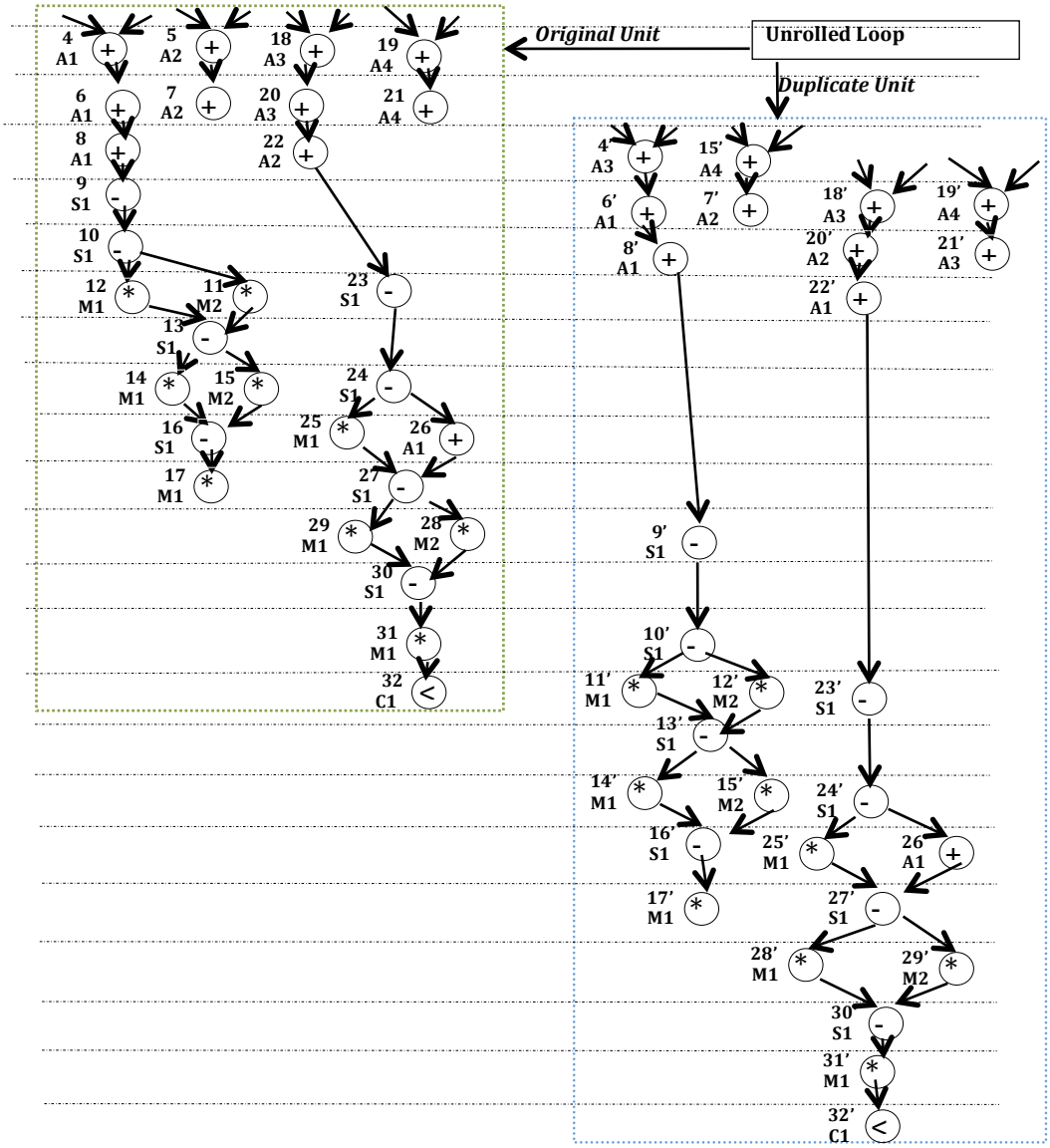

Fig 3: k_c-cycle fault secured SCDFG^{DMR} of FFT loop body for resource configuration(4(+),2(*),1(-),1(<), UF=2) at I=4 and k_c=2.
(adopted from [9])

denoted byX_i; T_{max}^{DMR} = Maximum execution time of a fault secured DMR system calculated using minimum resources and minimum unrolling factor (UF= Iteration Count); A_{max}^{DMR} = Maximum area of a fault secured DMR system calculated using maximum resources and maximum unrolling factor. Note: In our work, in order to provide equal priority to both area and execution delay, φ_1 , φ_2 = 0.5

B. Block Diagram of Proposed Methodology

The framework of the proposed multi cycle fault secured PSO-DSE for CDFGs is shown in Figure 1. The input blocks comprise of module library, behavioral description of CDFG, predefined user parametric constraints for area and delay as well as pre- processing of unrolling factors. The iteration count is provided as an input for the pre-processing block. Furthermore, the input block for control parameters comprises of acceleration coefficient, inertia weight, swarm size and terminating criteria which are used for regulating the PSO driven exploration process. These inputs are fed to the PSO-DSE block where following steps are done: a) Initialization and encoding of the particles b) velocity and position up-gradation c) velocity clamping and end-terminal perturbation d) Mutation e) Local best and global best positions are updated. To evaluate the fitness of a particle, each encoded particle is

passed through transient fault security block for designing a fault secured DMR scheduled control data flow graph ($SCDFG^{DMR}$) which is responsible for converting an untimed CDFG into a scheduled k-cycle fault secured CDFG DMR. After this process, appropriate cut for additional checkpointing (defined later in section C. d) is inserted based on proposed scheme to optimize delay overhead associated with fault security, followed by its fitness evaluation. Every such new design solutions (particle) obtained are again similarly convert it into a fault secured SCDFG Subsequently, the global best and local best solutions in the PSO process are also updated. This process continues until the terminating criterion is reached yielding an optimal fault secured datapath architecture (or SCDFG) which comprehensively satisfies the constraints of A_{CONS}, T_{CONS}, k_c and minimizes eqn. (5).

a) Pre-processing of Unrolling Factor: The code density of the $SCDFG^{DMR}$ increases with the increase in the unrolling factor, which in turn increases the sharing of resources (more number of multiplexers and demultiplexers) thereby increasing the area overhead. In such cases, the reduction in delay is marginal while the area overhead is much higher and thus the overall cost increases. Therefore, higher values of unrolling factor need to be carefully screened. This is accomplished by the pre-processing algorithm adopted from [7]. It filters unfit UFs to create a list of viable solutions.

b) *PSO-DSE Framework :* In this paper, the PSO-DSE framework [7] which explores the new design solution for feeding into the fault secured $SCDFG^{DMR}$ block. For a CDFG, the particle position 'X_i' of an 'i^{th}' particle is given as:

$$X_i = (N(R_1), (N(R_2),..(N(R_d).. (N(R_D), UF_n) \quad (4)$$

The proposed algorithm terminates when one of following condition holds true: When the maximum number of iteration have been exceeded (M = 100) or, S^1: When no improvement is seen in global best solution over '£' number of iteration. (£=10); S^2: If the population reaches to equilibrium state i.e. all particles velocity become zero ($V^+ = 0$).

c) Proposed Algorithm for Design of Multi-cycle Fault Secured DMR System: The process is responsible for designing a k_c cycle fault secured $SCDFG^{DMR}$. The algorithm takes three inputs a) Xi (particle position representing datapath configuration and loop unrolling factor) b) CDFG and c) fault security constraint (kc). The output of the proposed algorithm is a k_c cycle fault secured $SCDFG^{DMR}$.

The DMR system involves a scheduled control data flow graph ($SCDFG^{DMR}$), consisting of schedules of original unit (U^{OG}) and duplicate unit (U^{DP}). These units are concurrently scheduled following the As Soon As Possible (ASAP) scheduling algorithm. The user supplied resource constraints (indicated in Xi) and available dependency information of the nodes is taken into consideration while scheduling. After the scheduling of the DMR, hardware allocation is done for both units (U^{OG} and U^{DP}) taking the fault security conditions (schemes) adopted from [9], shown below:

i. Allocate $opn\ (v) \in U^{OG}$ and $opn\ (v') \in U^{DP}$ to distinct operators (hardware units) based on availability.

ii. If unavailable, then:
Keep same assignment for v'(as v) in U^{DP} such that:
$$t(v') - t(v) > k_c \quad (5)$$

iii. If above condition (eqn. 5) is false, then:
Push v' *(and its successors)* $\in U^{DP}$ one CS below until eqn. (5) is true.

If the rules proposed in the algorithm are not followed while allocating the hardware to $SCDFG^{DMR}$, then k_c cycle Transient Fault Hazards (TFH) can occur in between similar operations (of original and duplicate) assigned to same hardware unit i.e. TFH between similar operations belonging to a same hardware exists when:

$$t(v') - t(v) < k_c, \text{ where } v \in U^{OG} \text{ and } v' \in U^{DP}. \quad (6)$$

These hazards are resolved in the proposed algorithm by pushing the affected operation v' (and accordingly its successors) of the duplicate unit in later control steps, if allocation rules (i) and (ii) fail. The affected operation, v' is pushed until the interval between $v \in U^{OG}$ and $v' \in U^{DP}$ is greater than (or equals to) k_c. This resolution of the TFH is performed until the TFHs of the whole DMR system are resolved, i.e. $SCDFG^{DMR}$ obeys either of the fault security scheme.

4. Result and Analysis

Table I. Variation of exploration time with swarm size (S) in ms

Benchmark [8]	S=3	S=5	S=7
FIR	1216	1621	1853
FFT	3999	6370	7496
Differential	1819	1924	2415
MPEG MV	16482	24624	31604
ARF	17666	29993	43515
WDF	10911	17299	24781

Table II. Exploration time vs. inertia weight (at S=3)

Benchmark	Linearly decreasing(ms)	ω=0.5 (ms)	ω =1.0 (ms)
FIR	1216	1259	1514
FFT	3999	4810	4827
Differential	1819	1776	1872
MPEG MV	16482	17194	18484
ARF	17666	19670	18881
WDF	10911	11736	11624

Table III. Experimental results of the proposed approach for $k_c = 1$

Benchmark [8]	Final solution	A_c (area unit)	A_T^{DMR} (area unit)	Tc (us)	T_E^{DMR} (us)	Cost
FIR	2(+),3(*),1(<),UF=2	23058	16506	78.54	46.24	-0.208
FFT	2(+),2(-),4(*),1(<),UF=1	53739	36638	273.14	184.4	-0.218
Differential	1(+),2(-),5(*),1(<),UF=1	36379	24976	308.70	137.60	-0.262
MPEG MV	1(+), 4(*)	24000	13776	170	82.67	-0.240
ARF	1(+), 2(*)	15500	8092	220	178.7	-0.179
WDF	2(+), 2(*)	14000	10500	172	125.3	-0.196

i. Inertia weight linearly decreases from 0.9 to 0.1
ii. Acceleration coefficients initialized to 2.0 (as established in [7] in order to achieve faster convergence)
iii. Swarm size (S) is initialized to 3
iv. $\Phi_1 = \Phi_2 = 0.5$ in the fitness function.

Table IV. Experimental results of the proposed approach for kc = 4

Benchmark [8]	Final solution	A_c (area unit)	A_T^{DMR} (area unit)	Tc (us)	T_E^{DMR} (us)	Cost
FIR	1(+),4(*),1(<),UF=2	23058	16940	78.54	49.60	-0.189
FFT	3(+),2(-),3(*),1(<),UF=2	53739	36638	278.78	186.08	-0.222
Differential	1(+),2(-),6(*),1(<),UF=1	36379	27440	308.70	139.84	-0.238
MPEG MV	1(+), 4(*)	24000	13776	170	82.67	-0.240
ARF	1(+), 2(*)	15500	8092	220	178.7	-0.179
WDF	2(+), 2(*)	14000	10500	172	125.3	-0.196

v. Inertia weight linearly decreases from 0.9 to 0.1
vi. Acceleration coefficients initialized to 2.0 (as established in [7] in order to achieve faster convergence)
vii. Swarm size (S) is initialized to 3
viii. $\Phi_1 = \Phi_2 = 0.5$ in the fitness function.

Table V. Variation of proposed approach with [5]
Note: For proposed approach $\Phi_1 = \Phi_2 = 0.5$ in the fitness function

Benchmark	Final solution proposed	Final solution	Cost proposed	Final Cost ([5])
FIR	2(+),3(*), 1(<),UF=2	2(+), 4(*), 1(<),UF=8	-0.208	-0.121
FFT	2(+),2(-), 4(*),1(<), UF=1	4(+), 2(-),4(*), 1(<),UF=3	-0.218	-0.150
Differential	1(+),2(-), 5(*),1(<), UF=1	2(+), 2(-),4(*), 1(<),UF=4	-0.262	-0.123
MPEG MV	1(+), 4(*)	3(+), 7(*)	-0.240	-0.168
ARF	1(+), 2(*)	4(+), 2(*)	-0.179	-0.061
WDF	2(+), 2(*)	2(+), 2(*)	-0.196	-0.161

The proposed approach has been implemented in java language on Intel core i5-2450M processor with 3MB L3 cache memory and 4GB DDR3 primary memory. The processor frequency is 2.5 GHz. The results are discussed in four phases a) variation of exploration time with change in swarm size b) variation of exploration time with inertia weight c) results of the proposed approach in terms of area occupied and execution delay of the final solution along with its associated final cost d) comparison of proposed approach with [5] in terms of solution explored and final cost. Phase a) shown in Table I, presents the increase in exploration time with the increase in swarm size at the cost of no improvement

in the final explored solution. In other words, final solution explored is optimal for all different swarm sizes. However, exploration time increases due to increase in computation complexity per iteration. Further, the results of phase b), shown in Table II, presents the sensitivity analysis of various inertia weights with their associated exploration time values. For instance, exploration time for FFT is lesser in case of linearly decreasing inertia weight (from 0.9 to 0.1) as compared to constant inertia weight (w=0.5 and w=1). Similar trend is observed for other benchmarks. Phase 3 is demonstrated through Table III & IV which indicates that the results of proposed approach comprehensively meets the user constraints of area and delay as well as minimizes the hybrid cost function (eqn. 3) as specified in section *B* for both single cycle (kc = 1) and multi-cycle transient (kc = 4). Further, the solutions obtained for the tested benchmarks are real optimal solutions which were verified by comparing with the golden solutions found by exhaustive analysis (for sake of brevity further optimality details has been omitted). Finally, in phase d), the proposed approach has been compared with fault secured approach [5] in terms of final solution for faults secured DMR and its associated cost. Table V indicates the improvement in final solution cost of the proposed approach obtained over [5] for various benchmarks at kc = 1 (*Note: kc = 1 is only considered during comparison as multi cycle transient faults are not handled by [5]*). As evident, the cost of final solution found through proposed approach is significantly lower than [5].

5. Conclusion

A novel approach for multi-cycle SET fault security aware MO-DSE for single loop CDFGs during behavioral synthesis is presented in this paper. Results of proposed approach when compared to similar approach [5] indicated better quality solution within acceptable runtime.

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Design for Manufacturability: From Ad Hoc Solution to Extreme Regular Design

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1. Introduction and Motivation

In very large scale integrated (VLSI) circuit design, shrinking transistor feature size using advanced lithography techniques has been a holy grail for the whole semiconductor industry. However, the gap between the manufacturing capability and the design expectation becomes more and more critical for sub-28nm technology nodes. Under the constraint of 193nm wavelength lithography, advanced circuit designs are vulnerable to many reliability issues, such as open/shorts, performance degradation, or parametric yield loss. There are several lithography techniques to overcome these issues [1]. In emerging technology node and the near future, multiple patterning lithography (MPL) has become the most viable lithography technique. Generally speaking, MPL consists of two different manufacturing processes: litho-etch type and self-aligned patterning type. In the longer future (for the logic node beyond 14nm), there are several next generation lithography options, such as extreme ultra violet (EUV), electron beam lithography (EBL), directed self-assembly (DSA), and nanoimprint lithography (NIL).

Design for manufacturability (DFM), in conjunction with process integration challenges, are being actively research, to provide friendliness to these lithography techniques. For MPL, there are intensive investigations to solve layout decomposition, where the input layout is divided into several masks (e.g. [2–6]). Besides, some research work considers particular MPL constraints in early design stage, such as placement [7, 8] and routing [9–11]. For EUV, to migrate the mask blank defect, layout patterns are relocated to avoid the defect impact [12]. Also, related design constraints to avoid blank defect can be integrated into early physical design stage (e.g. [13]). For EBL, since its key limitation is the low throughput, many approaches have been developed to improve the system throughput [14–16]. For DSA, how to design and verify the guiding template patterns, which form DSA holes insides, have been investigated in [17] and [18], respectively.

However, so far most of the DFM research is merely providing ad hoc solutions. That is, one specific work is targeting at one particular lithography constraint, and one work is hard to be re-used by another one where a new lithography constraint is involved. Therefore, CAD vendors may have to prepare a bunch of technical supports to these emerging design challenges. Recently there is a trend that different lithography techniques may be combined to provide better printability (e.g., MPL+EBL [19] and MPL+DSA [20]). Due to such trend, in the near future, the situation may be even worse that more and more CAD tools and design supports are required.

Extreme regular design is a promising solution for DFM community to resolve the diverse design challenges [21, 22]. Fig. 1 gives an example of such extreme regular layout [23], where we can see that the layout can be decomposed into line patterns and cut patterns. The benefit of such regularity is twofold. On the one hand, although various resolution enhancement techniques (RET) are utilized, random geometrical configurations are still hard to implement due to lithography limitation. Extreme regular style is able to improve the manufacturability and achieve manageable post-layout processing complexity. As shown in Fig. 1, the regular layout is the ease of splitting into line patterns and cut patterns. This allows independent process optimization of the line patterns and cut patterns. On the other hand, extreme regular design is naturally friendly to different emerging lithography techniques. For example, the cut patterns can be easily manufactured using EBL, DSA, or MPL.

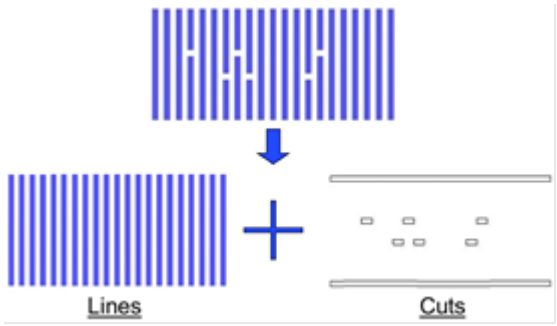

Figure 1: Regular design can be decomposed into lines and cuts [23].

2. Current Research for extreme Regularity

a. Standard Cell Design Stage

Standard cell design is a critical stage for providing overall layout regularity. There have been some cell synthesis works for regular standard cells [24–27]. However, while the yield and performance benefits of regularized layouts may be well accepted, the biggest barrier to broader implementation of regularized layout styles is the perceived impact on layout density and intra-cell routability [28]. Recently, a Tungsten-based middle of line (MOL) structure is introduced to

connect intra-cell transistors [29]. MOL structure is made up of two different local interconnection layers, CA and CB (sometimes called IM1 and IM2, respectively), where the CA layer is used as a connection layer for active fins and better landing for the contacts in active region, while the CB layer is mostly used for via landing and gate shortening [30].

Ye et al. [31] studied the problem of cell layout regularity optimization under MOL structure. Fig. 2 gives an example of the proposed cell optimization, where the input 2D cell in older technology node is shown in Fig. 2(a), while the optimized unidirectional cell is in Fig. 2(b). Due to the unidirectional shapes of MOL and Metal-1 layers, the patterns are SADP friendly. That is, the line-space array decomposition can be applied to SADP with trim masks, with tight control on overlay and wafer-print artifacts. A general integer linear programming (ILP) formulation is proposed to solve the unidirectional cell optimization under MOL structure. Besides, a set of hybrid techniques is presented to search for high quality cell optimization solution.

For regular layout design, several works have been done on the investigation of contact layer fabrication and contact layer optimization. Yi et al. [32] demonstrated the fabrication of regular standard cell contacts using DSA process. Besides, Du et al. [17] proposed a contact layer optimization method. By assigning cost function to different DSA templates based on their manufacturability, they optimized the DSA aware contact layer. Recently, Ou et al. [33] performed a comprehensive investigation on the DSA based end-cutting problem, where a mathematical formulation is proposed to search for minimum wire extensions and minimum conflicts for all test cases.

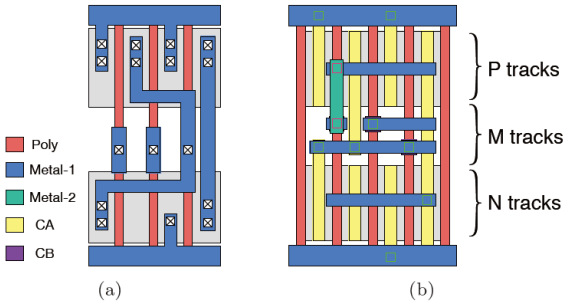

Figure 2: Example of cell regularity optimization in [31]. (a) The input layout with ten tracks. (b) The optimized layout with nine tracks.

b. Detailed Routing Stage

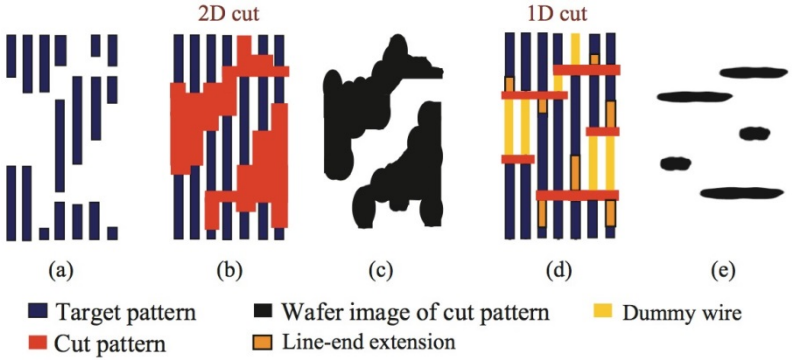

Figure 3: The 1D target patterns in (a) can be formed by a 1D nanoarray with (b) 2D irregular or (d) 1D regular line-end cut patterns. (c) The wafer images of 2D irregular cut patterns suffer from distortion and degrade the printability of line ends. (e) The wafer images of 1D regular cut patterns have better line-end printability [35].

Detailed routing aims at pin access and search for exact routes of each net. A typical detailed routing strategy performs pathfinding of the nets sequentially. [34, 35] proposed a comprehensive framework to explicitly address the regular routing under regular layout constraints. Fig. 3 illustrates an example of such regular detailed routing result. The wafer image quality of irregular 2D line-end cut patterns in Fig. 3(c) suffers from more severe pattern distortion than that of 1D cut patterns in Fig. 3(e) [35].

3. Further Work

There is a large amount of emerging design challenges, along with the regular design style. In the following three of them are listed.

- Firstly, due to limited local routing resources and dense I/O pins, pin access is still a serious problem for detailed routing. To overcome the local congestion problem, physical design tools should be aware of the congestion derived from the dense I/O pin cells. For instance, in placement stage local congestion mitigation can be applied to prevent placing hard-to-routed cells too close together [36]. More importantly, the standard cell library should be carefully designed to enhance the pin accessibility. That is, I/O pins need to be balanced distributed within a cell, as the alignment or the densely packing of pins make the cell more difficult to be accessed.
- Secondly, under regular design style, although the printability and yield is improved, one standard cell may suffer from area and timing penalty. How to optimize the cell layout while timing constraints are satisfied is a critical problem.
- Thirdly, a coherent physical design framework is imperative. Although there are some attempts on extreme regular routing (e.g. [34, 35]), how to handle the extreme regular design style across the placement and routing stage is still an open problem.

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Opinions

Protection of Reusable IP core at Architectural Level

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I. Introduction

Reusable intellectual property (IP) cores have become affordable solution in system-on-chip (SoC) designs to combat the conflicting demands of maximizing productivity in concurrency with minimal design time. This leads to future design challenges of tremendous complexity with reduced time to market. In this goal of optimizing orthogonal demands during SoC design, globalization plays a critical role. However, the global SoC design supply chain may manifest itself into unwanted attacks/compromise/counterfeit. Therefore, designing a trustworthy /secured IP which has capability to protect authorship is instrumental in confronting anti-piracy. Intellectual property cores must have sturdy protection technique to preserve its value i.e. IP cores should come along with robust ownership protection scheme to prevent ownership conflict in situations such as IP piracy. This article discusses/reviews two major protection mechanisms for reusable IP core at architectural level used in system-on-chip (SoC) [1,2].

2. IP core Protection Mechanisms

[I] Watermarking for IP protection at Architecture Level

A. Target Technology

The watermarking approach for IP protection is applicable to the current IP development tool infrastructure. Current watermarking methods can be easily adopted by current and future set of design tools which uses either hardware description language (HDL) or high level language for IP generation. In other words, the current watermarking methodology applies to the protection of both hardware and software IP [3].

B. Dynamic Watermarking Method

For the purpose of embedding a watermark, signature insertion as additional constraints needs to be imposed in the design during one of the architecture level design steps. In the recent approaches for inserting the additional watermarking constraints, an architectural synthesis step of IP design may be register allocation or scheduling. The concept of colored interval graph is used for register allocation during architectural synthesis, where the nodes of the graph represents the storage variables and the edges represent the existence of overlapping lifetime between variables. In other words, if the lifetime of two variables overlaps, then there will be an edge between the same. Having an edge between two storage variables of a colored interval graph indicates that a common register cannot be allocated for storing the two storage variables. Any number of additional edges (additional constraints) as signature may be added in the register allocation step [3,4]. The more the number of edges (constraints), greater is the security of the signature, more robust is the watermark. The respective storage variables of a colored interval graph are forced to execute through distinct registers based on the additional edges added as watermarking constraints. However these additional watermarking constraints have to be specified through owners' hidden signature. Therefore it becomes necessary to design a robust signature scheme and strong encoding mechanism. The signature of the owner (author) selected comprises of a random bitstream of 1s and 0s which remains in encrypted cyphertext format using RSA technique for data security. The bitstream is interpreted as follows: For each bit of the watermark, the terminal node is chosen such that the terminal node represents the bit value. Now decoding of the signature value to represent watermarking constraints is to be performed. First, all nodes of the colored interval graph are first sorted and numbered in increasing order of their lifetimes. Each node from left to right of the sorted order is considered for embedding a single bit. To embed a 1, the terminal node of the added edge should have an odd number, while to embed a 0 the terminal node of the added edge should have an even number [3,4].

Any watermarking scheme mandates inclusion of signature detection process. Signature detection is accomplished by a two step process:

a) *Reverse Engineering*: This phase intends to collect relevant information of the received IP in terms of structural property, specifications etc required to re-construct the controller design back.

b) *Signature Verification:* This step intends to verify the presence of owner signature in the received IP design. In order to perform the verification, firstly, the receiver needs to decrypt the cypher text using valid cryptographic key. On decryption, the encoded signature is decoded using the knowledge of the encoding rules. Finally, the additional constraints as watermark is available to checking its presence in the reverse engineered controller design. If the design indicates presence of additional constraints, then the received IP is genuine and valid, otherwise, the IP received is not from an authentic source [3].

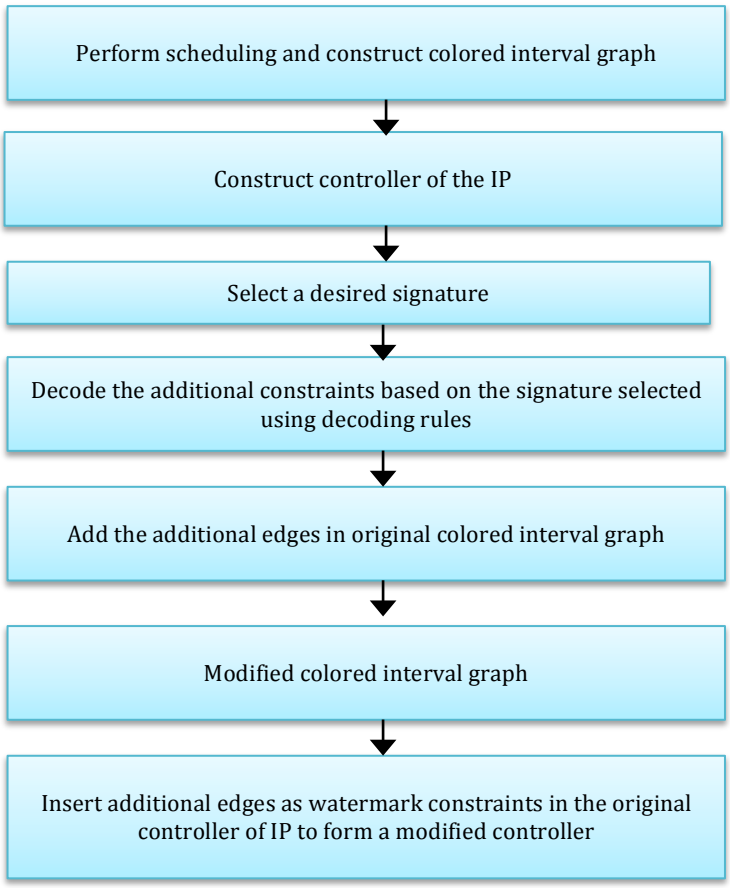

Fig.1 Watermarking at architectural level

[II] Metering for IP Protection at Architectural Level

A. Target Technology

Hardware metering is applicable to any IP vendor which provides IP to chipset manufacturers or system on chip integrators. Further like watermarking, metering can be easily adopted by any design house.

B. Hardware Metering Method

Hardware metering is performed by making a small part of the design programmable during configuration time. For each manufactured chip this small portion is configured in a unique way. Different configurations may be obtained by making different implementations of scheduling or register allocation during architectural synthesis. This allows proper control of the IP royalties by the IP providers. This is because since each

manufactured chip is configured its unique way, hence such each manufactured chip or software release has a unique ID associated with it. It becomes straightforward for the IP vendors to enforce royalty for each such manufactured chip or software release. Let us take an example: In hardware metering, if a foundry produces 'n' chips who IDs are not reported to the design house, and say it produces 'p' chips who IDs were reported to the design house, then in such a case, the probability that a random chip has non-approved ID is n/(n+p). Hence only a few tests would be able to detect an unauthorized chip produced by the foundry. Another naïve and straightforward hardware metering approach would be to just add an extra piece of programmable memory that carries the ID of the manufactured chip or addition of an extra identification mark of the software. This incurs area overhead compared to the first hardware metering technique discussed, as in the first case the ID is programmed within the design. Secondly, in case of the first approach, reverse engineering is difficult, as the unique configuration is programmed within the design in contrast to a disconnected piece of memory [5].

Hardware metering is implemented as follows: First the scheduling of the application is performed using standard algorithms such as soon as possible (ASAP). Once scheduled, the scheduling contains the storage variable information. Lifetime evaluation of each storage variable is determined and a colored interval graph is constructed. The nodes of the colored interval graph represent the storage variables while an edge between two nodes may only exist if their lifetimes overlap. The colored interval graph represents the minimum number of registers required for allocation. Assigning two variables to same registers indicate that the two variables have a common color. There can be many potential colored interval graphs depending on the register assignment chosen for the storage variables. However, the key point is that the number of registers required to implement does not change. Further, the datapath also does not change; the only thing that changes with change in register assignment is the information of control unit (FSM). So for any alternative graph coloring, the datapath remains constant (including same minimum number of colors) with only small change in control unit. Hence the mask can be kept same for each layout. Since the control unit represents a very small segment of the total mask, hence it can be implemented as an EEPROM. This EEPROM need not be configured during mask but can be configured later. Thus each manufactured chip is inserted with a unique ID by keeping the same datapath but configuring the control unit in a different way i.e. through different scheduling or register allocation of variables [5].

Finally, we conclude the discussion of metering of IPs by providing a typical example where metering plays a very important role. Say company 'X' builds a system that outperforms all similar products in the market. No 'X' gives the HDL description of the system to company 'B' who is responsible for its manufacture. 'X' enters into an agreement with 'Y' to manufacture 5 million copies of it. The first 1 million copies are sold out very quickly, however, the sales slows down after that indicating saturation. 'X' lowers the price due to this. Meanwhile market survey shows 7 million similar products in use in the market. In this scenario, 'X' is suspecting that 'Y' has violated their agreement, however due to lack of evidence, suffers from loss in R&D revenue. In such cases metering of IP by providing unique ID number for each product would have helped to figure out unauthorized copying. No sooner two products with same ID number would have been found, and then unauthorized copying is evident [5].

3. Conclusion

This article reviewed the major reusable IP core protection mechanisms useful in chipsets such as JPEG encoder used in camera processor IP, MPEG in HDI, as well as other applications such as IDCT used in set-top boxes (STBs). Watermarking and hardware metering at architecture level are the well-known schemes used for reusable IP core protection which has its own advantage and disadvantages. For example, watermarking is more vulnerable to threats than metering due to inclusion of reverse engineering involved during signature detection. Secondly, for watermarking, the chances of hardware overhead is more than hardware metering since, metering only reconfigures a small portion of controller. On the contrary, the flip side is, if the signature employed in watermarking is double layered protected (with strong encoding and encryption), then it is almost impossible to compromise the watermark by an attacker. Moreover, watermarking techniques employed at architectural level provides fault tolerance if the watermark constraints are uniformly distributed throughout the IP design. This is because removal/tampering of some portion of the watermark will still enable protection of the IP authorship.

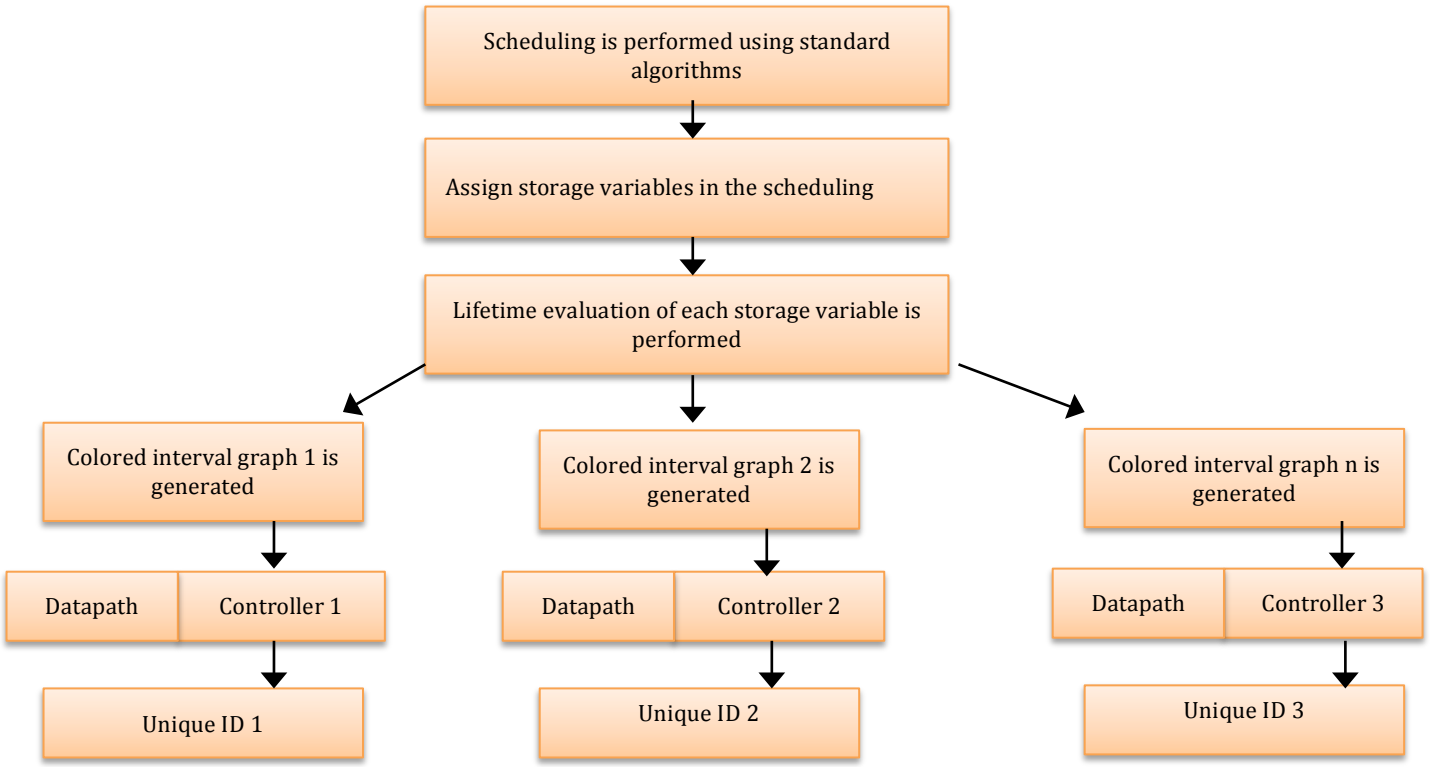

Fig.2 Hardware metering at architecture level

In terms of future research in this area, advanced signature encoding schemes are required that provides robust protection against attacks. Additionally, ways to mitigate watermark embedding cost needs to be investigated. Finally, other architectural synthesis steps may be used for inserting hidden signature for creation of quality watermark, such that minimal area overhead occurs.

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Nanoelectronic Mixed-Signal System Design Book Review (ISBN: 978-0-07-182571-9)

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Teaching traditional Integrated Circuit (IC) Design at the senior and graduate levels has been sharply divided into a very large set of "pure" digital VLSI courses, represented by numerous well-established textbooks, and a much smaller set of analog IC design courses (notice the absence of "VLSI") most commonly at the graduate level, supported by a very small

number of textbooks. The intersection of these sets, commonly known as "Mixed-Signal" or "Analog/Mixed-Signal" (AMS) design, has received even less attention. There are only a handful of textbooks, some at very advanced level and some being collections of loosely connected chapters or papers. On the other hand, all IC design these days is AMS by virtue of the device physics involved and the systems themselves: pure digital systems, even though still tremendously useful for computation, do not reflect daily usage of commodity electronics dictated by our connected society.

The book Nanoelectronic Mixed-Signal System Design amply fills this gap by covering a vast array of topics related to AMS IC design. The book covers the entire spectrum of modern IC technologies, from the design and simulation point-of-view, starting at the schematic level and progressing through to actual physical design, including post-layout simulation and design optimization. The audience for this massive and authoritative treatise is eclectic in its scope (those interested in AMS IC design, particularly at the nano level) but at the same time addressing the needs of everyone in that scope: seniors, Master's and PhD students as well as engineers and practitioners. Because of the immense and state-of-the-art amount of material covered, it can be used both as a textbook and reference book at the same time.

The author is a professor of Computer Science and Engineering at the University of North Texas, Denton, TX. He is the founder of a laboratory dedicated to the subject of nanoelectronic AMS IC design, the Nano-System Design Laboratory (NSDL), he has published over 170 papers on the subject and has co-authored or edited six other books, mostly in the same area. He has over 15 years of undergraduate and graduate teaching experience in the US and it shows in the structure and style of the book. As the author mentions in the preface (p. xxiii) "The author's objective is to provide nanoelectronic very large-scale integration (VLSI) design training requiring the shortest possible learning curve." In the opinion of this reviewer, this objective is accomplished admirably in the book.

The terms "comprehensive", "massive" and "treatise", already used to describe the book in this review are not unjustified. At a very large 8.5" × 11" page size and almost 800 pages of dense text, combined with hundreds of figures, diagrams, plots and over a thousand references, there is very little not covered on the subject. The book has 12 chapters and includes a very handy 8-page table of acronyms and a 4-page table of symbols. Each chapter is concluded by a large number of questions and references. Although not formally divided into sections, the book can be considered as covering four wide areas.

The first area consists of chapters 1 through 3 and provides a general overview of the subject. Specifically, chapter 1 discusses the state-of-the-art in nanoelectronic technology. Chapter 2 provides numerous examples of nanoelectronic systems used in our daily life and provides the justification for the need of a paradigm shift when studying the subject. Chapter 3 introduces gently the subject by providing a high-level overview of the design process with special emphasis on nanoelectronic-specific issues such as process variation, power and leakage concerns for battery-operated systems and the effect of post-layout parasitics and effects on the operation of the systems.

The second area is covered in chapters 4 through 7 and gets into the heart of what comprises a nanoelectronic system: its constituent components and subsystems. Chapter 4 discusses the all-important "heart" of a system, namely oscillators and phase locked loops (PLLs). This chapter by itself can serve as a general introduction to the subject. Coupled with the more than 100 references cited in this chapter, it becomes a true reference work. In the same spirit and style, chapter 5 covers analog-to-digital (A2D) and digital-to-analog (D2A) conversion, the primary characteristic of a mixed-signal system. Chapter 6 provides an extensive survey of sensors both at the circuit and system level. Finally, chapter 7 rounds up the system component concentration by describing all major memory types used in today's systems.

The third area builds on the material covered in the previous area and is focused on mixed-signal system design, simulation and post-layout re-simulation. It consists of chapters 8, 9 and 10. Chapter 8 follows a tutorial approach to mixed-signal system design and attempts to "lucidly discuss all the steps". This is accomplished by an impressive set of flowcharts, diagrams and examples that succeeds in this difficult objective. This particular chapter will be of great help to those trying to understand the jargon of modern IC design. Chapter 9 covers simulation from all possible viewpoints: from transistor-level continuous time SPICE analysis, to discrete-event behavioral simulation using hardware description languages (HDLs) to the commonly used today mixed frameworks that incorporate both types of simulation. A unique feature of this chapter is the inclusion of the widely used MATLAB® and Simulink® frameworks for exploratory system space exploration using novel and untested technologies. Chapter 10 re-examines the subject covered in chapter 8, namely

circuit and system simulation but from the physical point of view. Parasitic effects as well as power and thermal issues are discussed in depth.

The last area, covered in chapters 11 and 12, offers a unique perspective to what this reviewer considers to be the future of AMS simulation: variability-aware, metamodel-based design methodologies, an area where the author has published extensively and is recognized as one of the major contributors on the subject. Chapter 11 sets the stage for what follows in the culminating chapter 12 by analyzing techniques that have been used to address variability inclusion in the design, simulation and design optimization stages. Along with Monte Carlo and similar stochastic techniques, the very recently introduced (at least in AMS system design optimization) swarm methods are examined. Finally, chapter 12 integrates the whole book by looking at complex systems, analyzed through the methodologies presented in previous chapters, and modeled using metamodeling approaches such as classical polynomial and neural network models and the novel concepts of Kriging as applied to this field.

On the whole, the book succeeds in addressing the vast array of topics comprising the subject matter (mixed-signal system design in the nano regime) in a very approachable, intuitive and clear manner. Students, practitioners and instructors will find this book an invaluable resource for teaching or reference.

IoT: the Internet of... "Everything"?

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I. What is IoT?

Today's internet of approximately 4.9 billion things [7] is expected to touch the figure of around 25 billion by next five years only [2, 7]. With incredible growth of internet and internet users, the concept of ubiquitous computing is not a myth anymore, but it's being built today. Starting from 60's to present day we have experienced www (static web), and web2 (Social Network), and now we are at the doorstep to the actual web3 (ubiquitous network). The Internet of Things (IoT) is the most promising candidate to bring the concept of web3 in reality. As per the speculation of researchers, machine to machine, machine to infrastructure, machine to environment, the Internet of Everything, the Internet of Intelligent Things, intelligent systems— all is possible under the framework of *Internet of Things* [IoT]. IoT aims to unify everything in our world under a common infrastructure, giving us not only the control of things around us, but also keeping us informed about the state of the things.

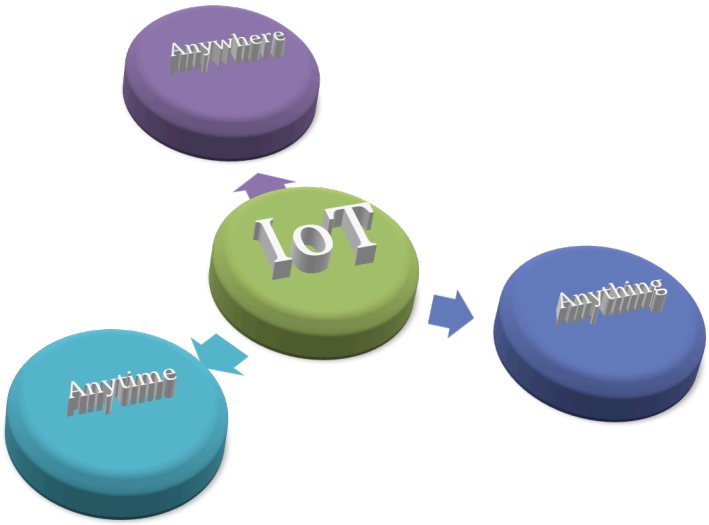

Figure 1: Ubiquitous network

II. Ubiquitous Computing and IoT

The word 'ubiquitous' has been originated from a Latin word 'ubique' meaning 'everywhere' [1]. From IoT perspective we can see it as 'anywhere'. Concept of IoT is based on three pillars viz. *Anything, Anywhere* and *Anytime*. So formally we may define IoT as *it is a network of interconnected 'things' where anything can communicate with any other at any time*.

The phrase IoT contains two words viz. *internet* and *things*. The word 'internet' implies the inter-connection of computing devices and 'things' refers to any uniquely identifiable device (with unique address). Computers, mobile phones, sensors, actuators etc everything can perform as a thing in IoT. The vision of IoT is to connect each and every object in this planet and thereby utilise the enormous capability of internetworked knowledge base during their operations. It's not about how to add a particular service to a specific product, but to turn the signal / information generated by several sensors, devices, things and services to some meaningful knowledge about the environment and thereby to initiate some meaningful action. All the devices can be monitored and can be controlled overseas in real-time manner, if required. RFID tagging, sensor technology, networking, and nano-scale computing are taking major roles to enable IoT in reality.

III. Enabling Technologies

To meet the vision of IoT properly we need to bring different technologies under one roof. Primarily five technologies are taking major roles to construct an IoT enabled service.

Ubiquitous ID: To connect an object in a network we must need a unique address. Statistics show that some trillions of things are coming under IoT in next few years [2]. A big problem will arise due to the fact of allotting these enormous numbers of objects with unique addresses (ubiquitous id) using the present standard IPv4 (Internet Protocol version 4). This 32bit addressing can only generate billions of unique addresses. Solution is to use the IPv6 addressing (128 bit address) where more than 3.4×10^{38} unique addresses are available to identify a trillion objects each day for trillion years, and still there will be few available as unused [3].

RFID Tagging: The idea of Radio Frequency Identification (RFID) was first introduced to replace traditional barcode technology in 1973 to overcome some of its limitations. But slowly it has become a major pillar in IoT because of its automated and wireless nature. RFID is an automated data transmitting 'thing' that uses radio frequency to transfer data. RFID technology requires three elements viz. RFID tag, RFID reader, and middleware. There are mainly two types of RFID tags available e.g. Passive tags and Active tags [1]. The RFID tag contains a very small chip that stores data about the object that is tagged and an antenna to transfer data. Passive tags do not have any inbuilt power supply. It uses

electromagnetic induction from the reader to activate. The reader collects data from the tag and transfers them to the base station. Successful use of RFID can be seen in the shopping malls, manufacturing companies, smart homes, hospitals, libraries etc.

Transducers: Transducers are devices able to transform energy from one kind to another. Mainly two types of transducers are used in IoT technology, sensors and actuators. Sensors monitor the physical phenomenon of the system and actuators impose any action on the system. Sensor technology and wireless sensor network take leading role to enable IoT. Sensor sends data about the environment over the sensor network to the base station in real-time basis. Applications of sensors in IoT can be seen in weather forecasting, chemical plants, patient monitoring systems and so on.

Smart Technology: Intelligent software and hardware are used to make IoT a smart system. Machine automation technology is used to react with actuators accordingly with the environment. Today's smart devices are clubbed to IoT systems to achieve its ultimate goal.

Nano-scale Computing and System Design: Nano technology acts as a shrink in IoT. The things are getting smaller and smaller to near microscopic elements in IoT. Integrated IC, NoC, SoC etc are taking major role to manufacture powerful integration of systems. Nano computing provides the opportunity of design complex, integrated, and microscopic devices to manufacture IoT enabled things.

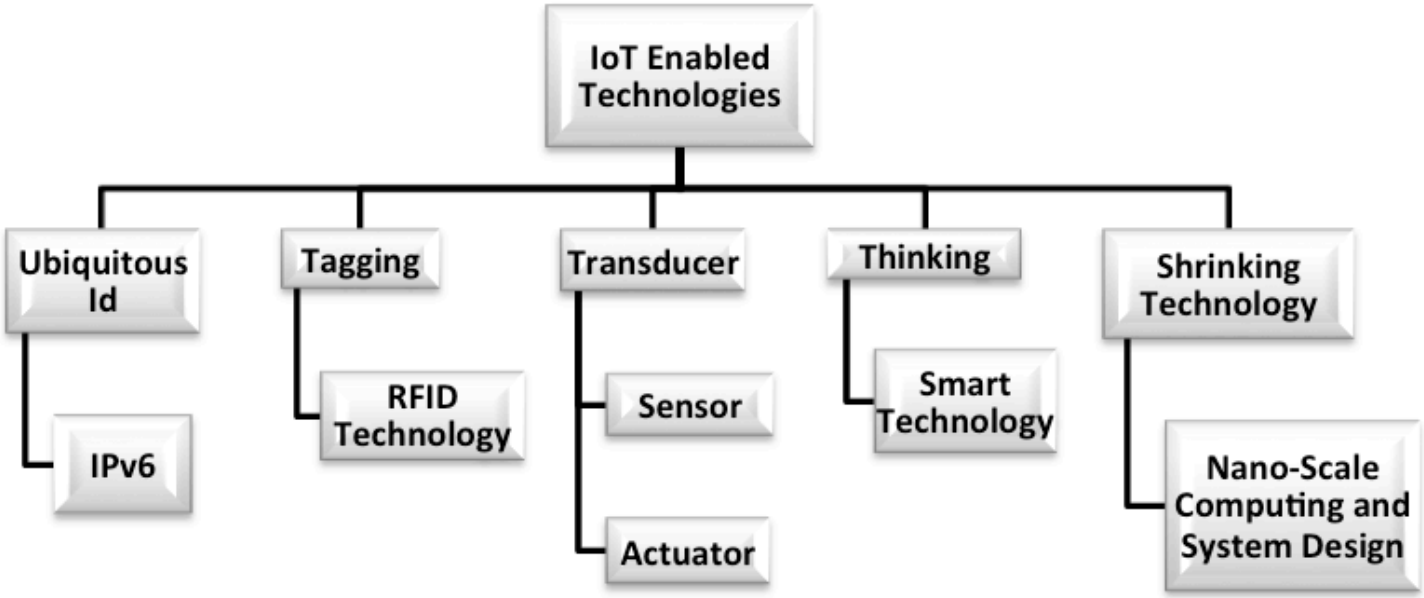

Figure 2: IoT enabled technologies [1]

IV. APPLICATIONS OF IOT

There are countless applications of IoT enabled technologies [4]. Few of them are discussed here.

Health Care: A revolution in the medical science can be achieved with the help of IoT technology. A doctor can receive continuous information of patients' physiological functions from the patient monitoring system in real-time basis and can assist the local doctors or control the local actuators in emergency situations from overseas.

Weather Forecasting: Continuous environmental information can be gathered continuously over the IoT network from the weather detecting sensors and can be forecasted to the citizens all the time.
Traffic Management: Intelligent traffic control system can be achieved from real-time traffic monitoring system.

Crowd Management: Emergency situations due to crowd can be handled from the crowd flow monitoring systems in stadiums, theatres, or railway stations.

Security and Surveillance: There are revolutionary applications of IoT in security and surveillance system. The security systems of our home and office can be under surveillance from anywhere over the network using IoT enabled devices.

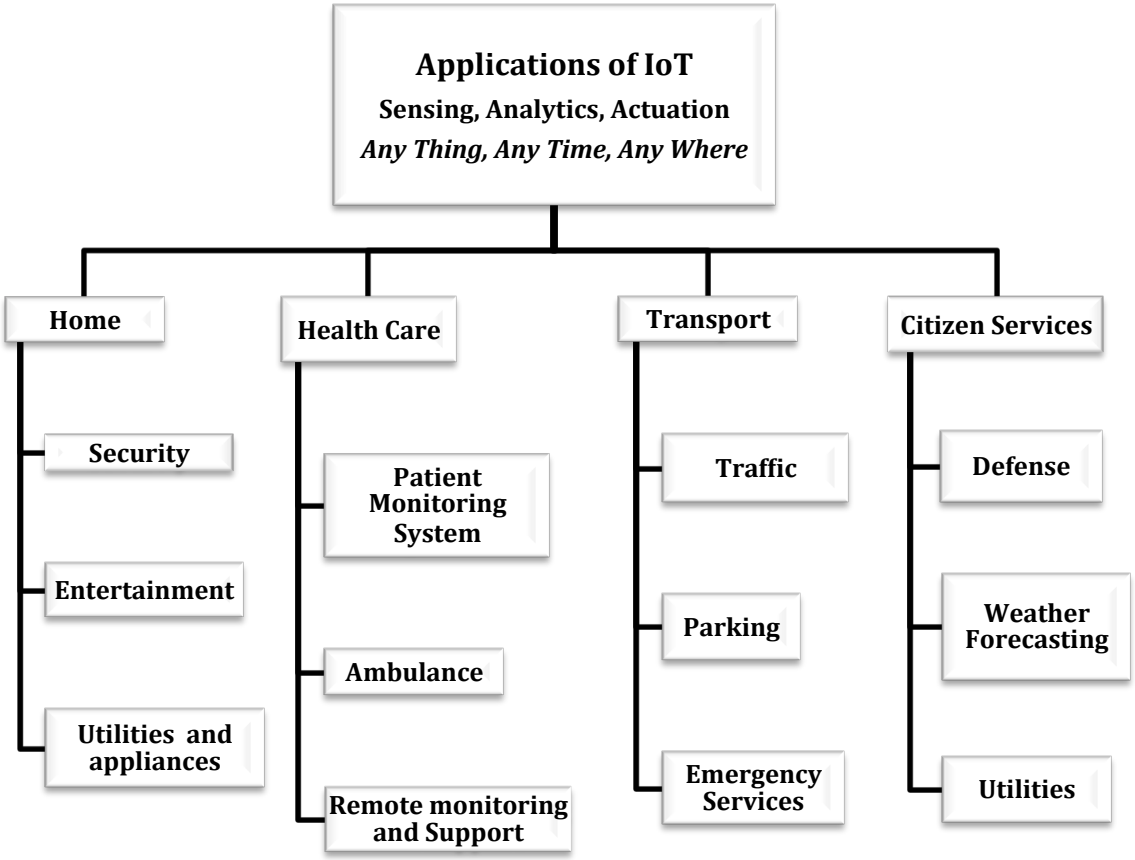

Figure 3: Applications of IoT

V. Challenges and Research Opportunities in IoT

IoT is a big concept in communication centric computing perspective. And big ideas always have big challenges. Countless technologies need to be clubbed to implement the actual aim where all of them come with different technological background. To merge all those technologies we need to face various challenges. The spectrum of research required to achieve IoT at the scale envisioned above requires significant research along many directions. Some are discussed below.

Heterogeneous set of Things: An IoT enabled system runs with several heterogeneous devices those are different to each other in terms of communication protocol, data format, data collection, data storage capability etc. This is a challenging task to develop communication protocols supported by all devices. Standard data format is required to enable machine to machine (M2M) communication more efficiently.

Energy: Most of the devices in IoT are wireless in nature and live in remote places (e.g. environment monitoring sensors) where energy is the most vital issue. We need ultimate energy efficient algorithms and hardware.

Security: Unlike any online system, security is one of the most important issues. This issue becomes more challenging In an IoT when we are using the network ubiquitously. We require specific data isolation techniques to provide proper

privilege to the end users according to their authority. Data encryption algorithms need to be much stronger. Most importantly, it should be energy efficient so that they could be used in very low power, low energy devices.

Privacy: The ubiquity and interactions involved in IoT can provide many conveniences and useful services for individuals, but also create many opportunities to violate privacy. To solve the privacy problem created by IoT applications of the future, the privacy policies for each (system) domain must be specified. Once specified either the individual IoT application or the IoT infrastructure (e.g., the utility capability) must enforce privacy. Consequently, the IoT paradigm must be able to express users' requests for data access and the policies such that the requests can be evaluated against the policies in order to decide if they should be granted or denied. A new language is required to express privacy policies.

Intelligence: Machine to machine (M2M) communication has high priority in IoT because machine automation must be improved to minimise delay, traffic, and immediate action. Smart technologies need to be more intelligent to enable automated systems.

Communication Protocol: The heterogeneous nature of IoT enabled services meet an unavoidable problem with communication protocols [5]. Each types of device use separate protocol in terms of data communication. Standard communication protocol needs to be developed for successfully implement IoT services.

Real-Time Solution: It will be really tough to implement the 'Anytime' concept of IoT in reality. The real-time systems need to be implemented in grass root level of the IoT things to react prominently at anytime. The complexity of the existing real-time systems must be minimised, so that they could be used in nano-scopic devices.

Creating knowledge and Big Data: In an IoT world there exist a vast amount of raw data being continuously collected. It can be expected that a very large number of real-time sensor data streams exist as it is common for a given stream of data to be used in many different ways for many different inference purposes. Here, the data provenance and how it was processed must be known, and privacy and security must be applied too. When the data is big, challenge becomes bigger. Data mining techniques are expected to provide the creation of important knowledge from all this data. In IoT system huge and huge amount of data needs to be managed in each second. It is said that 220 Exabytes of data will be stored in this year [4]. The big-data concept must be implemented in IoT to manage this enormous amount of data. That's why handling this big amount of data and creating knowledge from it is a major research problem for IoT.

Humans in the loop: As IoT applications demand more sophistication, many of these new applications will intimately involve humans, i.e., humans and things will operate synergistically. Human in-the-loop systems offer exciting opportunities to a broad range of applications including energy management [18], health care [17], and automobile systems [16, 19]. For example, it is hypothesized that explicitly incorporating human-in-the-loop models can improve safety, and using these models home health care can improve medical conditions of the elder people and keep them safe. Although having humans in the loop has its advantages, but modelling human behaviours is extremely challenging due to the complex psychological and behavioural aspect of human beings. New research is necessary to raise human-in-the-loop control to a central principle in system design and to solve key challenges [15].

VI. CONCLUSIONS

IoT has been gradually bringing a series of technological changes in our daily lives, which in turn helps to make our life simpler and more comfortable through various technologies and applications. There is innumerable usefulness of IoT applications in various domains including medical, manufacturing, industrial, transportation, education, governance, mining, habitat etc. In spite of abundant benefits IoT is facing several flaws in governance and implementation level. Key observations in the literature are as follows. Firstly, there is no standard definition worldwide till date. Second, universal standardizations are required in architectural level too. Third, as technologies vary from vendor-to-vendor, interoperability issues are to be addressed more seriously. Lastly, for better global governance, we need to build uniformly accepted global standard protocols with proper safety and security issues.

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Updates

Upcoming Conferences/Workshops

- FIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), October 5-7, 2015, Daejeon Convention Center, Daejeon, Korea. http://www.vlsi-soc.com/
- 2015 International Conference On Computer Aided Design (ICCAD), November 2-6, 2015, Austin, TX. http://www.iccad.com/
- The 1st IEEE International Symposium on Nanoelectronic and Information Systems, December 21-23, 2015, Indore, India. http://www.inisweb.org/
- 29th International Conference on VLSI Design (VLSI-Design), January 4-8, 2016, Kolkata, India. http://vlsidesignconference.org/

Call for Papers/Proposals

- 2016 IEEE INFOCOM Workshop on Cross-Layer Cyber-Physical Systems Security, San Francisco, CA, April 15-16, 2016. Submission deadline: December 18, 2015. http://www.cse.cuhk.edu.hk/~byu/INFOCOM-CPS-2016/
- 2016 29th International Conference on VLSI Design (VLSID), Kolkata (India), Jan 4-8, 2016. Submission deadline design contest: November 15, 2015. http://vlsidesignconference.org/
- 17th International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, March 14-16, 2016. Paper submission: October 1, 2015. http://www.isqed.org/
- 2016 Design, Automation and Test Europe (DATE), Dresden, March 14-18, 2016. Submission Deadlines for Exhibition Theatre: October 18, 2015; Submission Deadlines for European Projects: October 18, 2015; PhD Forum: October 18, 2015. http://www.date-conference.com/
- 2016 18th International Conference on Electronics and Communication Systems Engineering (ICECSE), Turkey, April 19-20, 2016. Paper submissions: October 19, 2015. https://www.waset.org/conference/2016/04/istanbul/ICECSE/abstracts
- 2016 IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Slovakia, April 20-22, 2016. Submission deadline: 10th January 2016. http://ddecs2016.fiit.stuba.sk/DDECS_2016/
- 2016 34th IEEE VLSI TEST SYMPOSIUM, April 25 - 27, 2016, April 25 - 27, 2016. Submission deadline: Oct 16, 2015. http://www.tttc-vts.org/
- 2016 18th International Conference on High Performance Computing (HPCS), Paris, May 16-17, 2016. Submission deadline: November 16, 2015. http://hpcs2015.cisedu.info/
- 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, May 22-26, 2016. Live demonstration Proposal deadline: October 9, 2015; Technical sessions (lectures & posters): Submission deadline of 4-page papers: October 9, 2015. http://iscas2016.org/
- 2016 30th IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 23-27, 2016, Chicago. Submission deadline: Oct 9, 2015. http://www.ipdps.org/
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Pittsburgh, Pennsylvania, U.S.A., July 11-13, 2016. Special Session Proposal Deadline: January 22, 2016; Paper Submission Deadline: February 19, 2016; Graduate Student Forum Submission Deadline: February 19, 2016. http://www.isvlsi.org/
- IEEE Transactions on Multi-Scale Computing Systems (TMSCS), Special Issue on Design and Applications of Neuromorphic Computing System, submission deadline is January 15, 2016. http://www.computer.org/cms/Computer.org/transactions/cfps/cfp_tmscs.pdf

Funding Opportunities

- The Department of Defense (DOD) invites proposals to support the Acquisition of R&D Equipment/Instrumentation by Researchers at Historically Black Colleges and Universities and Minority-Serving Institutions (HBCU/MI) to

augment existing research capabilities or to develop new capabilities in research areas of interest to DOD and attract students to pursue studies leading to STEM careers. Proposals are due Nov 13. More information regarding W911NF-15-R-0025 is available at: http://www.grants.gov/web/grants/view-opportunity.html?oppId=278954

- DARPA Invites proposals for the Wafer Scale Infrared Detectors (WIRED) that will support R&D projects on high-performance, low-cost infrared imagers that respond in the short wave infrared (SWIR) and mid wave infrared (MWIR) and that can be fabricated directly on silicon-based readout integrated circuit (ROIC) substrates at the wafer scale. Proposals are due Nov 23. More information regarding DARPA-BAA-15-57 is available at: https://www.fbo.gov/spg/ODA/DARPA/CMO/DARPA-BAA-15-57/listing.html.
- The Office of Naval Research invites proposals for its Young Investigator Program to attract young faculty members of Institutions of Higher Education to the Department of the Navy's research program, to support their research, and to encourage their teaching and research careers. Proposals are due Dec 1. More information regarding N00014-15-R-FO13 is available at: http://www.grants.gov/web/grants/view-opportunity.html?oppId=278925.
- National Science Foundation: Smart and Connected Health (SCH) 13-543, Full Proposal Deadline date: October 13, 2015 for Exploratory (EXP) Proposals and December 10, 2015 for Integrative (INT) Proposals
- National Science Foundation: CISE Research Infrastructure (CRI) 15-590, Preliminary Proposal due on November 10, 2015, and Full Proposal due on January 20, 2016
- National Science Foundation: Computer and Network Systems (CNS), Core Programs 15-572, Small Project Proposal is due on November 18, 2015. http://www.nsf.gov/pubs/2015/nsf15572/nsf15572.htm
- National Science Foundation: Computing and Communication Foundations (CCF), Core Programs 15-573, Small Project Proposal is due on November 18, 2015. http://www.nsf.gov/pubs/2015/nsf15573/nsf15573.htm
- National Science Foundation: Information and Intelligent Systems (IIS), Core Programs 15-574, Small Project Proposal is due on November 18, 2015. http://www.nsf.gov/pubs/2015/nsf15574/nsf15574.htm
- National Science Foundation: Secure and Trustworthy Cyberspace (SaTC) 15-575, Small Project Proposal is due on November 18, 2015. http://www.nsf.gov/pubs/2015/nsf15575/nsf15575.htm
- National Science Foundation: CISE Research Infrastructure (CRI) 15-590, Preliminary Proposal is due on November 10, 2015, and Full Proposal Deadline is January 20, 2016. http://www.nsf.gov/pubs/2015/nsf15590/nsf15590.htm
- Department of the Army: ARL Research Associateship Program (RAP). https://www.fbo.gov/notices/066a853b2277e9b2cd5f66be7b13d80e
- Young Scientist Scheme, Fast Track Scheme, Science & Engineering Research Board, Department of Science & Technology (DST).
- Young faculty Research Fellowship, Department of Electronics & IT (DEITY).
- USAID Funding Opportunities for Indian Science, Technology, Innovation, and Partnerships (India Partnerships Annual Program Statement).
- India-Republic of Korea applied R&D programme for joint co-development of collaborative Industrial R&D project in the areas of ESDM.
- SMDP program, Visveswaraya scheme, Department of Electronics & IT (DEITY).
- India-Republic of Korea Joint Applied R&D Programme is joint initiative by the Department of Science & Technology (DST) & Department of Electronics & Information Technology (DeitY), Government of India and Ministry of Science, ICT & Future Planning (MSIP), Government of Korea. Last date for submission of the proposal 18th September, 2015.
- India Japan Cooperative Science Programme (IJCSP). The Department of Science and Technology (DST), Ministry of Science & Technology. Government of India, New Delhi and the Japan Society for the Promotion of Science (JSPS) conduct the India- Japan Cooperative Science.
- Programme (IJCSP) to promote bilateral scientific collaboration between Indian and Japanese scientists. Last date for submission of the proposal 8th September, 2015.

Job Openings

- Assistant/Associate Professor-Computer Science, University of Texas at El Paso, Department of Computer Science, El Paso, TX

- Tenure-track Asst. Prof. in Mixed-Signal Integrate, Nanyang Technological University, School of Electrical & Electronic Engineering, Singapore, Singapore, Singapore
- Faculty Positions in Computer Science & Engineering, Indian Institute of Technology Gandhinagar, Various Disciplines/Departments, Ahmedabad, Gujarat, India
- Assistant/Associate Professor, Computer Science, Georgia Southwestern State University, School of Computing and Mathematics, Americus, GA
- Tenure-track Assoc. Professor/Assistant Prof., Nanyang Technological University, School of Electrical & Electronic Engineering, Singapore, Singapore
- Lecturer / Senior Lecturer, The University of Melbourne, Australia, Dept. of Computing & Information Systems, Melbourne School, Victoria, Australia
- Lecturer in Software Engineering, The University of Melbourne, Australia, Dept. of Computing & Information Systems, Melbourne School, Victoria, Australia
- Lecturer in Data Analytics, The University of Melbourne, Australia, Dept. of Computing & Information Systems, Melbourne School, Victoria, Australia
- Engineering Faculty, Case Western Reserve University, Case School of Engineering, Cleveland, OH
- Assistant Professor, Missouri University of Science and Technology, Rolla, MO
- Assistant Professor, Missouri University of Science and Technology, Rolla, MO
- Assistant Professor, Wichita State University, Electrical Engineering & Computer Science (EECS), Wichita, KS
- Assistant/Associate Professors, Texas Tech University, Department of Computer Science, Lubbock, TX
- Computer Engineering Assistant Professor, Central Michigan University, School of Engineering and Technology, Mount Pleasant, MI
- TISED Endowed Chair in Sustainable Engr. and Design, McGill University, Montreal, QC, Canada
- Hugh W. Pearson Family Professorship, Brown University, School of Engineering, Providence, RI
- Faculty Positions at All Levels, Temple University, Electrical and Computer Engineering, Philadelphia, PA
- Assistant Professor, CTT – Electrical Engineering, University of Colorado Denver, Department of Electrical Engineering, Denver, CO
- Project Manager, Nanyang Technological University, School of Electrical and Electronics Engineering, Singapore, Singapore
- Faculty Positions at All Ranks, Nanyang Technological University, School of Physical and Mathematical Sci., Singapore
- Research Associate, Nanyang Technological University, School of Electrical and Electronic Engineering (EEE), Singapore
- EE Tenure Track Assistant Professor, Department Electrical Engineering Computer Science, University of Toledo, Toledo, OH
- Department Head- Computer Science, Department Computer Science, Institution: Virginia Tech Blacksburg, VA
- Faculty Positions in Electrical Engineering and Computer Science, Indian Institute of Technology, Indore
- Faculty Positions in Electrical Engineering and Computer Science, Indian Institute of Technology, Gandhinagar
- Full Professor in Computer Architecture in the Faculty of Informatics, Vienna University of Technology (TU Wien), Austria **(Now due Oct 24th)**

Ph.D. Fellowships Available

- *Ph.D. Topic*: Exploring Carbon Nanotubes for Energy Efficient Integrated Circuits

  Description: Carbon nanotubes (CNTs) have been proposed as a candidate material to build next generation on-chip interconnects in electronics. Their unique electrical, thermal, and mechanical properties are expected to meet the challenges of miniaturization and heat dissipation of microsystems. To fully exploit the potential of CNTs in the interconnection application, a number of problems must be solved. Progresses must be made in CNT modeling and circuit analysis to improve the implementation quality of CNTs, and enhance signal, power and thermal integrity of circuits with CNT interconnect. Furthermore, CNTs must be efficiently and reliably integrated with existing design flows.

  Major responsibilities: We are looking for a talented and highly motivated PhD student to join our activities in developing carbon nanotube based device and interconnect models for energy efficient circuits and architectures. Project will be guided a European funded project.

  Position summary: The position is limited to a maximum of three years. Student will be located at CNRS-LIRMM/Univ. Montpellier (http://www.lirmm.fr/lirmm_eng) in Montpellier, France. CNRS is the top research institute in Europe in fundamental research.

  For questions, please contact: Dr. Aida Todri-Sanial, CNRS-LIRMM, France, aida.todri@lirmm.fr

TCVLSI Member News

- None.

Outreach and Community

Methods to Approach Outreach: Help for the Classroom and Beyond

Mike Borowczak
Erebus Labs and Consulting, Laramie, Wyoming USA
Andrea Burrows
Department of Secondary Education, University of Wyoming, Laramie, WY, USA

In this issue of *Outreach and Community* the authors discuss the potential impacts of outreach - or ways to engage community with domain content - for the content knowledge experts who are doing the outreach; discuss the connections between floorplanning and other K-20 subjects - focusing on cross-cutting concepts; and highlight the outreach experiences of several university STEM faculty members. Faculty and professionals are highly encouraged to send highlights of their outreach activities for future issues! The *Outreach and Community* section ends with a knapsack problem puzzle which you can share amongst your peers, colleagues and students. Correct entries, sent to the section editor, will be placed in a drawing for a prize and/or recognized on the TCLVSI website - located at www.tcvlsi.org.

While it may be in our altruistic nature to give back to a community, classroom of students (of any age), or professional development for K12 teachers, there are other tangible personal benefits for domain experts doing outreach. For example, domain experts can learn negotiation techniques. Effective outreach requires negotiation between two different domain experts - in this case a K12 teacher and a VLSI/STEM domain knowledge expert. Negotiations are critical to ensure that the outreach event/session/class is of actual benefit to the audience. Negotiations are most likely when domain experts present explicit expectations of the event/session/class. What are the objectives of the event/session/class? How do these objectives fit into the previous learning of the audience? What does the audience need and how do the objectives help the audience? Openness of the domain expert, willingness to listen to the audience, and preparedness to adjust teaching accordingly, facilitates negotiations and learning. Through the process of effective negotiation an effective outreach event/session/class can be planned and executed (which translates specific domain content or research knowledge into well defined audience learning objectives given their prior knowledge). The lessons that are learned from simple negotiations translate far beyond the outreach experience as typical VLSI/STEM domain experts are not classically trained negotiation experts, and participating in and reflecting upon the process (in this case of defining a single outreach experience) can facilitate in the collegiate classroom as well. A first step could be approaching traditionally difficult content as a mini-outreach experience. Thus, the domain expert establishes the exact learning objectives for the students and then explores how well those objectives fit into the students' prior knowledge. Lastly, the domain expert must establish an open 'give and take' where participants are both learners and guides in the content lesson.

Generally, another hurdle for a VLSI/STEM domain knowledge expert is how to translate content/research knowledge to a 'novice' audience in order to address the negotiated objectives. The answer is simple clarity and novel approaches, not just showing a lecture power-point presentation. Since content experts are generally passionate about their area of research when doing outreach (e.g. they don't need motivation, background or scaffolding), engagement through active learning is critical, and traditional presentations of lecture slides are not enough. A relatively straightforward method for increasing motivation and contextual framing for any topic is through audience *input on, discussion of, and interaction with* topics' applications, careers and societal impacts (**ACS**). Any audience should leave an event/session/class knowing what the topic is, where the topic is used, by whom it is investigated, and what relevance it has to society! The same is true in the collegiate classroom, a technical presentation, or graduate mentoring or symposiums. When teaching, or collaborating with peers, domain experts can apply the same techniques of topic clarity and audience interactions. Albeit, the input, discussions, and conversations should be at a more challenging level than those usually occurring during outreach.

By far one of the hardest parts of outreach is gluing together the above parts (clear outreach objectives, topic relevance to the audience, topic clarity, and audience participation with the topic) without creating a one-way flow of information. While an end of the presentation Q&A *can* work in expert forums - less technical audiences require more topic engagement and connections to have any lasting effect. There are no shortcuts to learning how to glue together the parts and pieces of effective outreach - but one key may lie in the ability to know and read the audience - in real time.

Viewing the outreach as a system, where all parts work together to create an enjoyable learning environment, can assist a domain expert to realize the importance of audience input and participation. Viewing outreach systems effectively takes time and practice, however, the benefits to the domain expert and the audience members are undeniable as outreach lessons impact classroom teaching and graduate student mentoring.

For VLSI/STEM domain knowledge experts, outreach sessions can be a wonderful opportunity to develop and enhance their in-classroom teaching as well as their ability to collaborate with peers outside of their direct domain expertise.

Faculty Outreach Spotlight

This issues' faculty outreach spotlight focuses on Amy Banic - an Assistant Professor in the Department of Computer Science, in the College of Engineering and Applied Science at the University of Wyoming who holds a joint appointment with the Idaho National Laboratory. While in the previous section the benefits of outreach on an individual researcher were highlighted, Amy's submission focuses on the positive impacts that her outreach activities have on the communities they serve.

According to Amy, her lab, "focuses on human-centric research - specifically in designing and developing novel technology to help people and solve real-world problems." She extends her and her lab's research through outreach - specially through an NSF funded Research Experience for Undergraduates (REU) and further through the co-teaching of a course for a Wyoming-based High School Summer Institute (UWYO HSI) with University of Wyoming Professor Ruben Gamboa. Amy highlighted some of the impacts of her REU session(s) on students it has served.

The yearly REU sessions:

- Exposes students to research early on when they are making decisions about careers
- Teaches students professional and educational development as they relate to novel technology and methods
- Encourages more students, especially women and other underrepresented minorities, to pursue research careers, increasing the pipeline and expanding the diversity of ideas in solutions
- Prepares the next generation of researchers to have the expertise, ethics, and skills to conduct the next big research problems in the future
- Helps students to realize there is more to a CS career than sitting in front of a PC coding, by actually helping people solve real world problems that can make a difference

Of particular interest, especially in light of our previous section are the first, third and last bullet points - which mention both careers and real-world problems. Amy's contribution to outreach extends beyond the collegiate level into K12 education with a 3-week course which engages students in activities while exposing them to an advanced learning environment free of grades. The course uses concepts of generative art, which "uses code to create patterns, repetition, art forms, and reusable code" to teach them coding elements such as variables, loops, functions, and parameters. The course also focuses on art and design elements, such as "composition, positive/negative space, line, form, function, movement, and perceptions."

The three-week course:

- Exposes HS students to coding early since many K12 students in Wyoming do not have exposure to CS at all
- Engages HS students through art, creativity, and design rather than 'pure' coding
- Encourage more students, especially women and other underrepresented minorities, to pursue studies in college that relate to STEM, especially computer science.

And some of the direct results from students that have taken the course include:

- 67% of the students reported that they would take more computer science courses in the future.

- Several female students who reported prior to taking the course that they would not take any computer science courses in the future changed their perceptions after taking the course.
- Students also self-reported that they "liked the assignments, making art, having the freedom to build what they wanted, learning all the cool things they could do in a virtual world and that the class was comfortable, different, challenging and fun."

From the two outreach experiences that Amy shared with us, we can summarize a few key points - first and foremost - outreach experiences for students can in fact be "different and challenging," and what's critical is knowing the audience. Translating a domain expert's research content in a way that is approachable, understandable, engaging and interesting can take many forms. Establishing partnerships with peers can help drive an end product that makes a compromise between pure research and ideas.. Outreach isn't just something "needed for a grant," it is something critical for content awareness and expansion as well as enjoyable to do!

Do you have outreach experiences that you would like to share? If you would like to be featured in the next issue of TCVLSI's newsletter, or if you would like to nominate someone to featured in the next issue send an email to mike@erebuslabs.com with details and contact information.

A Puzzle for All: Knapsack Logs

You're given 20 items *n* (n=1 to 20) with weights *w* (w=1+$\log_2$ n) and profit values *p* ($p = \sqrt{\square} + w \bmod n$), first compute the weight and profit of all 20 items. After computing the profit density for each item, greedily attempt to fill a knapsack that can hold a total *weight of 50*.

1. What are the resulting weights and profits when filling the knapsack greedily by profit, weight and density?
2. What is the optimal solution result?
3. When profit is a function of weight and item number is it possible to derive a formula for the items to be included in the greedy knapsacks? What about the optimal solution?

Use the table below to get started and submit your answers to this puzzle to mike@erebuslabs.com. You'll be added to a running scoreboard of correct submissions and be entered for a chance to win a prize.

item # n	weight $1 + \log_2 n$	profit sqrt(w) + w MOD n	pi/wi	greedy by profit	greedy by weight	greedy by density	optimal solution
1	1.00	1.00					
2	2.00	1.41					
3	2.58	2.02					
4	3.00	2.73					
5	3.32	3.50					
6							
7							
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20							

Have a puzzle? Do you want to try to stump your colleagues? Send your puzzle ideas to mike@erebuslabs.com and you might see it featured here!

Call for Contributions

The VLSI Circuits and Systems Letter aims to provide timely updates on technologies, educations and opportunities related to VLSI circuits and systems for TCVLSI members. The letter will be published twice a year and it contains the following sections:

- **Features**: selective short papers within the technical scope of TCVLSI, "What is" section to introduce interesting topics related to TCVLSI, and short review/survey papers on emerging topics in the areas of VLSI circuits and systems.
- **Opinions**: Discussions and book reviews on recent VLSI/nanoelectronic/emerging circuits and systems for nano computing, and "Expert Talks" to include the interviews of eminent experts for their concerns and predictions on cutting-edge technologies.
- **Updates**: Upcoming conferences/workshops of interest to TCVLSI members, call for papers of conferences and journals for TCVLSI members, funding opportunities and job openings in academia or industry relevant to TCVLSI members, and TCVLSI member news.
- **Outreach and Community**: The "Outreach K20" section highlights integrating VLSI computing concepts with activities for K-4, 4-8, 9-12 and/or undergraduate students. It also features student fellowship information as well a "Puzzle" section for our readership.

We are soliciting contributions to all these four sections. Please directly contact the editors and/or associate editors by email to submit your contributions.

Submission Deadline:

All contributions must be submitted by March 1, 2016 in order to be included in the April issue of the letter.

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