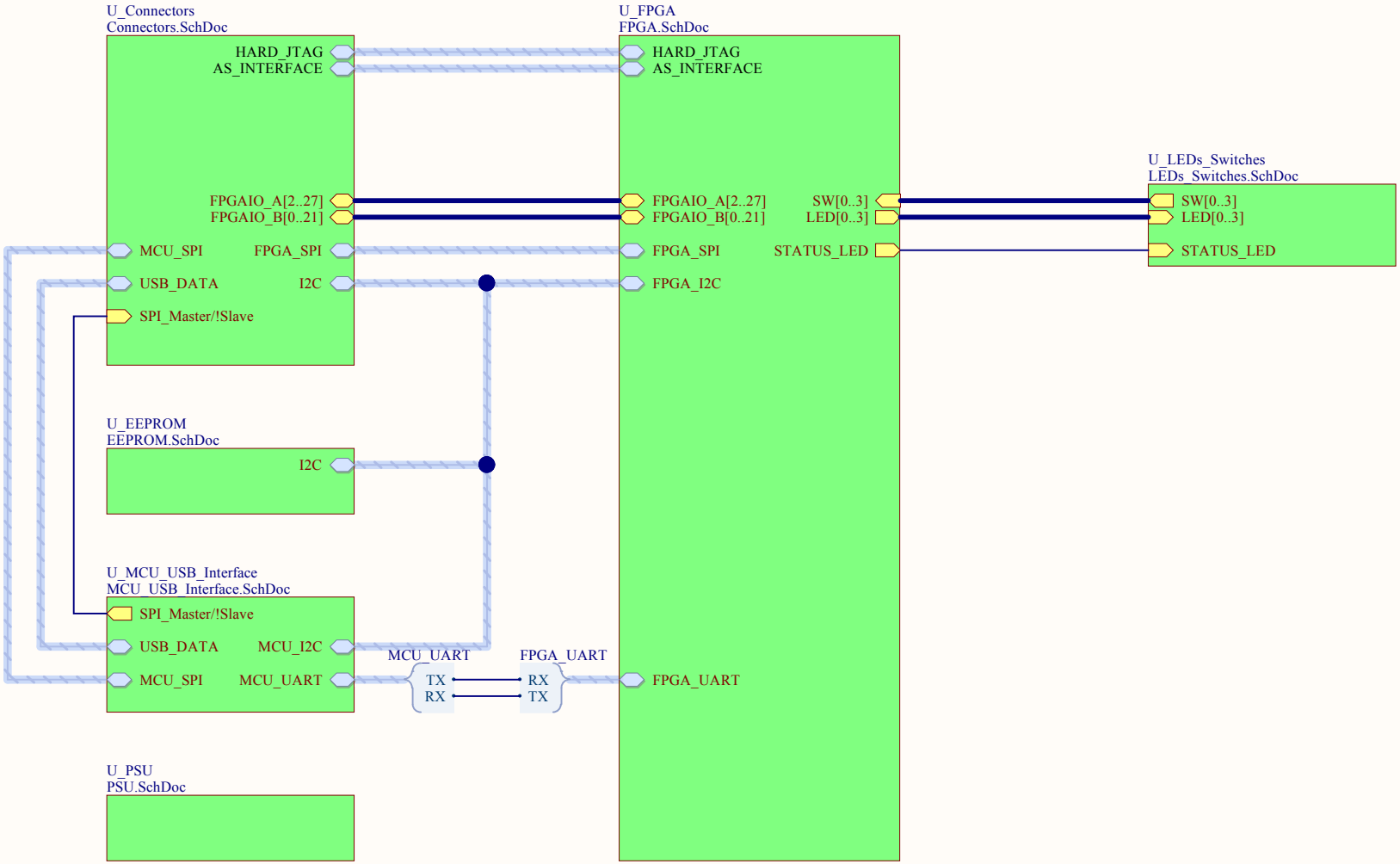
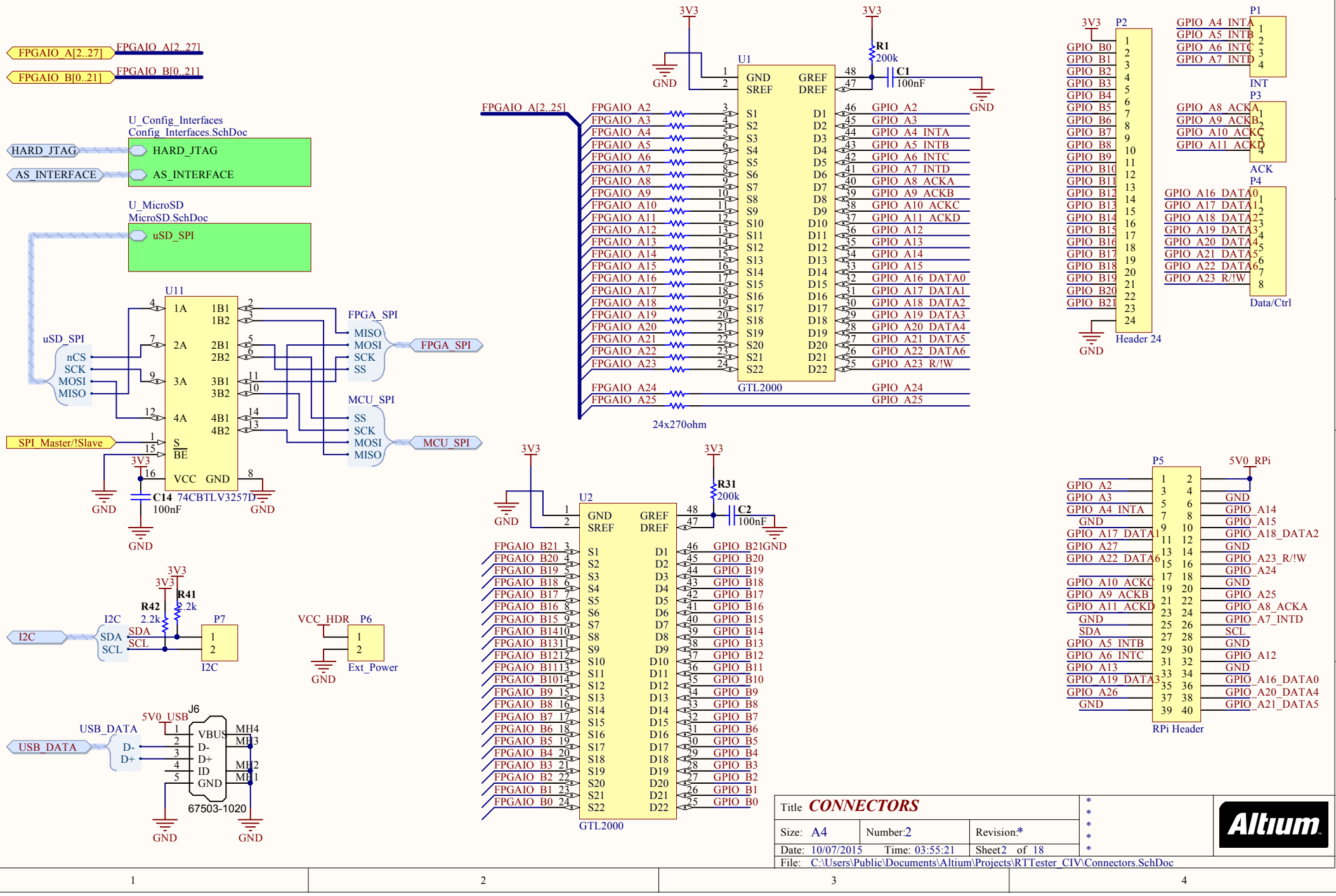
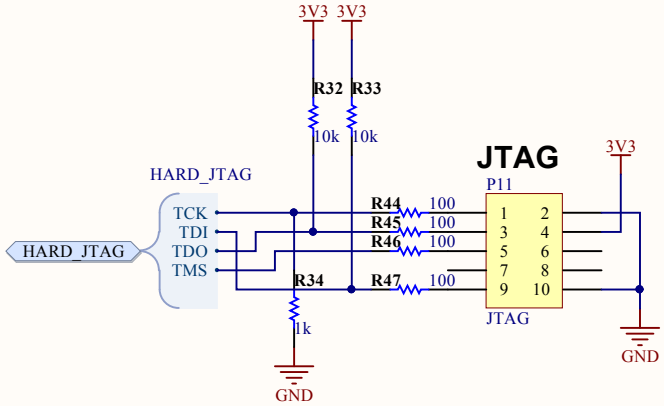
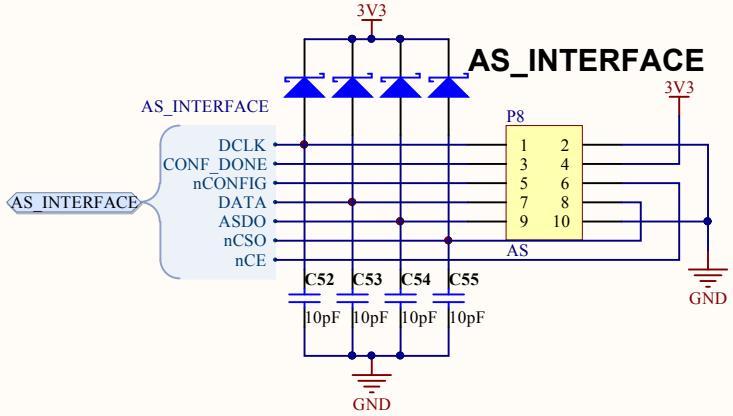


Title **TOP**			* * * * *
Size: A4	Number:1	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet1 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\Top.SchDoc			



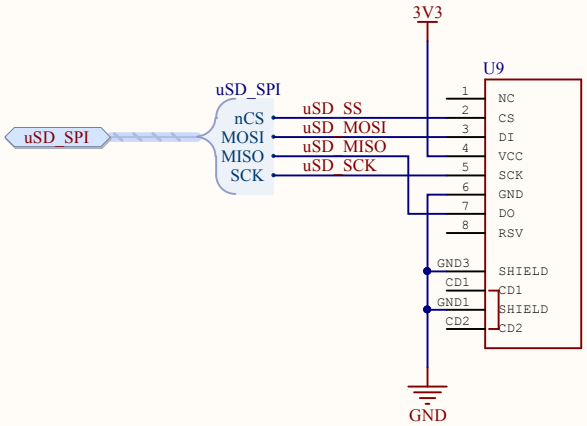
Title	**CONNECTORS**		
Size: A4	Number:2	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet2 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\Connectors.SchDoc			



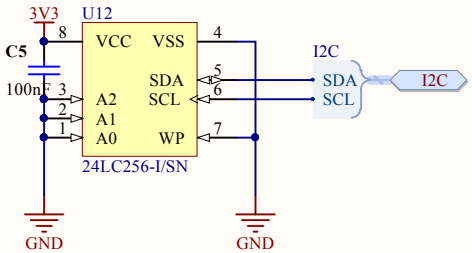


Title	*CONFIG. INTERFACES*		
Size: A4	Number:3	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet3 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\Config_Interfaces.SchDoc			

Altium

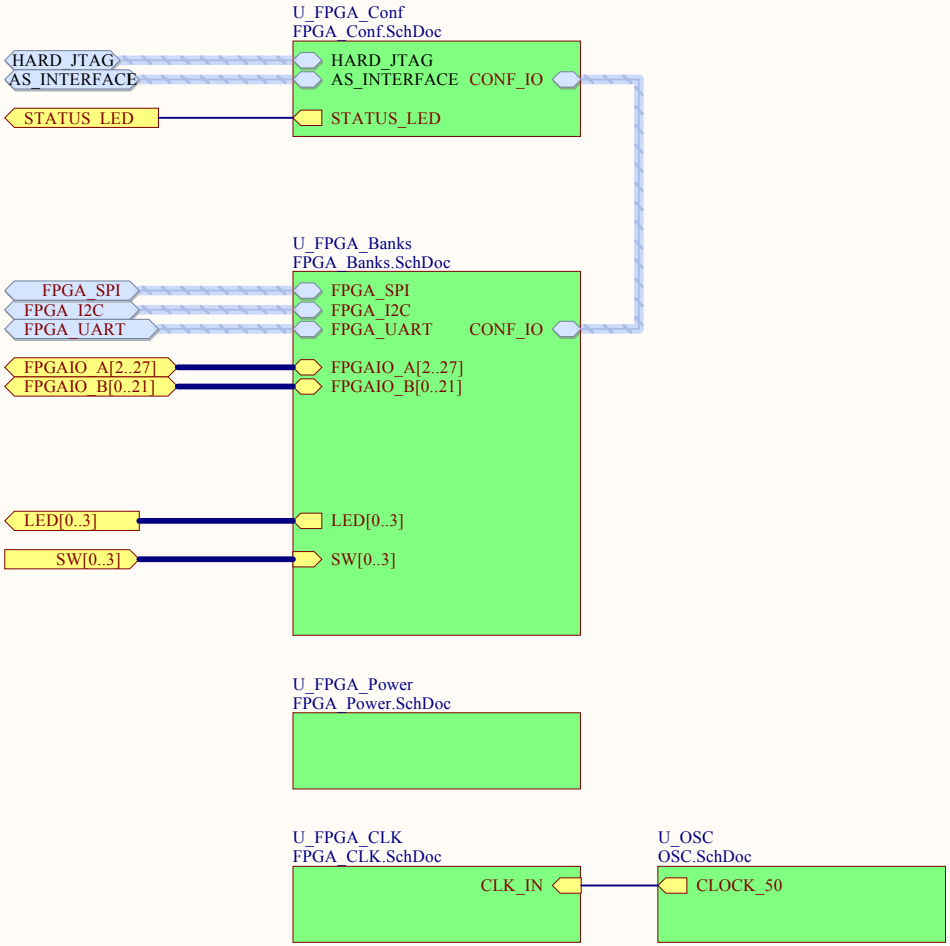


Title	***MICRO-SD***		
Size: A4	Number:4	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet4 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\MicroSD.SchDoc			

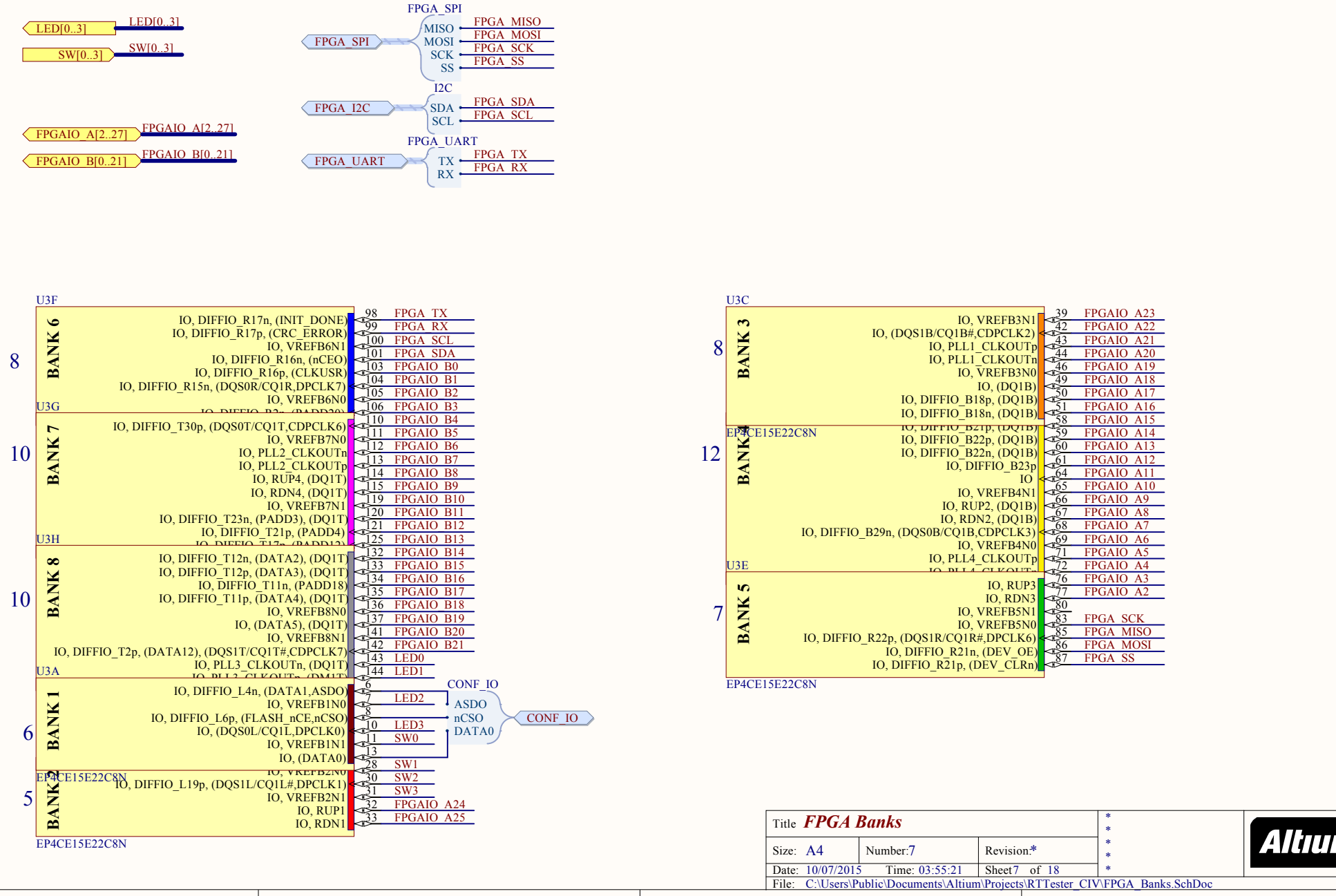


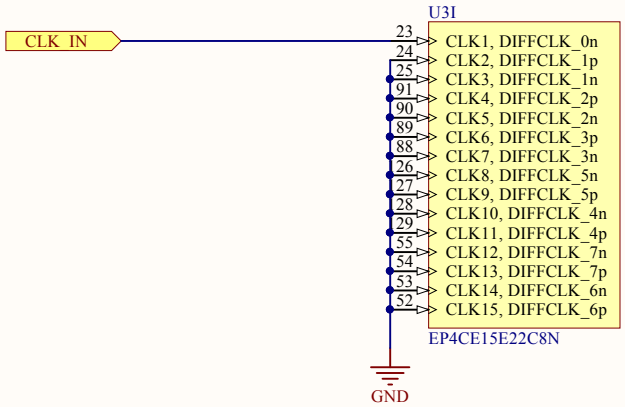
I2C Address:
0xA0 = 1010000

Title	**EEPROM**		
Size: A4	Number:5	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet5 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\EEPROM.SchDoc			

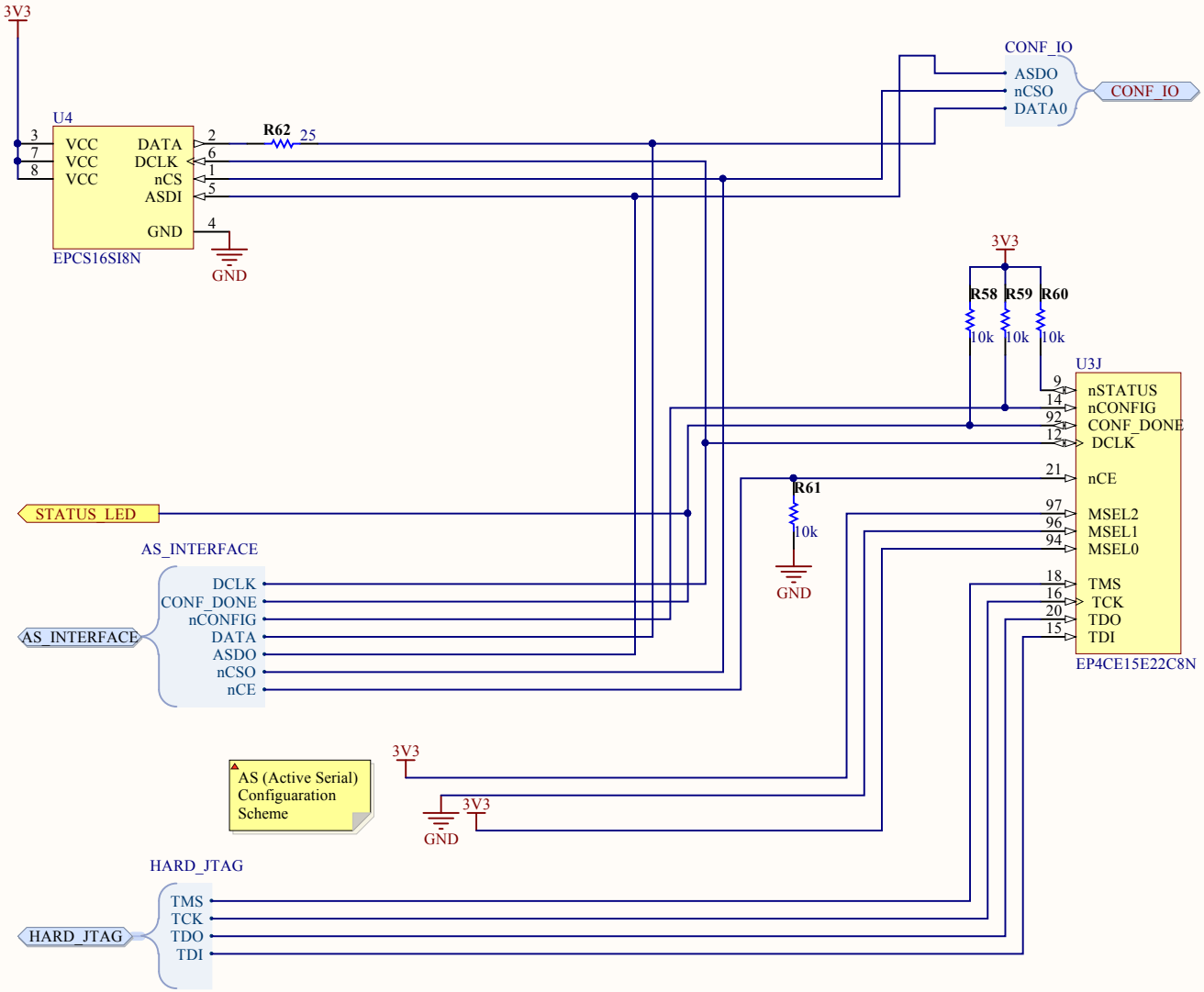


Title	***FPGA TOP***		
Size: A4	Number:6	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet6 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\FPGA.SchDoc			

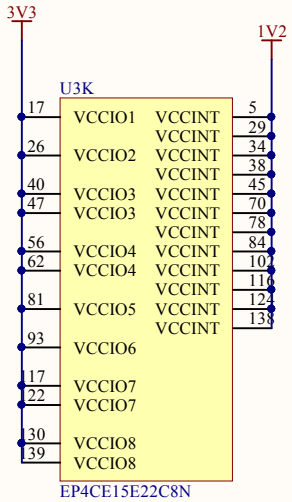

LED[0..3]
LED[0..3]
SW[0..3]
SW[0..3]
FPGAIO_A[2..27]
FPGAIO_A[2..27]
FPGAIO_B[0..21]
FPGAIO_B[0..21]
FPGA_SPI
FPGA_SPI
MISO
MOSI
SCK
SS
FPGA_MISO
FPGA_MOSI
FPGA_SCK
FPGA_SS
I2C
FPGA_I2C
SDA
SCL
FPGA_SDA
FPGA_SCL
FPGA_UART
FPGA_UART
TX
RX
FPGA_TX
FPGA_RX
U3F
BANK 6
IO, DIFFIO_R17n, (INIT_DONE)
IO, DIFFIO_R17p, (CRC_ERROR)
IO, VREFB6N1
IO, DIFFIO_R16n, (nCEO)
IO, DIFFIO_R16p, (CLKUSR)
IO, DIFFIO_R15n, (DQS0R/CQ1R,DPCLK7)
IO, VREFB6N0
98 FPGA_TX
99 FPGA_RX
100 FPGA_SCL
101 FPGA_SDA
103 FPGAIO_B0
104 FPGAIO_B1
105 FPGAIO_B2
106 FPGAIO_B3
U3G
BANK 7
IO, DIFFIO_T30p, (DQS0T/CQ1T,CDPCLK6)
IO, VREFB7N0
IO, PLL2_CLKOUTn
IO, PLL2_CLKOUTp
IO, RUP4, (DQ1T)
IO, RDN4, (DQ1T)
IO, VREFB7N1
IO, DIFFIO_T23n, (PADD3), (DQ1T)
IO, DIFFIO_T21p, (PADD4)
110 FPGAIO_B4
111 FPGAIO_B5
112 FPGAIO_B6
113 FPGAIO_B7
114 FPGAIO_B8
115 FPGAIO_B9
119 FPGAIO_B10
120 FPGAIO_B11
121 FPGAIO_B12
125 FPGAIO_B13
U3H
BANK 8
IO, DIFFIO_T12n, (DATA2), (DQ1T)
IO, DIFFIO_T12p, (DATA3), (DQ1T)
IO, DIFFIO_T11n, (PADD18)
IO, DIFFIO_T11p, (DATA4), (DQ1T)
IO, VREFB8N0
IO, (DATA5), (DQ1T)
IO, VREFB8N1
IO, DIFFIO_T2p, (DATA12), (DQS1T/CQ1T#,CDPCLK7)
IO, PLL3_CLKOUTn, (DQ1T)
132 FPGAIO_B14
133 FPGAIO_B15
134 FPGAIO_B16
135 FPGAIO_B17
136 FPGAIO_B18
137 FPGAIO_B19
141 FPGAIO_B20
142 FPGAIO_B21
143 LED0
144 LED1
U3A
BANK 1
IO, DIFFIO_L4n, (DATA1,ASDO)
IO, VREFB1N0
IO, DIFFIO_L6p, (FLASH_nCE,nCSO)
IO, (DQS0L/CQ1L,DPCLK0)
IO, VREFB1N1
IO, (DATA0)
6 LED2
8
10 LED3
11 SW0
13
CONF_IO
ASDO
nCSO
DATA0
CONF_IO
EP4CE15E22C8N
BANK 2
IO, DIFFIO_L19p, (DQS1L/CQ1L#,DPCLK1)
IO, VREFB2N1
IO, RUP1
IO, RDN1
28 SW1
30 SW2
31 SW3
32 FPGAIO_A24
33 FPGAIO_A25
EP4CE15E22C8N
U3C
BANK 3
IO, VREFB3N1
IO, (DQS1B/CQ1B#,CDPCLK2)
IO, PLL1_CLKOUTp
IO, PLL1_CLKOUTn
IO, VREFB3N0
IO, (DQ1B)
IO, DIFFIO_B18p, (DQ1B)
IO, DIFFIO_B18n, (DQ1B)
39 FPGAIO_A23
42 FPGAIO_A22
43 FPGAIO_A21
44 FPGAIO_A20
46 FPGAIO_A19
49 FPGAIO_A18
50 FPGAIO_A17
51 FPGAIO_A16
58 FPGAIO_A15
EP4CE15E22C8N
BANK 4
IO, DIFFIO_B22p, (DQ1B)
IO, DIFFIO_B22n, (DQ1B)
IO, DIFFIO_B23p
IO
IO, VREFB4N1
IO, RUP2, (DQ1B)
IO, RDN2, (DQ1B)
IO, DIFFIO_B29n, (DQS0B/CQ1B,CDPCLK3)
IO, VREFB4N0
IO, PLL4_CLKOUTp
59 FPGAIO_A14
60 FPGAIO_A13
61 FPGAIO_A12
64 FPGAIO_A11
65 FPGAIO_A10
66 FPGAIO_A9
67 FPGAIO_A8
68 FPGAIO_A7
69 FPGAIO_A6
71 FPGAIO_A5
72 FPGAIO_A4
U3E
BANK 5
IO, RUP3
IO, RDN3
IO, VREFB5N1
IO, VREFB5N0
IO, DIFFIO_R22p, (DQS1R/CQ1R#,DPCLK6)
IO, DIFFIO_R21n, (DEV_OE)
IO, DIFFIO_R21p, (DEV_CLRn)
76 FPGAIO_A3
77 FPGAIO_A2
80
83 FPGA_SCK
85 FPGA_MISO
86 FPGA_MOSI
87 FPGA_SS
EP4CE15E22C8N
Title FPGA Banks
Size: A4
Number:7
Revision:*
Date: 10/07/2015
Time: 03:55:21
Sheet7 of 18
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\FPGA_Banks.SchDoc
Altium

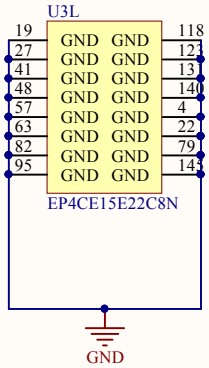


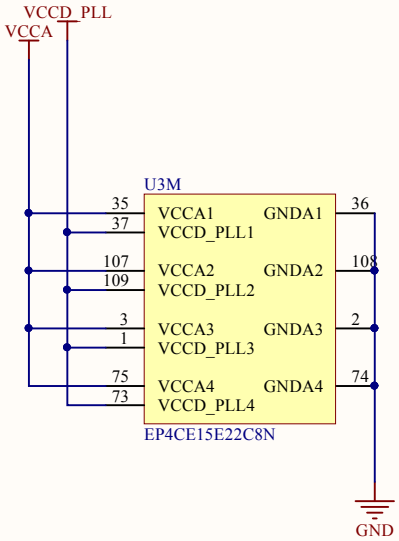
Title	***FPGA CLOCK***		
Size: A4	Number:8	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet8 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\FPGA_CLK.SchDoc			



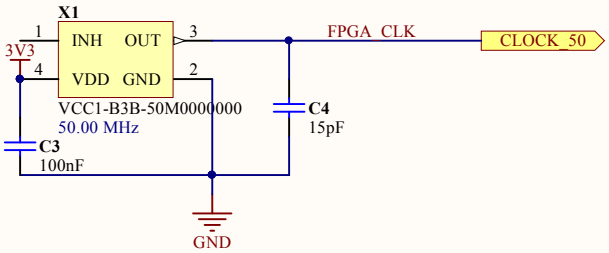
Title	*FPGA CONFIGURATION*		
Size: A4	Number:9	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet9 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\FPGA_Conf.SchDoc			



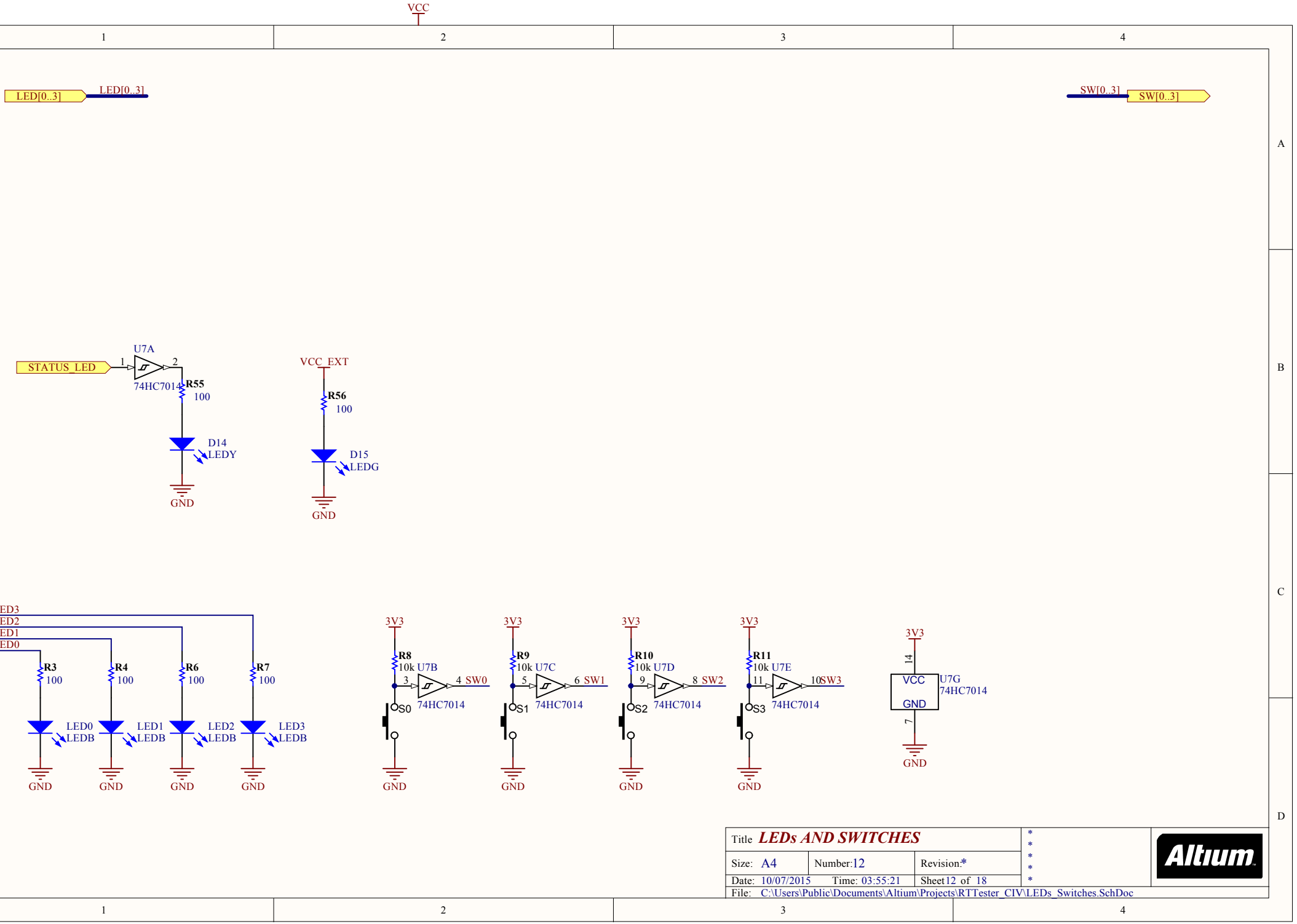


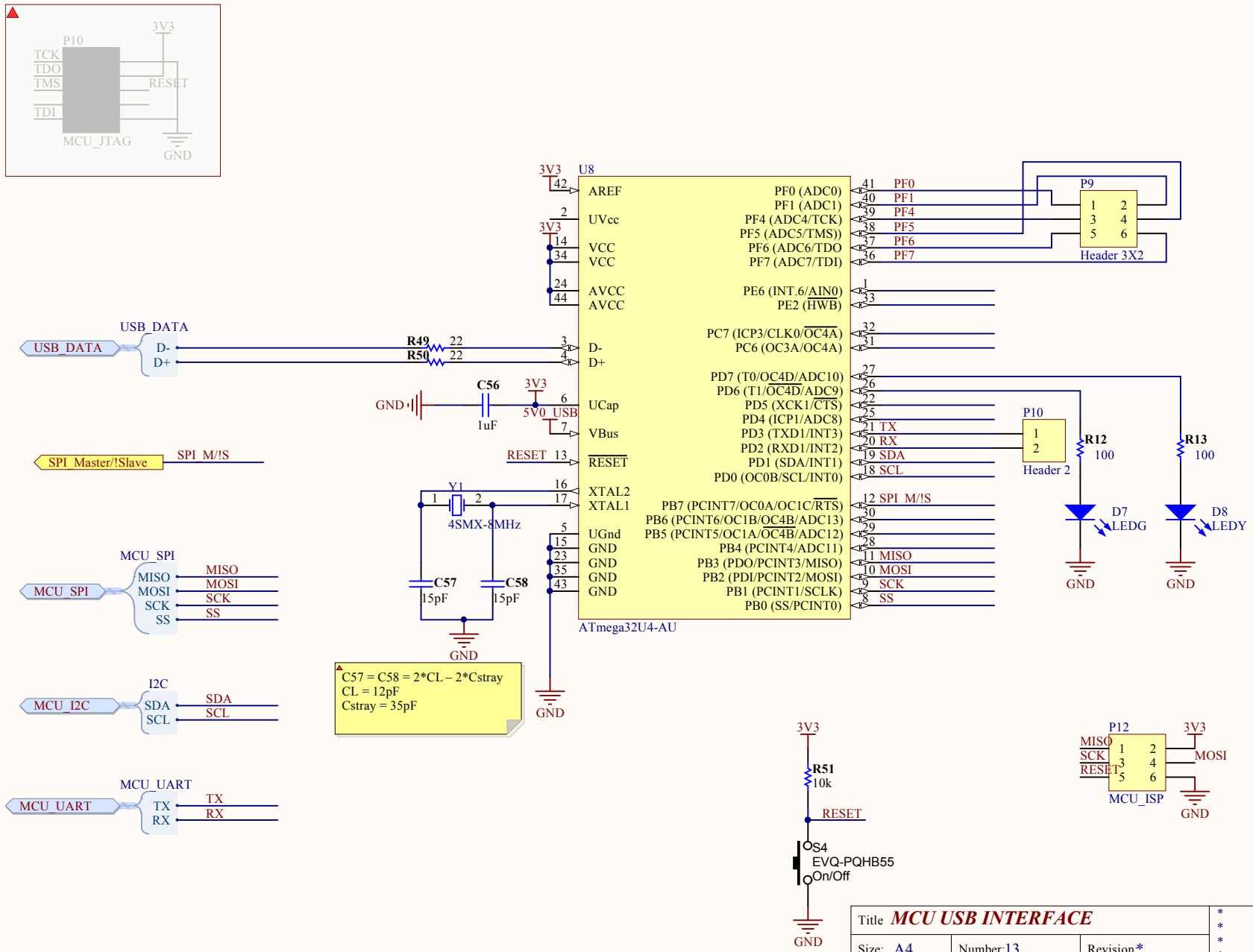


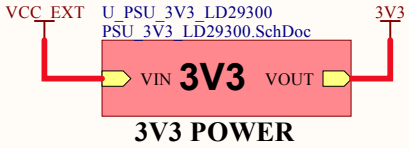
Title	**FPGA POWER**		
Size: A4	Number:10	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet 10 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\FPGA_Power.SchDoc			



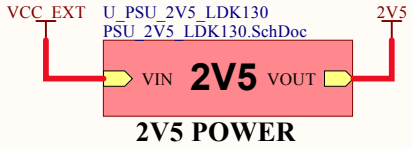
Title	***OSCILATOR***		
Size: A4	Number:11	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet11 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\OSC.SchDoc			


VCC
LED[0..3]
LED[0..3]
SW[0..3]
SW[0..3]
STATUS_LED
U7A
74HC7014
R55
100
D14
LEDY
GND
VCC_EXT
R56
100
D15
LEDG
GND
LED3
LED2
LED1
LED0
R3
100
R4
100
R6
100
R7
100
LED0
LEDB
LED1
LEDB
LED2
LEDB
LED3
LEDB
GND
3V3
R8
10k U7B
4 SW0
S0
74HC7014
R9
10k U7C
6 SW1
S1
74HC7014
R10
10k U7D
8 SW2
S2
74HC7014
R11
10k U7E
10SW3
S3
74HC7014
3V3
14
VCC
GND
U7G
74HC7014
7
GND
Title LEDs AND SWITCHES
Size: A4
Number:12
Revision:*
Date: 10/07/2015
Time: 03:55:21
Sheet12 of 18
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\LEDs_Switches.SchDoc
Altium


P10
3V3
TCK
TDO
TMS
RESET
TDI
MCU_JTAG
GND
U8
3V3
AREF
UVcc
VCC
VCC
AVCC
AVCC
D-
D+
UCap
VBus
RESET
XTAL2
XTAL1
UGnd
GND
GND
GND
GND
PF0 (ADC0)
PF1 (ADC1)
PF4 (ADC4/TCK)
PF5 (ADC5/TMS))
PF6 (ADC6/TDO
PF7 (ADC7/TDI)
PE6 (INT.6/AIN0)
PE2 (HWB)
PC7 (ICP3/CLK0/OC4A)
PC6 (OC3A/OC4A)
PD7 (T0/OC4D/ADC10)
PD6 (T1/OC4D/ADC9)
PD5 (XCK1/CTS)
PD4 (ICP1/ADC8)
PD3 (TXD1/INT3)
PD2 (RXD1/INT2)
PD1 (SDA/INT1)
PD0 (OC0B/SCL/INT0)
PB7 (PCINT7/OC0A/OC1C/RTS)
PB6 (PCINT6/OC1B/OC4B/ADC13)
PB5 (PCINT5/OC1A/OC4B/ADC12)
PB4 (PCINT4/ADC11)
PB3 (PDO/PCINT3/MISO)
PB2 (PDI/PCINT2/MOSI)
PB1 (PCINT1/SCLK)
PB0 (SS/PCINT0)
ATmega32U4-AU
PF0
PF1
PF4
PF5
PF6
PF7
P9
Header 3X2
USB_DATA
D-
D+
R49 22
R50 22
C56
1uF
5V0_USB
SPI_M/!S
SPI_Master/!Slave
Y1
4SMX-8MHz
C57
15pF
C58
15pF
TX
RX
SDA
SCL
MISO
MOSI
SCK
SS
P10
Header 2
R12
100
R13
100
D7
LEDG
D8
LEDY
C57 = C58 = 2*CL – 2*Cstray
CL = 12pF
Cstray = 35pF
MCU_SPI
MCU_I2C
I2C
MCU_UART
R51
10k
S4
EVQ-PQHB55
On/Off
P12
MCU_ISP
Title MCU USB INTERFACE
Size: A4
Number:13
Revision:*
Date: 10/07/2015
Time: 03:55:21
Sheet13 of 18
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\MCU_USB_Interface.SchDoc
Altium

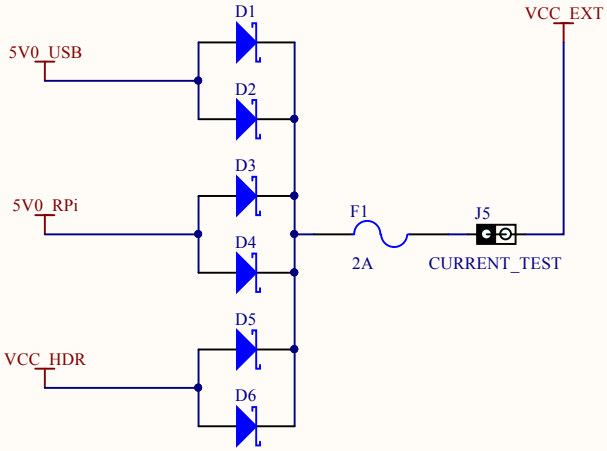


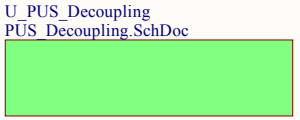
3V3 POWER



2V5 POWER

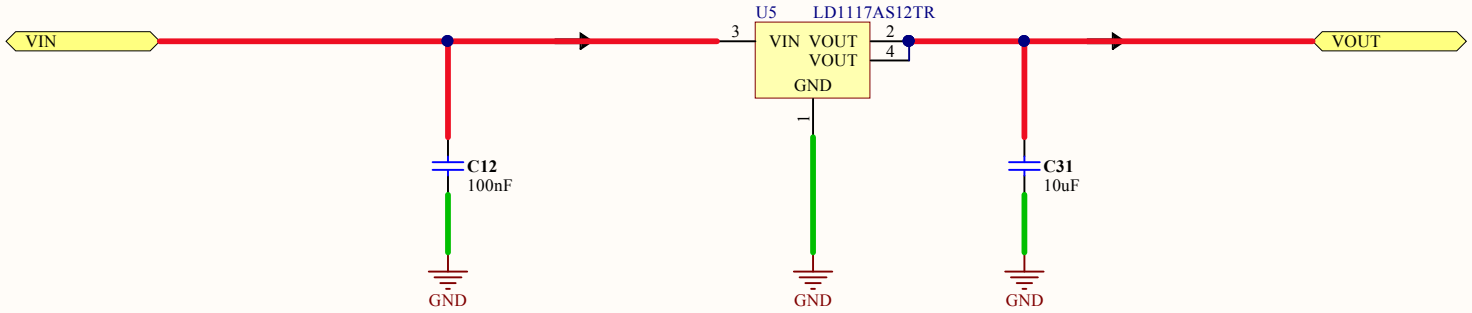
1V2 POWER



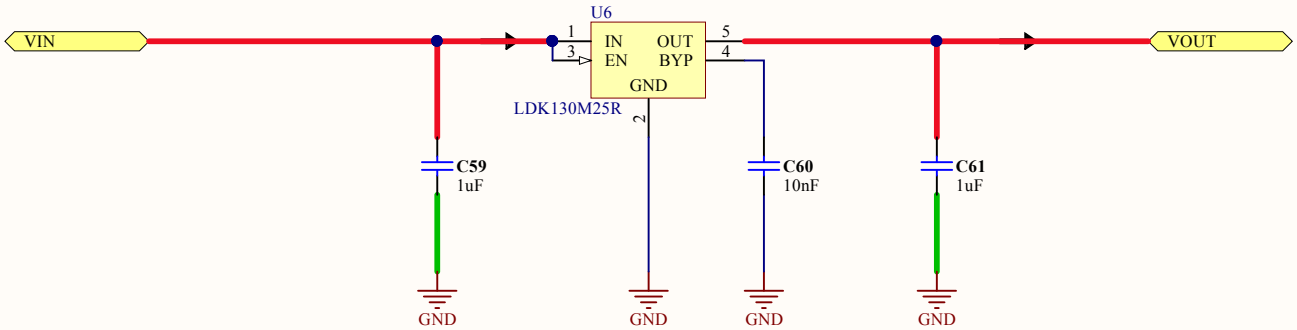


Title	***PSU TOP***		
Size: A4	Number:14	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet 14 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\PSU.SchDoc			

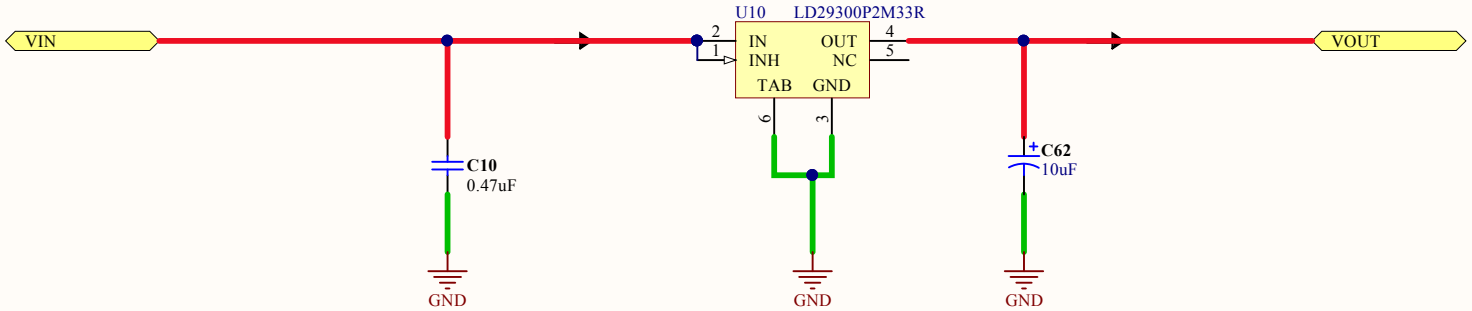
Altium



Title	***PSU 1V2***		
Size: A4	Number:15	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet 15 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\PSU_1V2_LD1117A.SchDoc			

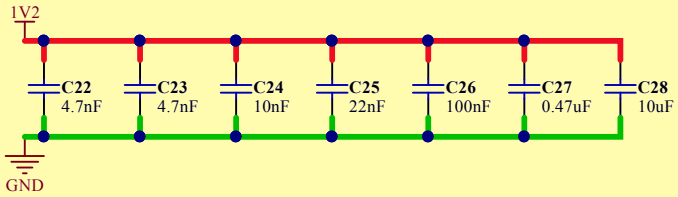


Title	*PSU 2V5*		
Size: A4	Number:16	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet16 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\PSU_2V5_LDK130.SchDoc			

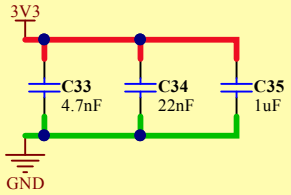


Title	***PSU 3V3***		
Size: A4	Number:17	Revision:*	
Date: 10/07/2015	Time: 03:55:21	Sheet17 of 18	
File: C:\Users\Public\Documents\Altium\Projects\RTTester_CIV\PSU_3V3_LD29300.SchDoc			

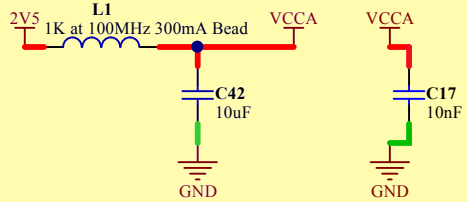
1.2V Decoupling



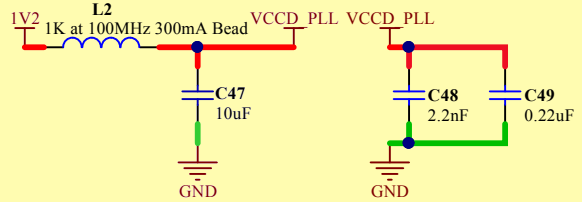
3.3V Decoupling

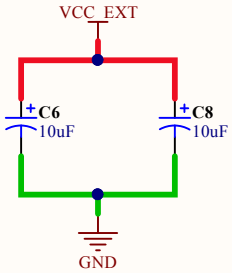


PLL VCCA Decoupling



PLL VCCD Decoupling





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