LAPORAN UJIAN AKHIR SEMESTER
ELEKTRONIKA DAYA

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Github : **https://github.com/dityrwp/Elday-UAS-2025-1**

DEPARTEMEN TEKNIK ELEKTRO DAN TEKNOLOGI INFORMASI

FAKULTAS TEKNIK UNIVERSITAS GADJAH MADA

YOGYAKARTA

2025

TASK I

Totem Pole Low Side Gate Driver

1.1 Objective and Design

Objective

- Investigate MOSFET switching behavior under a resistive load.
- Evaluate the impact of gate-driver topology on switching speed, Miller effect, and switching losses.
- Compare a resistive gate drive and an active totem-pole gate driver in simulation and hardware.

Power Stage and MOSFET

- MOSFET: **IRFZ48N**, low-side configuration.
- Supply voltage: **12 V**.
- Load: **220 Ω resistive load**.

Gate Driver Topologies

- Resistive gate drive
    - Gate driven through series resistor R_g.
- Totem-pole gate driver
    - Implemented using **BD139 (NPN)** and **BD140 (PNP)** BJTs.

Gate Resistance Selection

- R_g varied in simulation: **10 Ω, 47 Ω, 100 Ω, 220 Ω**.

Input Signal and Operating Conditions

- Gate drive: **12 V**, 50% duty cycle.
- Fast rise/fall times to avoid source-limited switching.
- Local decoupling capacitor used to stabilize supply during transients.

1.2 Simulation Results and Analysis

Q1. How does the totem-pole driver improve MOSFET switching performance compared to using only a gate resistor and voltage source?

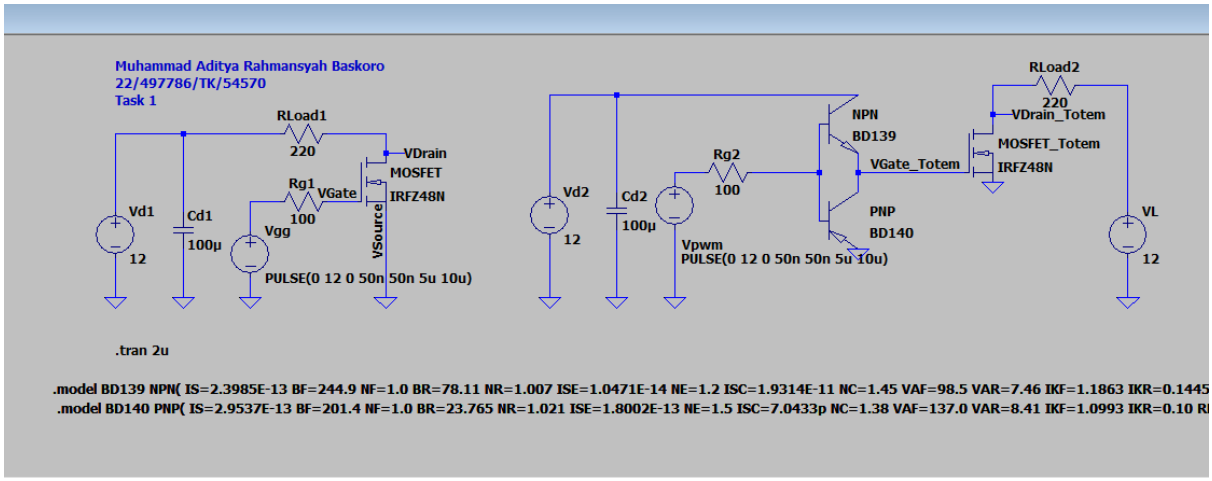
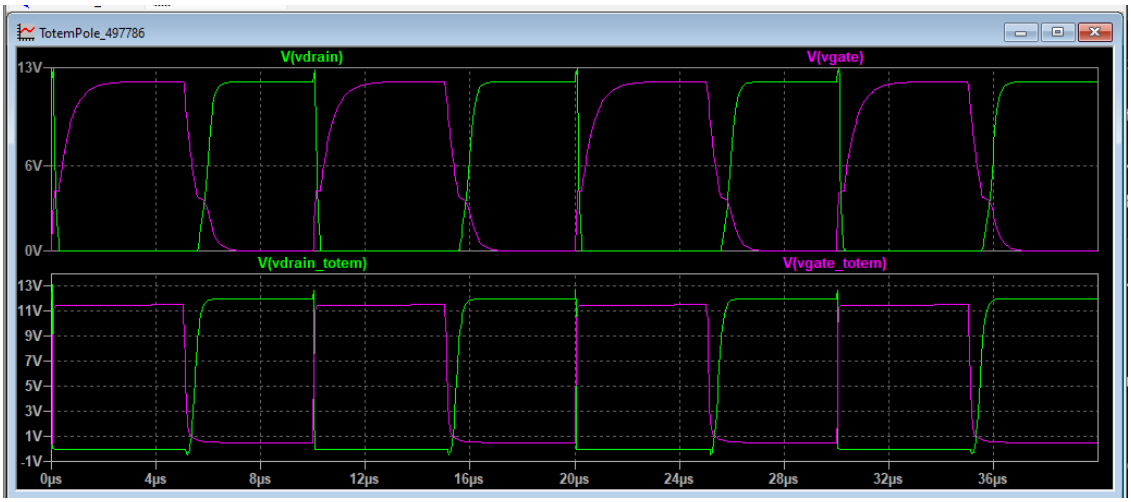


Fig.1 Rangkaian dan Hasil AC Analysis LPF LTSpice



Observation :

- **Delay Time:** Time to reach 10% of final voltage ($t_{10\%}$).
- **Rise/Fall Time:** Transition time between 10% and 90%.
- **Plateau:** The Miller Plateau voltage measured while the drain voltage (V_{ds}) is swinging between 10V and 2V.

Parameter	vgate (Standard Drive)	vgate_totem (Totem Pole)
Delay Time (On)	44.0 ns	25.5 ns
Rise Time	1.11 µs	62.5 ns
Turn-on Plateau	4.24 V	None
Fall Time	1.11 µs	206.0 ns
Turn-off Plateau	4.10 V	None
Overshoot	None	None

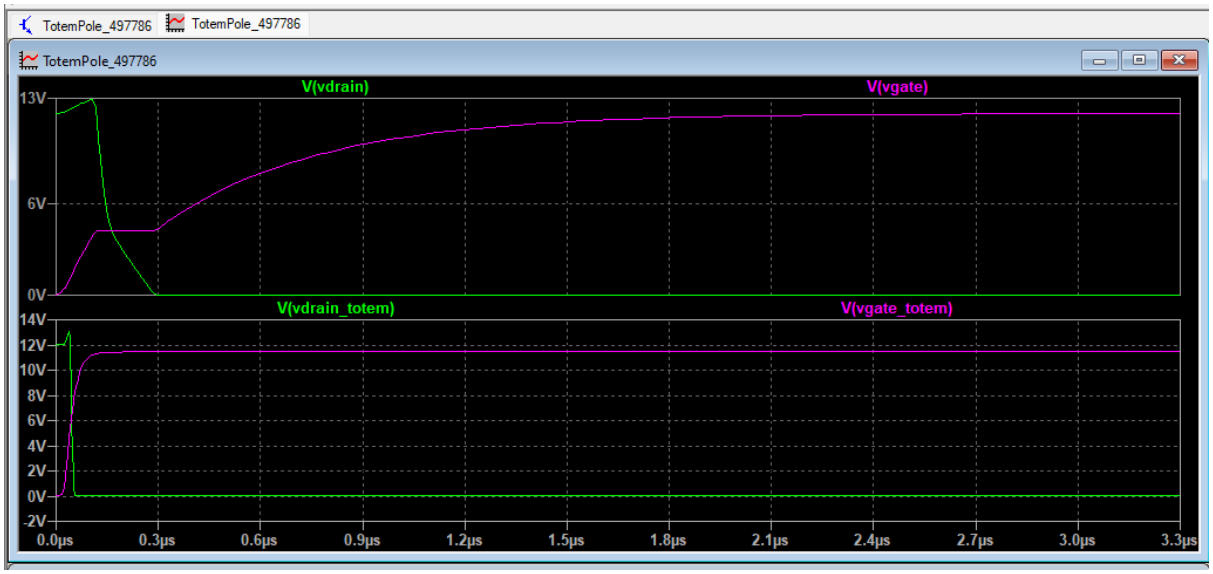


Fig.2 Waveform comparison between resistive (top) and totem pole gate driver (bottom)

The totem-pole gate driver significantly improves MOSFET switching performance by actively sourcing and sinking gate current, thereby reducing the effective gate drive impedance compared to a simple voltage source with a series gate resistor.

From the simulation results, the resistive gate drive creates a slow gate voltage transition, during which the MOSFET gate current is limited by $R_g$and the MOSFET input capacitances. This results in a transition where drain source voltage and drain current overlap, which shown in the Vgate rise and slower Vdrain fall.

In contrast, the totem pole driver supplies substantially higher transient gate current, as shown by the BJT emitter and collector current waveforms. During turn-on, the NPN rapidly charges the gate capacitance, while during turn-off, the PNP provides a low impedance discharge path. This leads to a much steeper $v_{GS}(t)$ transition and a instantaneous transition through the Miller plateau. As a result, the drain source voltage falls rapidly while the drain current rises sharply, minimizing the duration of simultaneous high v_{DS} and i_D.

To answer, the totem-pole driver improves switching performance by:

- Increasing peak gate charging and discharging current
- Reducing turn-on and turn-off delay times

Q2. Explain how the sourcing and sinking currents of the BJTs affect the switching speed.

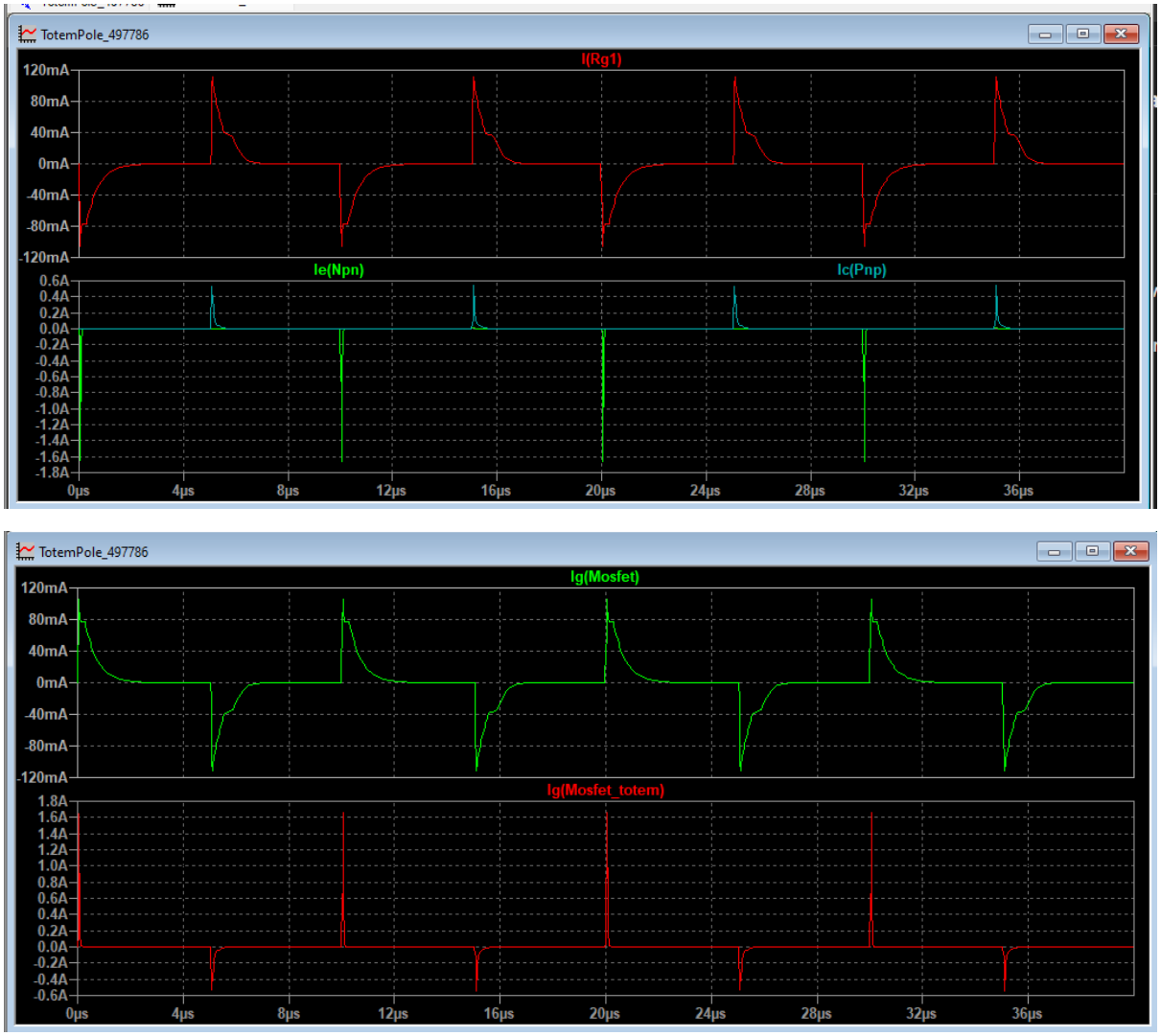


Fig.3 Sinking and Sourcing current comparison between both gate drivers

The switching speed of a MOSFET is strictly determined by how fast the Gate Driver can charge and discharge the parasitic input capacitance ($C_{iss} \approx C_{gs} + C_{gd}$).

$$dt = C_{iss} \cdot \frac{dV}{I_{gate}}$$

Therefore, higher current (I_{gate}) directly results in faster switching time (dt).

A. Sourcing Current (The Turn-ON Process)

- Totem Pole: NPN pumps current into the gate. Because of the transistor's current gain (β), it delivered a spike which charges C_{iss} instantly, allowing the gate voltage to pass the Miller Plateau and minimizing the time the MOSFET spends in the linear region, w

B. Sinking Current (The Turn-OFF Process)

- Totem Pole: PNP provides a low-impedance path to Ground, This allows the stored charge on the gate capacitors to dissipate with a high peak discharge current. This fast

discharge forces the gate voltage to drop below the threshold voltage immediately, making the MOSFET to turn off faster.

Q3.Analyze the effect of gate resistance Rg on:

(a) Switching speed

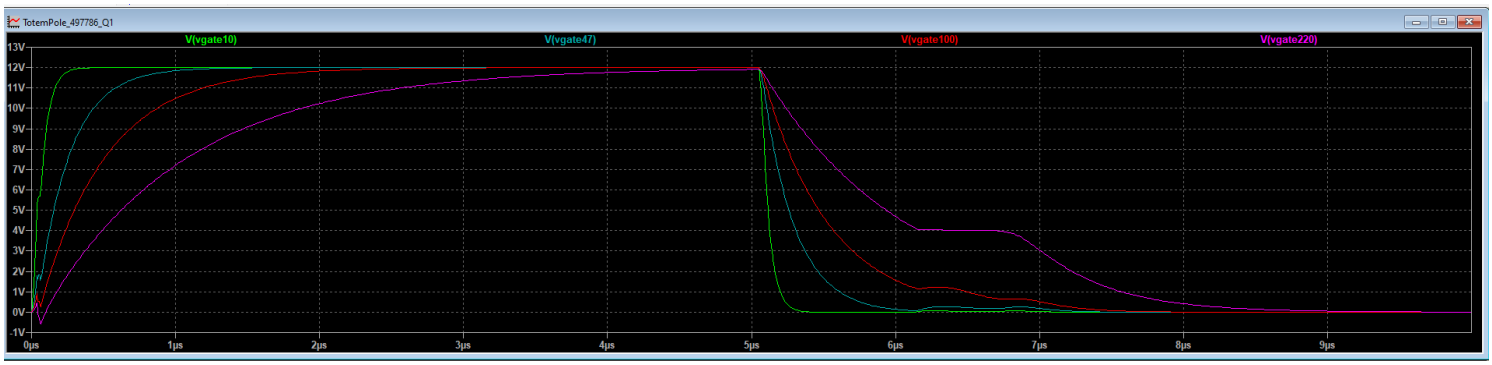


Fig.4 Rgate varying on the resistive gate driver

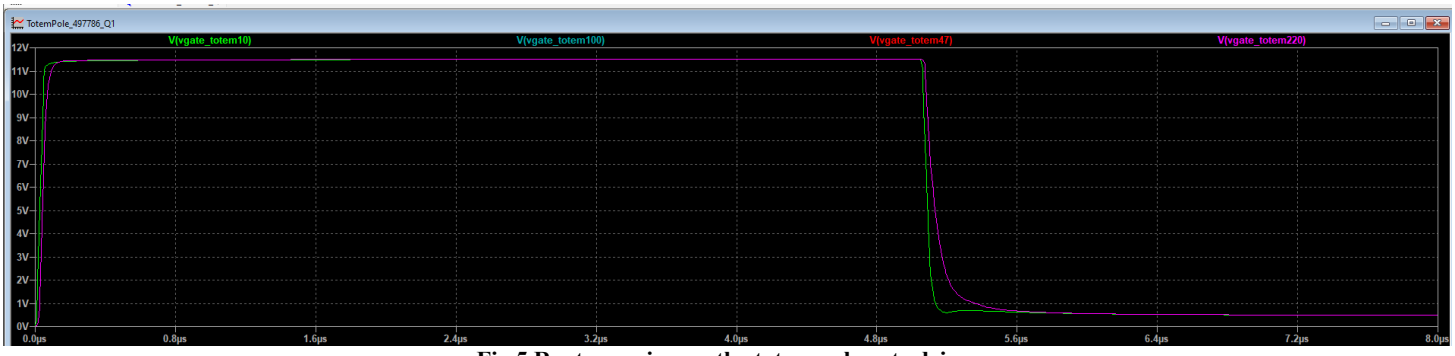


Fig.5 Rgate varying on the totem pole gate driver

Increasing R_g directly slows down the switching speed by increasing the time constant ($\tau = R_g C_{iss}$). The gate driver can deliver less current ($I_g = V_{drive}/R_g$) to charge the input capacitors.

(b) dv/dt and di/dt

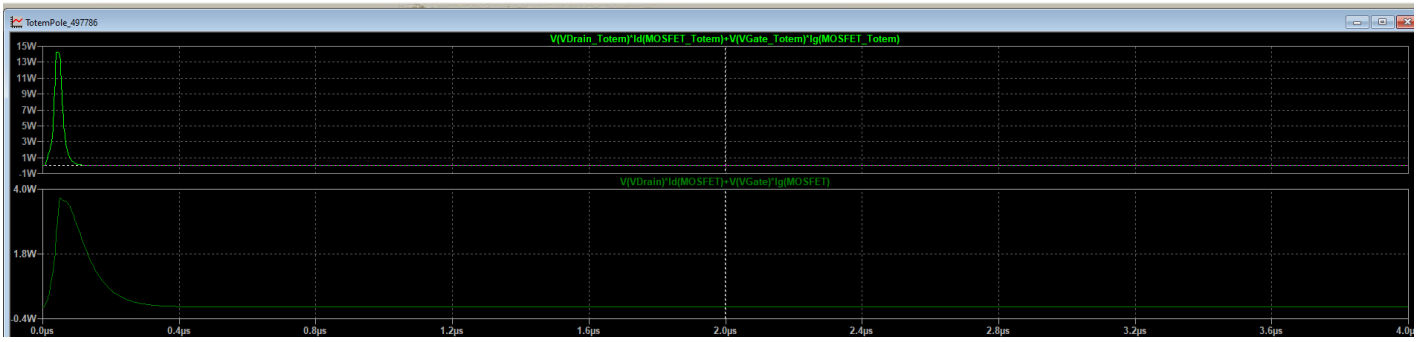


Fig.6 Power comparison for both gate drivers on Rgate = 10 Ω

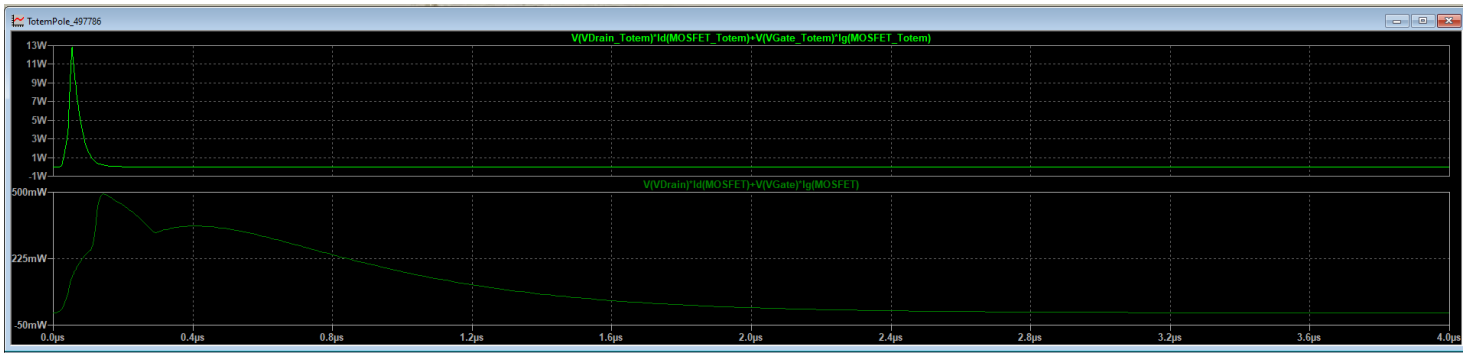


Fig.7 Power comparison for both gate drivers on Rgate = 100 Ω

Higher R_g reduces the rate of change of voltage (dv/dt) and current (di/dt). While this slows the device, it reduces the peak power stress and electromagnetic interference (EMI).

(c) Switching energy/losses

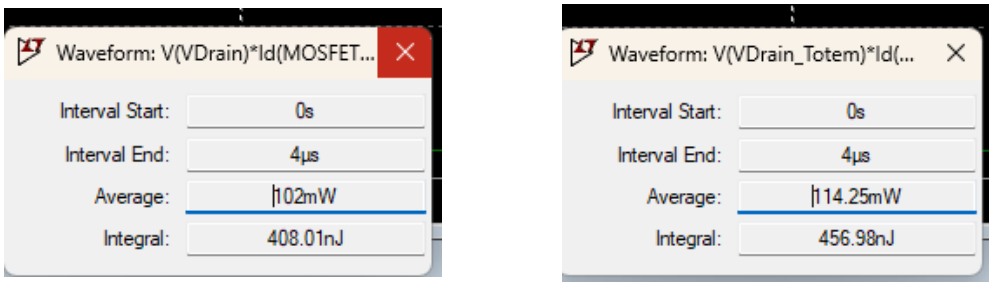


Fig.7 Switching Energy comparison for both gate drivers on Rgate = 10 Ω

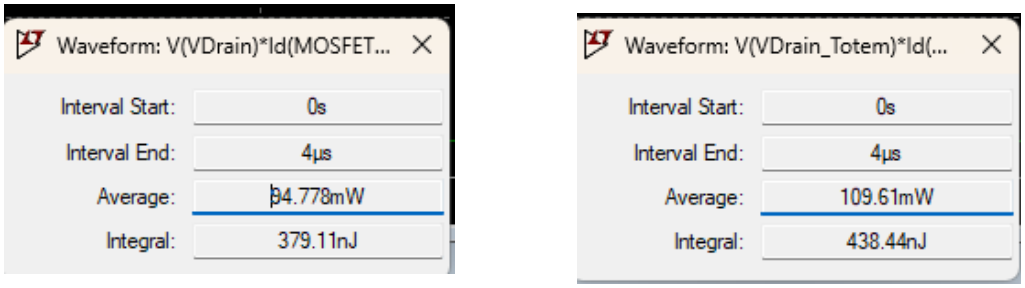


Fig.8 Switching Energy comparison for both gate drivers on Rgate = 100 Ω

Increasing R_g increases switching energy loss (E_{on}). Since the MOSFET lingers in the linear region (where both Voltage and Current are high) for a longer time, the integral of power ($\int v \cdot i, dt$) grows larger.

1.3 Hardware Prototyping

As requested in the exam, hardware prototype is used to validate simulation results.

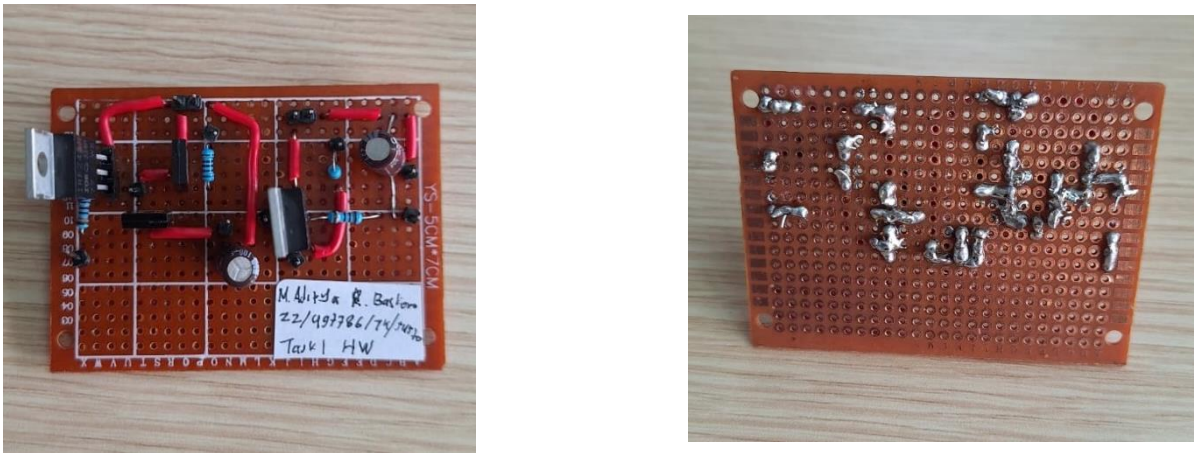


Fig.9 Hardware Prototype

Fig.10 Vgate plot using the resistive gate driver

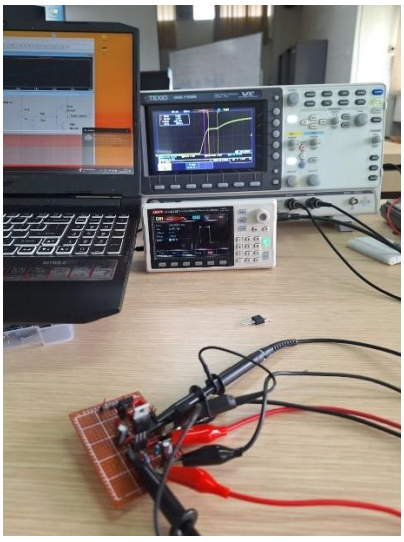


Fig.11 Experiment Setup

Fig.12 Vgate plot using the totem pole gate driver

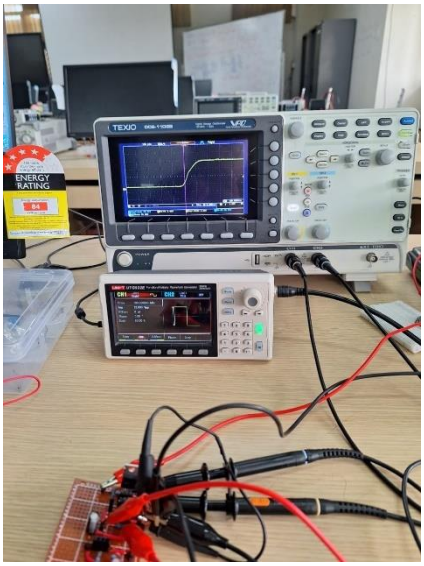


Fig.13 Experiment Setup

As shown in the experiment results, there is a distinguishable miller plateau on the resistive gate driver, this validates the phenomenon even in the hardware domain. Moreover, the miller plateau diminished on the totem pole gate driver as shown in Fig. 12. This shows the capability of the totem pole driver and verifies that the hardware prototype worked as intended.

TASK II

THREE CONVERTER TOPOLOGIES

2.1 Plot Output Voltage in Time and Frequency Domains For each inverter topology

(a) Generate the switching waveforms of the output voltage vo(t) using SPWM.

(b) Plot the time-domain waveform of the output voltage at different modulation indices ma (e.g., 0.6, 0.8, 1.0).

(c) Obtain the frequency-domain representation using FFT:

• Identify the fundamental component.

• Identify dominant switching harmonics.

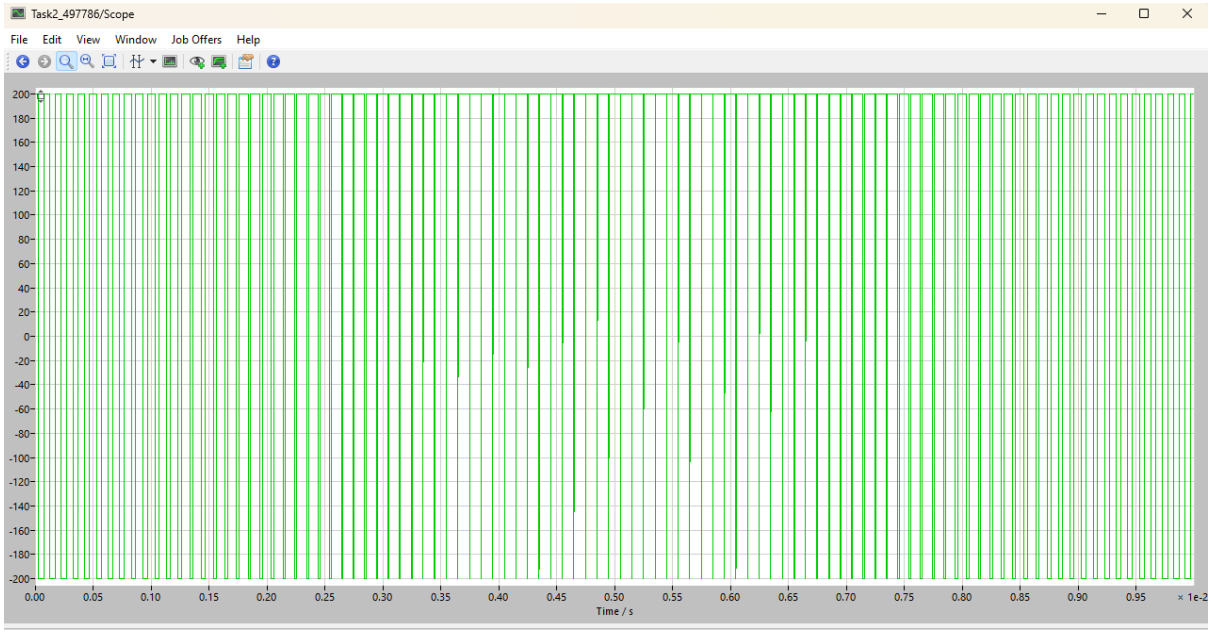
• Compare harmonic spectra among the three converter types.

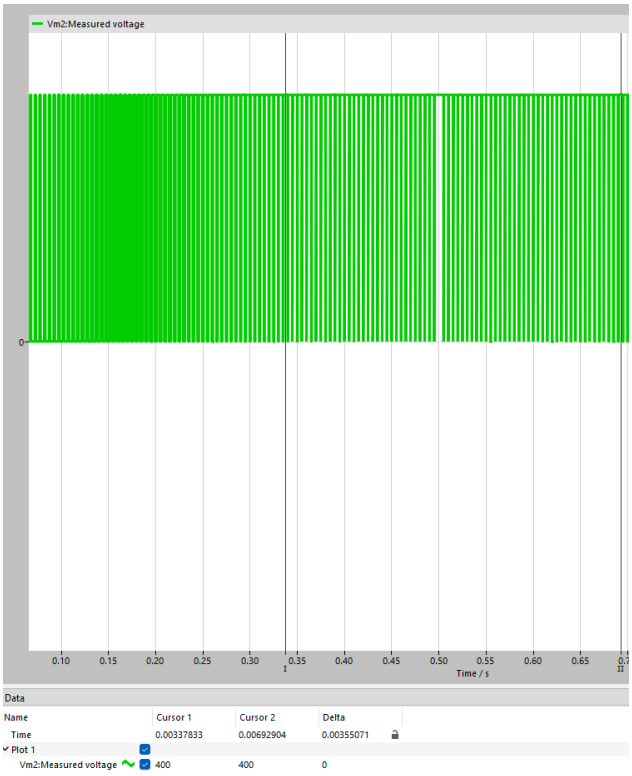
2.1.1 Design

For all topologies, Parameters used are given below :

- DC Link Voltage (V_{dc}): 400 V (standard bus voltage for 220V AC systems)
- Fundamental Frequency (f_1): 50 Hz (Indonesian Standard)
- Switching Frequency (f_{sw}): 10 kHz
- Load : Resistor $R = 60\ \Omega$

2.1.2 Switching waveforms





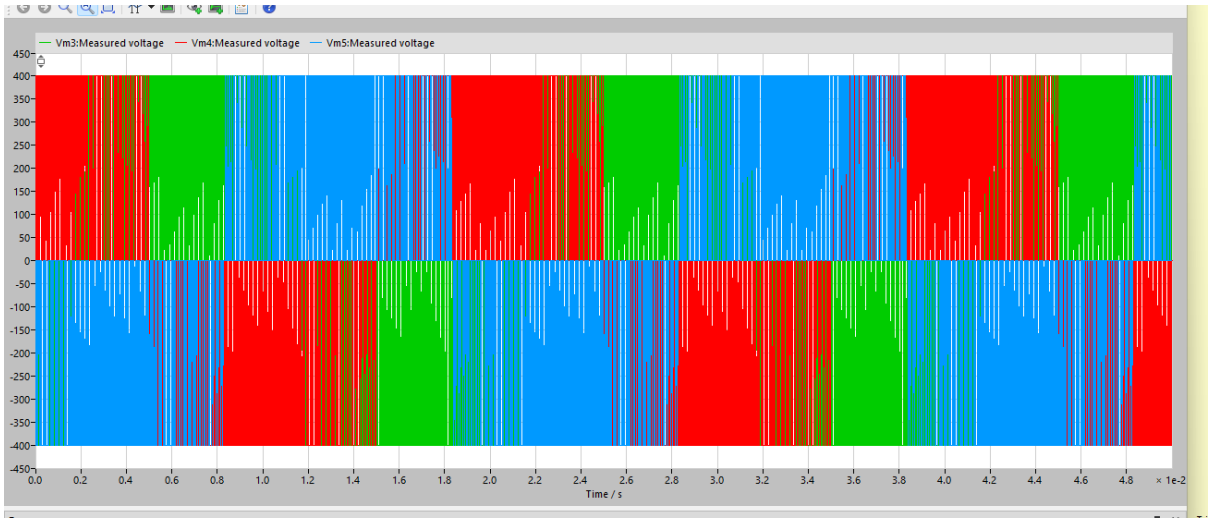
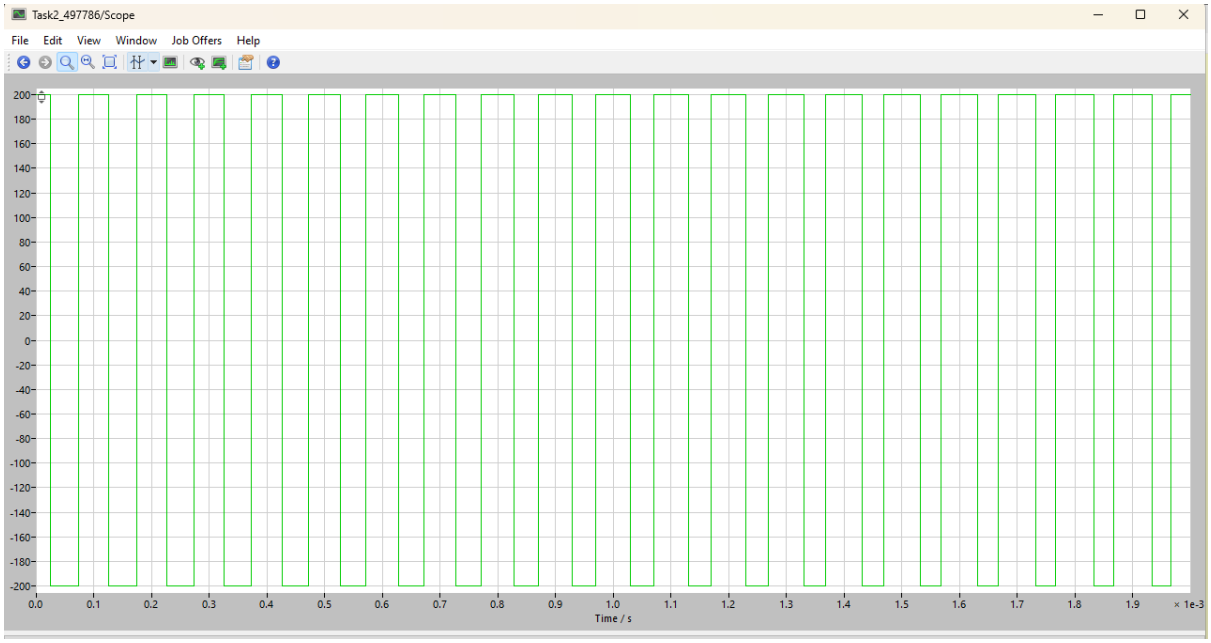
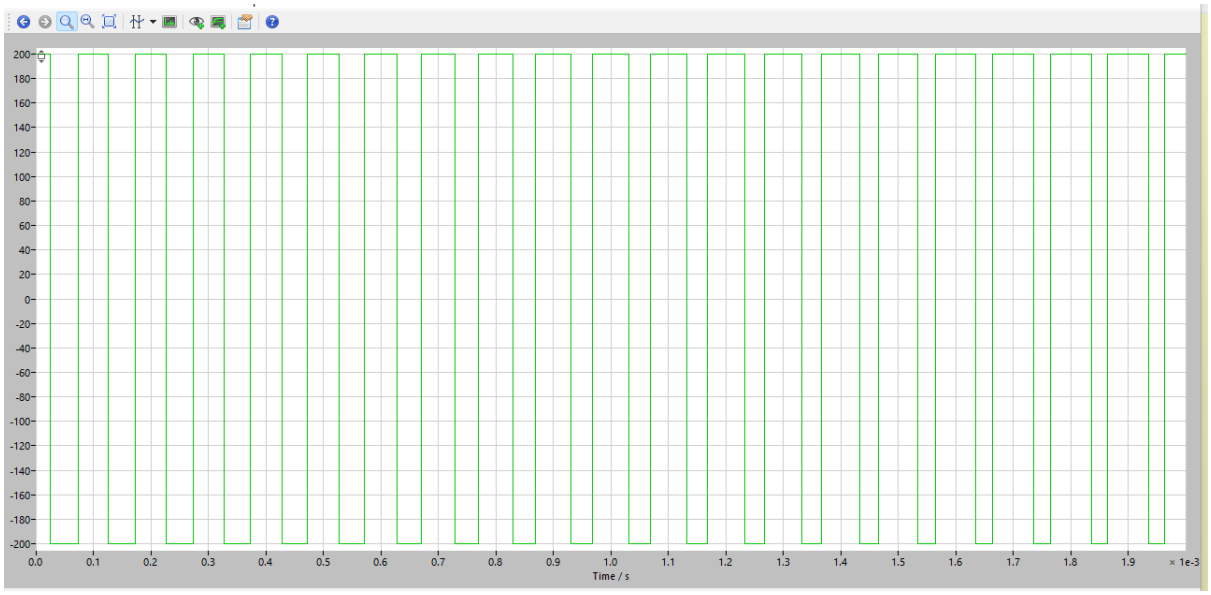


Fig.14 Switching waveforms for 3 topologies, Half Bridge (Top), Full Bridge (Middle), 3 Phase (Bottom)

m=0.6


Task2_497786/Scope
File Edit View Window Job Offers Help
Time / s
× 1e-3

m=0.8


Time / s
× 1e-3

m=1.0

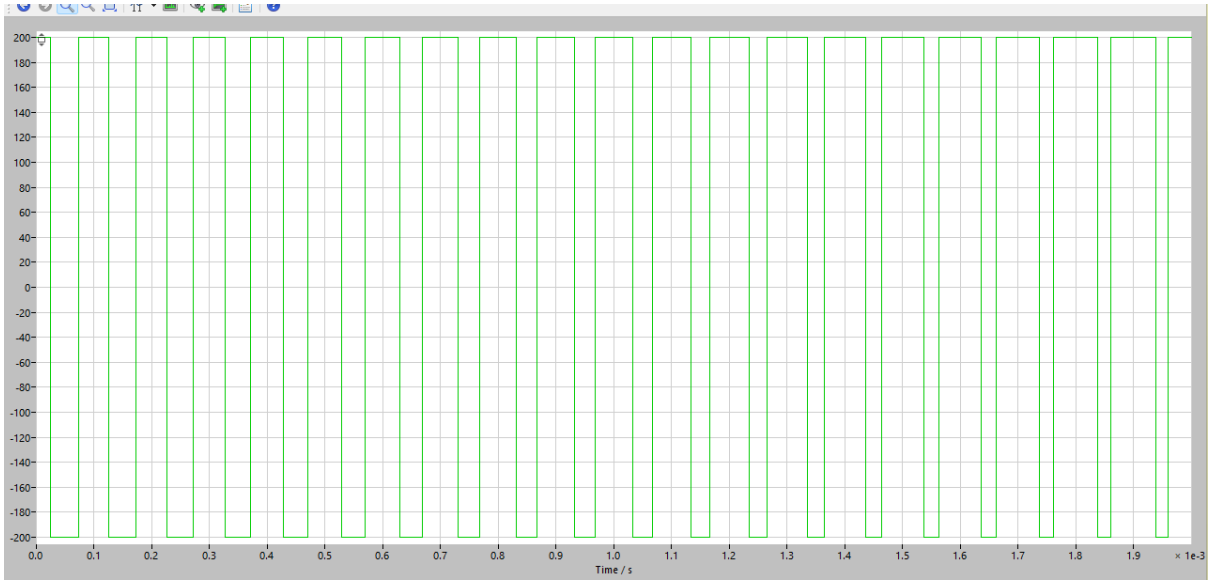


Fig.15 Modulation varying, 0.6 (Top), 0.8 (Middle), 1.0 (Bottom)

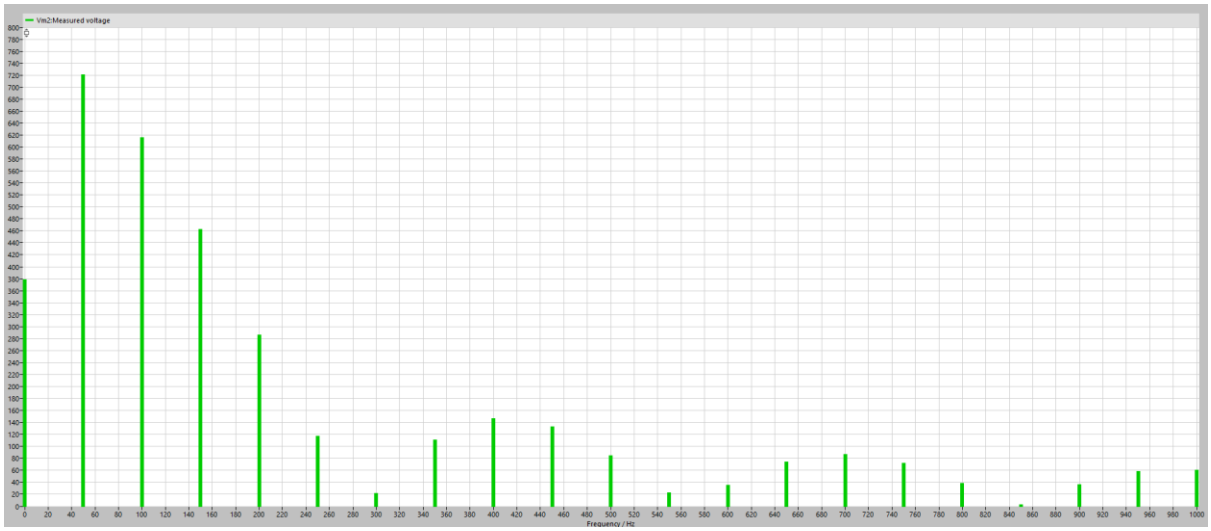


Fig.16 Modulation varying, 0.6 (Top), 0.8 (Middle), 1.0 (Bottom)

The FFT of the inverter output voltage shows a clear fundamental component at the reference frequency (50 Hz), which represents the desired sinusoidal output produced by SPWM. The amplitude of this fundamental increases proportionally with the modulation index, confirming correct modulation behavior.

In addition to the fundamental, the spectrum contains dominant switching harmonics centered around the switching frequency f_{sw} and its multiples. These harmonics appear as clusters with sidebands at $f_{sw} \pm nf_1$, which are characteristic of sinusoidal PWM. After the output LC filter is applied, the high-frequency switching harmonics are significantly attenuated, leaving the fundamental component dominant in the spectrum.

2.2 Second-order LC Filter Design

- Selected Topology: **Single-Phase Full-Bridge Inverter**
- Cutoff Frequency (f_c): using Rule of Thumb:

$$10f_1 < f_c < \frac{1}{10} f_{sw}$$

$$Range: 500\ \text{Hz} < f_c < 1000\ \text{Hz}$$

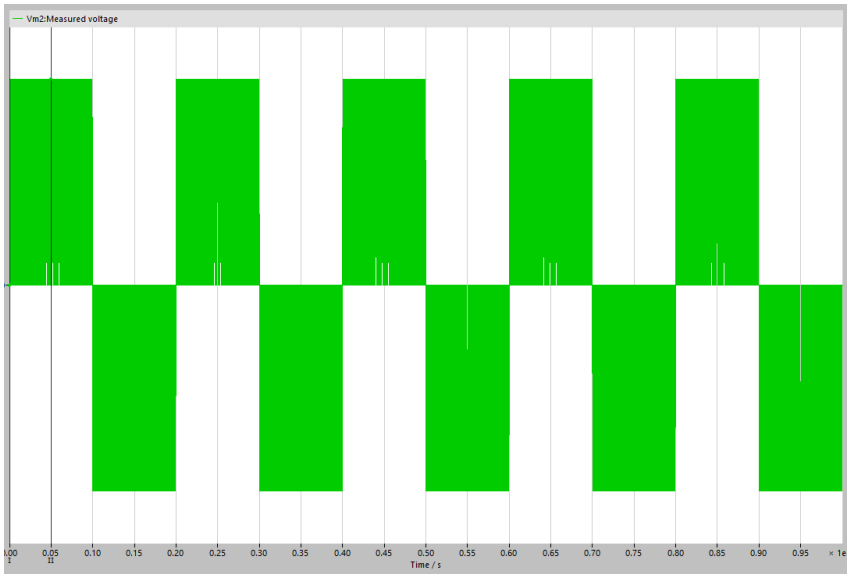
Pick: $f_c = 1$ kHz .

Design: $f_c = \frac{1}{2\pi\sqrt{LC}}$

With standard capacitor $C = 4.7\ \mu F$

$$L = \frac{1}{(2\pi f_c)^2 C} = \frac{1}{(2\pi \cdot 1000)^2 \cdot 4.7 \times 10^{-6}} \approx \mathbf{5.4}\ \text{mH}$$

Final Values: $L = 5.4$ mH, $C = 4.7\mu F$



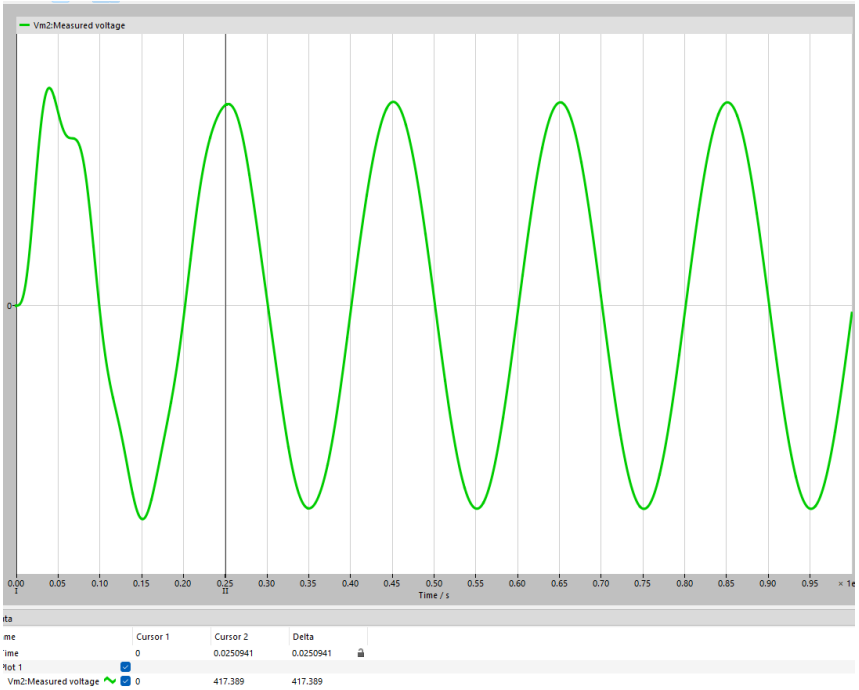


Fig.20 Unfiltered (Top) vs filtered (Bottom) Waveform

After the second-order LC filter is applied, the inverter output voltage transitions from a high-frequency PWM waveform to a smooth, near-sinusoidal signal. The switching ripple present in the unfiltered waveform is strongly attenuated, indicating effective suppression of high-frequency components around the switching frequency.

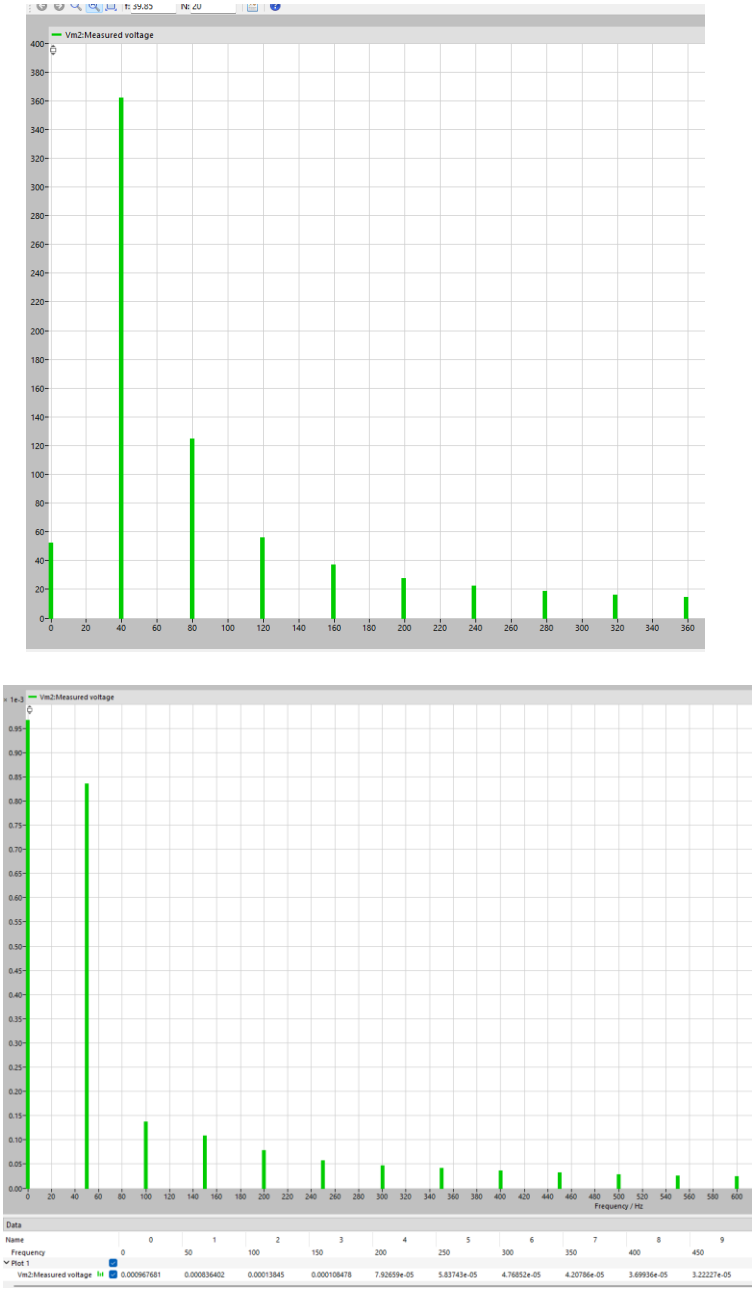


Fig.21 Unfiltered (Top) vs filtered (Bottom) FFT Plot

All higher-order harmonic components are significantly attenuated. Which are close to 0. The total harmonic distortion (THD) of the filtered output voltage is **below 8%**, with individual harmonic components remaining below **5% of the fundamental amplitude**. This satisfies typical academic and practical criteria for acceptable voltage waveform quality and is consistent with grid-interfacing limits such as those referenced in IEEE 519 for low-voltage systems.

The results confirm that the redesigned LC filter effectively suppresses both switching-frequency harmonics and dominant low-order harmonics while preserving the fundamental

component. The filtered output therefore represents a substantial improvement over the unfiltered case and demonstrates the intended function of the second-order output filter.

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