ECR6600 Pin MultiFunction

Revision history

Revision	Release Date	Summary
1.0	2021/4/14	Initial draft
2.0	2021/4/27	1：GPIO13 FUN4 change IRout to UART_TXD 2: GPIO16 FUN3 change bledebug0 to PWM_CTRL2
3.0	2021/5/13	1: Modify LX1 LX2 Definiation 2:Add ECR6600T pinmux
3.1	2021/6/3	1: Delete ECR6600T ResetB/TestMode Pinmux Function
4.0	2021/8/21	Delete 32Pin ECR6600 Package

ECR6600 Pin MultiFunction

ECR6600 QFN40 MultiFunction

40Pin_No（40）	Cell name	Driver	IO Power Domain	Reset input/output	IO 类型	Reset Value	function0		function1		function2		function3		function4		function5		function6	
							pin mux name	type	pin mux name	type	pin mux name	type	pin mux name	type	pinmux name	type	pinmux name	type	pinmux name	type
1	VDD_BAT			P	Vdd_bat1 and Vdd bat2,for RF BG, LP BG/LDO etc															
2	VDD_1p0RF			P	BUCK feedback															
3	GPIO23	4mA	VDDIO_33	wpd			SD_H_DATA1	I/O	GPIO23	I/O	UART1_RTS	O	PWM_CTRL1	O	I2S_TXSCK	I/O				
4	GPIO22	4mA	VDDIO_33	wpd			SD_H_DATA0	I/O	GPIO22	I/O	UART0_TXD	O	PWM_CTRL0	O	I2S_TXWS	I/O				
5	GPIO13	4mA	VDDIO_33	wpd			SD_H_CLK	O	GPIO13	I/O	UART2_TXD	O	I2C_SCL	TRI	I2S_RXD	I	dpll_80M_o	O		
6	GPIO21	4mA	VDDIO_33	wpd			SD_H_CMD	I/O	GPIO21	I/O	UART0_RXD	I	I2C_SDA	TRI	I2S_TXD	O				
7	GPIO25	4mA	VDDIO_33	wpd			SD_H_DATA3	I/O	GPIO25	I/O	phy_entrx	O	PWM_CTRL3	O	!phy_entrx	I/O	I2C_SDA	TRI		
8	GPIO24	4mA	VDDIO_33	wpd			SD_H_DATA2	I/O	GPIO24	I/O	UART1_CTS	I	PWM_CTRL2	O	I2S_MCLK	I				
9	GPIO17	4mA	VDDIO_33	wpd			WAKEUP	I	GPIO17	I/O	UART2_RXD	I	SPI1_WP	I/O	PWM_CTRL5	O	I2S_TXWS	I/O	bledebug2	
10	GPIO16		VDDIO_33	wpd			NC	I	GPIO16	I/O	UART1_CTS	I	ir_out	O	PWM_CTRL2	O				
11	XTAL_O			A																
12	XTAL_I			A																
13	VDD_0P8			P	digital power supply															
14	VDD_1P0			P	VDD_1p0，优先考虑不加磁珠，EVK 版本需要留个磁珠位置															
15	LX2			P	DCDC POWER Inductance L/ Regulator Power Supply for LDO mode															
16	LX1			P	DCDC POWER Inductance L/for LDO mode NC															
17	POWERKEY		VDDIO_33	Analog	Power Key		POWER_ON/OFF													
18	VDD_BUCK			P	VDD BUCK															
19	VDDIO			P	IO power 1.8V~3.3V															
20	VDD_EFUSE		Typical 1.8V	P	efuse program power .18V															
21	UART0_TXD		VDDIO_33	wpu	数模复用		UART0_TXD	O	GPIO6	I/O	COLD_RESET	O	32K_CLK_OUT		I2S_RXSCK	I/O	XTAL_O_32k	Analog		
22	UART0_RXD		VDDIO_33	wpu	数模复用		UART0_RXD	I	GPIO5	I/O	40M_CLK_OUT	O	ir_out	O	I2S_RXWS	I/O	XTAL_I_32k	Analog		
23	SD_DATA2	8mA	VDDIO_33	wpu			SD_DATA2	I/O	GPIO8	I/O	MSPI_HOLD	I/O								
24	SD_DATA3	8mA	VDDIO_33	wpu			SD_DATA3	I/O	GPIO7	I/O	MSPI_MOSI	I/O								
25	SD_CMD	8mA	VDDIO_33	wpu			SD_CMD	I/O	GPIO12	I/O	MSPI_WP	I/O								
26	SD_CLK	8mA	VDDIO_33	wpu			SD_CLK	I	GPIO9	I/O	MSPI_CLK	O								
27	SD_DATA0	8mA	VDDIO_33	wpu			SD_DATA0	I/O	GPIO11	I/O	MSPI_MISO	I/O								
28	SD_DATA1	8mA	VDDIO_33	wpu			SD_DATA1	I/O	GPIO10	I/O	MSPI_CS0	O								
29	TRST	4mA	VDDIO_33	wpd			TRST	I	GPIO4	I/O	UART0_RTS	O	SPI1_CS1	I/O	PWM_CTRL4	O	MSPI_CS1	O	bledebug7	
30	TDI	4mA	VDDIO_33	wpd			TDI	I	GPIO3	I/O	UART0_CTS	I	SPI1_MISO	I/O	PWM_CTRL3	O	I2C_SDA	TRI	bledebug6	
31	TDO	4mA	VDDIO_33	wpd			TDO	O	GPIO2	I/O	UART1_TXD	O	SPI1_MOSI	I/O	PWM_CTRL2	O	I2C_SCL	TRI	bledebug5	
32	TMS	4mA	VDDIO_33	wpd			TMS	I	GPIO1	I/O	UART1_RXD	I	SPI1_CS0	I/O	PWM_CTRL1	O	I2S_RXD	I	bledebug4	
33	TCK	4mA	VDDIO_33	wpd			TCK	I	GPIO0	I/O	UART2_TXD	O	SPI1_CLK	I/O	PWM_CTRL0	O	I2S_TXSCK	I/O	bledebug3	
34	GPIO18	4mA	VDDIO_33	wpu	数模复用		TestMode	I	ResetB	I/O	UART1_RTS	O	SPI1_HOLD	I/O	I2C_SCL	TRI	I2S_TXD	O	aux_3/vout_in	Analog
35	GPIO20		VDDIO_33	wpd	数模复用		PWM_CTRL3	O	GPIO20		aux_2/vout_ip	Analog	I2S_MCLK	I/O						
36	GPIO15		VDDIO_33	wpu	数模复用		BOOTMODE1	I	GPIO15	I/O	ATST_B/aux_1/vout_qn	Analog			PWM_CTRL5	O	I2S_TXWS	I/O		
37	GPIO14		VDDIO_33	wpu	数模复用		BOOTMODE0	I	GPIO14	I/O	ATST_A/aux_0/vout_qp	Analog			PWM_CTRL4	O	I2S_TXD	O		
38	VDD_DA			P	DA power															
39	VDD_PA			P	PA Power															
40	LNA			Analog																

ECR6600 Pin MultiFunction

ECR6600-TS2D QFN32 DCDC MultiFunction

32Pin_No	Cell name	Driver	IO Power Domain	Reset input/output	IO 类型	Reset Value	function0		function1		function2		function3		function4		function5		function6	
							pin mux name	type	pin mux name	type	pin mux name	type	pin mux name	type	pinmux name	type	pinmux name	type	pinmux name	type
1	VDD_BAT			P	Vdd_bat1 and Vdd bat2,for RF BG, LP BG/LDO etc															
2	VDD_1p0RF			P	BUCK feedback															
3	GPIO23	4mA	VDDIO_33	wpd			SD_H_DATA1	I/O	GPIO23	I/O	UART1_RTS	O	PWM_CTRL1	O	I2S_TXSCK	I/O	[illegible]	O		
4	GPIO22	4mA	VDDIO_33	wpd			SD_H_DATA0	I/O	GPIO22	I/O	UART0_TXD	O	PWM_CTRL0	O	I2S_TXWS	I/O				
5	GPIO13	4mA	VDDIO_33	wpd			SD_H_CLK	O	GPIO13	I/O	UART2_TXD	O	I2C_SCL	TRI	I2S_RXD	I	dpll_80M_o	O		
6	GPIO21	4mA	VDDIO_33	wpd			SD_H_CMD	I/O	GPIO21	I/O	UART0_RXD	I	I2C_SDA	TRI	I2S_TXD	O	[illegible]	I		
7	GPIO25	4mA	VDDIO_33	wpd			SD_H_DATA3	I/O	GPIO25	I/O	phy_entrx	O	PWM_CTRL3	O	phy_entrx	I/O	I2C_SDA	TRI		
8	GPIO24		VDDIO_33	wpd			SD_H_DATA2	I/O	GPIO24	I/O	UART1_CTS	I	PWM_CTRL2	O	I2S_MCLK	I	[illegible]	I		
9	GPIO17			A			WAKEUP	I	GPIO17	I/O	UART2_RXD	I	SPI1_WP	I/O	PWM_CTRL5	O	I2S_TXWS	I/O	bledebug2	
10	GPIO16			A			NC	I	GPIO16	I/O	UART1_CTS	I	ir_out	O	PWM_CTRL2	O				
11	XTAL_O			P																
12	XTAL_I			P																
13	VDD_0P8			P	digital power supply															
14	VDD_1P0			P	VDD_1p0，优先考虑不加磁珠，EVK 版本需要留个磁珠位置															
15	LX2		VDDIO_33	Analog	DCDC POWER Inductance L/for LDO mode Regulator Power Supply		POWER_ON/OFF													
16	LX1			P	DCDC POWER Inductance L/for LDO mode NC															
17	VDDIO/VDD_BUCK/PWR_KEY			P	IO power 1.8V~3.3V/VDD_BUCK/PWR_KEY															
18	VDD_EFUSE		Typical 1.8V	P	efuse program power .18V															
19	UART0_TXD		VDDIO_33	wpu	数模复用		UART0_TXD	O	GPIO6	I/O	COLD_RESET	O	32K_CLK_OUT		I2S_RXSCK	I/O	XTAL_O_32k	Analog		
20	UART0_RXD		VDDIO_33	wpu	数模复用		UART0_RXD	I	GPIO5	I/O	40M_CLK_OUT	O	ir_out	O	I2S_RXWS	I/O	XTAL_I_32k	Analog		
21	TRST	4mA	VDDIO_33	wpd			TRST	I	GPIO4	I/O	UART0_RTS	O	SPI1_CS1	I/O	PWM_CTRL4	O	MSPI_CS1	O	bledebug7	
22	TDI	4mA	VDDIO_33	wpd			TDI	I	GPIO3	I/O	UART0_CTS	I	SPI1_MISO	I/O	PWM_CTRL3	O	I2C_SDA	TRI	bledebug6	
23	TDO	4mA	VDDIO_33	wpd			TDO	O	GPIO2	I/O	UART1_TXD	O	SPI1_MOSI	I/O	PWM_CTRL2	O	I2C_SCL	TRI	bledebug5	
24	TMS	4mA	VDDIO_33	wpd			TMS	I	GPIO1	I/O	UART1_RXD	I	SPI1_CS0	I/O	PWM_CTRL1	O	I2S_RXD	I	bledebug4	
25	TCK	4mA	VDDIO_33	wpd			TCK	I	GPIO0	I/O	UART2_TXD	O	SPI1_CLK	I/O	PWM_CTRL0	O	I2S_TXSCK	I/O	bledebug3	
26	ResetB/TestMode	4mA	VDDIO_33	wpu	数模复用		TesrMode	I	ResetB	I										
27	GPIO20		VDDIO_33	wpd	数模复用		PWM_CTRL3	O	GPIO20		aux_2/vout_ip	Analog	I2S_MCLK	I/O						
28	GPIO15		VDDIO_33	wpu	数模复用		BOOTMODE1	I	GPIO15	I/O	ATST_B/aux_1/vout_qn	Analog			PWM_CTRL5	O	I2S_TXWS	I/O		
29	GPIO14		VDDIO_33	wpu	数模复用		BOOTMODE0	I	GPIO14	I/O	ATST_A/aux_0/vout_qp	Analog			PWM_CTRL4	O	I2S_TXD	O		
30	VDD_DA			P	DA power															
31	VDD_PA			P	PA Power															
32	LNA			Analog																

ECR6600 Pin MultiFunction

ECR6600-TS2L QFN32 LDO MultiFunction

32Pin_No	Cell name	Driver	IO Power Domain	Reset input/output	IO 类型	Reset Value	function0		function1		function2		function3		function4		function5		function6	
							pin mux name	type	pin mux name	type	pin mux name	type	pin mux name	type	pinmux name	type	pinmux name	type	pinmux name	type
1	VDD_BAT			P	Vdd_bat1 and Vdd bat2,for RF BG, LP BG/LDO etc															
2	VDD_1p0RF			P	BUCK feedback															
3	GPIO23	4mA	VDDIO_33	wpd			SD_H_DATA1	I/O	GPIO23	I/O	UART1_RTS	O	PWM_CTRL1	O	I2S_TXSCK	I/O				
4	GPIO22	4mA	VDDIO_33	wpd			SD_H_DATA0	I/O	GPIO22	I/O	UART0_TXD	O	PWM_CTRL0	O	I2S_TXWS	I/O				
5	GPIO13	4mA	VDDIO_33	wpd			SD_H_CLK	O	GPIO13	I/O	UART2_TXD	O	I2C_SCL	TRI	I2S_RXD	I	dpll_80M_o	O		
6	GPIO21	4mA	VDDIO_33	wpd			SD_H_CMD	I/O	GPIO21	I/O	UART0_RXD	I	I2C_SDA	TRI	I2S_TXD	O				
7	GPIO25	4mA	VDDIO_33	wpd			SD_H_DATA3	I/O	GPIO25	I/O	phy_entrx	O	PWM_CTRL3	O	!phy_entrx	I/O	I2C_SDA	TRI		
8	GPIO24		VDDIO_33	wpd			SD_H_DATA2	I/O	GPIO24	I/O	UART1_CTS	I	PWM_CTRL2	O	I2S_MCLK	I	dpll_80M_o	O		
9	GPIO17	4mA	VDDIO_33	wpd			WAKEUP	I	GPIO17	I/O	UART2_RXD	I	SPI1_WP	I/O	PWM_CTRL5	O	I2S_TXWS	I/O	bledebug2	
10	GPIO16		VDDIO_33	wpd			NC	I	GPIO16	I/O	UART1_CTS	I	ir_out	O	PWM_CTRL2	O				
11	XTAL_O			A																
12	XTAL_I			A																
13	VDD_0P8			P	digital power supply															
14	VDD_1P0			P	VDD_1p0，优先考虑不加磁珠，EVK 版本需要留个磁珠位置															
15	LX2			P	DCDC POWER Inductance L/for LDO mode Regulator Power Supply															
16	VDD_BUCK/POWER_KEY			P	VDD_BUCK/PWR_KEY															
17	VDDIO			P	IO power 1.8V~3.3V															
18	VDD_EFUSE		Typical 1.8V	P	efuse program power .18V															
19	UART0_TXD		VDDIO_33	wpu	数模复用		UART0_TXD	O	GPIO6	I/O	COLD_RESET	O	32K_CLK_OUT		I2S_RXSCK	I/O	XTAL_O_32k	Analog		
20	UART0_RXD		VDDIO_33	wpu	数模复用		UART0_RXD	I	GPIO5	I/O	40M_CLK_OUT	O	ir_out	O	I2S_RXWS	I/O	XTAL_I_32k	Analog		
21	TRST	4mA	VDDIO_33	wpd			TRST	I	GPIO4	I/O	UART0_RTS	O	SPI1_CS1	I/O	PWM_CTRL4	O	MSPI_CS1	O	bledebug7	
22	TDI	4mA	VDDIO_33	wpd			TDI	I	GPIO3	I/O	UART0_CTS	I	SPI1_MISO	I/O	PWM_CTRL3	O	I2C_SDA	TRI	bledebug6	
23	TDO	4mA	VDDIO_33	wpd			TDO	O	GPIO2	I/O	UART1_TXD	O	SPI1_MOSI	I/O	PWM_CTRL2	O	I2C_SCL	TRI	bledebug5	
24	TMS	4mA	VDDIO_33	wpd			TMS	I	GPIO1	I/O	UART1_RXD	I	SPI1_CS0	I/O	PWM_CTRL1	O	I2S_RXD	I	bledebug4	
25	TCK	4mA	VDDIO_33	wpd			TCK	I	GPIO0	I/O	UART2_TXD	O	SPI1_CLK	I/O	PWM_CTRL0	O	I2S_TXSCK	I/O	bledebug3	
26	ResetB/TestMode	4mA	VDDIO_33	wpu	数模复用		TestMode	I	ResetB	I										
27	GPIO20		VDDIO_33	wpd	数模复用		PWM_CTRL3	O	GPIO20		aux_2/vout_ip	Analog	I2S_MCLK	I/O						
28	GPIO15		VDDIO_33	wpu	数模复用		BOOTMODE1	I	GPIO15	I/O	ATST_B/aux_1/vout_qn	Analog			PWM_CTRL5	O	I2S_TXWS	I/O		
29	GPIO14		VDDIO_33	wpu	数模复用		BOOTMODE0	I	GPIO14	I/O	ATST_A/aux_0/vout_qp	Analog			PWM_CTRL4	O	I2S_TXD	O		
30	VDD_DA			P	DA power															
31	VDD_PA			P	PA Power															
32	LNA			Analog																