ESWIN

ECR6600 Datasheet

802.11b/g/n/ax Wi-Fi6 1T1R WLAN + BLE SOC

Beijing ESWIN Computing Technology Co. Ltd

Tel: 010- 56800992

www.eswin.com

Copyright

Disclaimer

The contents of this document are subject to revision without notice due to continued progress in methodology, design and manufacturing. ESWIN shall have no liability for any error of damage of any kind resulting from the use of this document.

Trademarks

ESWIN® is registered trademarks of Beijing ESWIN Computing Technology Co. Ltd.
All other trademarks are the property of their respective owners.

Revision History

Table 1 Revision History

Revision	Date	Description	Author
1.0	2021/01/29	Initial draft	Wang Qi
1.1	2021/03/17	Update performance data, temperature Add BLE performance data	Wang Qi
1.2	2021/04/27	Update package and pin list	Wang Qi
1.3	2021/05/19	Add ECR6600-TS2D/TS2L package and pin description.	Wang Qi
1.4	2021/06/08	Update pin description, BLE description, and the block diagram of the chip	Wang Qi
1.5	2021/06/22	Add TX Maximum output power	Wang Qi
1.6	2021/09/02	Remove ECR6600-S2D/S2L	Liu Jianxiang

Contents

1 Product Overview

This chapter introduces the ECR6600 and corresponding features.

1.1 General Description

ESWIN ECR6600 series is a highly integrated single-chip low power 802.11ax Wireless LAN (WLAN) and BLE controllers. The chip combines the modules including High-performance Andes D10 MCU, WLAN MAC, 1T1R capable WLAN baseband, RF, and Bluetooth, etc. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for variant applications and control use.

ECR6600 series integrates internal memories to support Wi-Fi protocol functions and provides simple application developments via the embedded memory configuration.

1.1.1 Wi-Fi Features

ECR6600 series supports the following Wi-Fi features:

- Support of Full MAC (LMAC+UMAC)
- Support of Access Point (AP), station (STA) and Wi-Fi Direct modes in 11ax/b/g/n mode
- Support of WEP, WPA, WPA2, WPA3 (Personal and Enterprise modes)
- Support of WMM QoS
- WPS
- All guard interval (0.8/1.6/3.2 us)

- Support of 802.11ax MCS0 up to MCS7
- Maximal bit-rate of 150 Mbps
- Support of MU-OFDMA in UL and DL as a non-AP STA
- Support of Beamforming as a STA (beamformee)
- Support of Mid-amble
- Support 20M and 40M bandwidth
- Support of DCM

1.1.2 BLE Features

ECR6600 series supports the following BLE features:

- BLE5.1
- Support BLE and BT multi-device connection
- Supports simultaneous broadcast of packages and scanning
- Enhanced Power Control
- The output power is up to +10 dBm
- Adaptive frequency hopping (AFH)
- Simultaneous advertising and scanning
- Supports asynchronous data sending and receiving
- Supports connection parameter update
- Supports extend packet length
- Supports link layer encryption
- Supports LE Ping

1.1.3 MCU Features

ECR6600 series has the following MCU features:

- MCU up to 240MHz
- XIP
- RAM direct mapping to data
- RAM space Multiplexing program download and JTAG interface
- 50 MHz SDIO interface
- SPI interface
- Dual I2C interface
- Dual high speed UART with flow control capability
- Six 32-bit timers and one always on timer
- Six 32-bit PWM with either high-speed clock or low power clock
- Microphone signal amplify (to be confirmed)
- Multi-channel ADC with high speed 10-bits or low speed 16-bits with internal decimation filter
- 1 Kbit eFuse
- True random number generator
- Support of 26 MHz and 40 MHz Crystal

1.2 Block Diagram

Figure 1.1 shows the major physical blocks in the ECR6600 series.

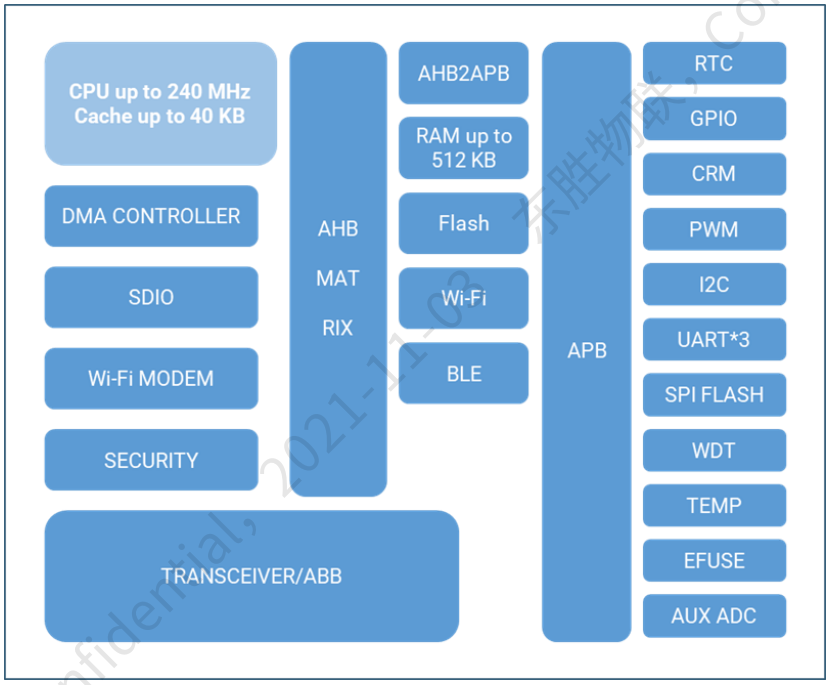


Figure 1.1 SoC Block Diagram

1.3 Power Supply Diagram

Figure 1.2 shows the typical power supply of the ECR6600 series.

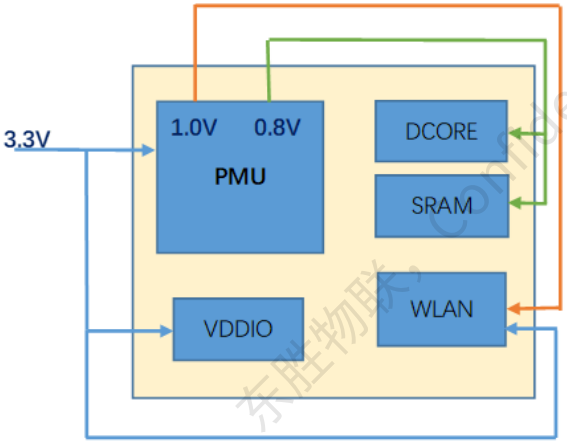


Figure 1.2 Power Supply Diagram

2 SoC Working Mode

2.1 Deep Sleep Mode

In deep sleep mode, the chip costs less power, because it shuts down the DCDC and all analog circuit part. When ECR6600 series chip is in deep sleep mode, internal RTC and external GPIO interrupt source can wake it up.

2.2 Light Sleep Mode

In light sleep mode, the chip maintains the instruction set and data memory, while shut down the other parts of SoC. When ECR6600 is in light sleep mode, the internal RTC or external GPIO interrupt source can wake it up, and then the MPU works immediately. The wake-up process costs only one millisecond.

2.3 CPU Sleep Mode

CPU sleep mode switches off the whole logical circuit, including the RF part, but the PMU and DCXO still works. In this mode, leakage is the only power consumption source.

When ECR6600 is in CPU sleep mode, the RTC and GPIO external interrupt can wake it up. The wake-up process costs several milliseconds.

2.4 IDLE Mode

The IDLE mode that is called WFI mode, powers up the whole chip. When ECR6600 is in IDLE mode, it can recover from IDLE mode and enter RUN

mode if any interrupt occurs.

2.5 RUN Mode

In RUN mode, every module works at its designed frequency, or can be controlled by the gate according to the specific scenario. In this mode, every module can receive and transmit data as needed.

2.6 WAKEUP Source

ECR6600 series has the following wakeup sources:

- RTC timer interrupt
- Rising edge of WAKEUP pin interrupt (long press)
- Rising edge of WAKEUP pin interrupt (short press)
- Keyon turn to low

3 Hardware Description

3.1 DMA Channel

The DMA controller provides 13 handshake pairs for the following transmissions:

- Memory-to-peripheral
- Peripheral-to-memory
- SDIO buffer-to-memory
- Memory -to- SDIO buffer
- Memory -to-MAC buffer
- MAC buffer-to-memory
- Peripheral-to-peripheral

3.2 UART Controller

- AMBA 2.0 APB interface for registers access
- Hardware configurable 16, 32, 64 and 128 bytes transmit/receive FIFO
- Programmable over-sampling frequency (even multiples ranging from 8x to 32x). Programming sequence is compatible with the 16C550D UART.
- Supports 5 to 8 bits per character
- Supports 1, 1.5 and 2 STOP bits
- Supports even, odd and stick parity bits
- Supports DMA function

- Supports programmable baud rate
- Supports modem control interface
- Supports complete status reporting capabilities
- Supports line breaks, parity errors, framing errors and data overrun detection

3.3 IIC Controller

- Supports AMBA 2.0 APB bus
- Supports Standard-mode (100 Kb/s) and Fast-mode (400 Kb/s) protocols
- Programmable Master/Slave mode
- Supports 7-bit and 10-bit addressing mode
- Supports general call address
- Auto clock stretching
- Programmable clock/data timing
- Supports Direct Memory Access (DMA)

3.4 SPI Controller

- Compliant with AMBA 2 AHB protocol specification
- Compliant with AMBA 3 APB protocol specification
- Support of MSB/LSB first transfer
- Support of Direct Memory Access (DMA) data transfer
- Support of programmable SPI SCLK
- Support of memory-mapped access (read-only) through AHB bus or

EILM bus

- Support of SPI slave mode
- Configurable Dual and Quad I/O SPI interfaces
- Configurable TX/RX FIFO depth (The depth can be 2, 4, 8 or 16)
- Configurable programming port location on AHB/APB/EILM interfaces

3.5 SDIO Controller

This SDIO can act as SDIO/SD/MMC host or SDIO/SD/MMC device, connecting to SDIO device or SDIO host, respectively. Andes D10 can write or read SDIO register.

3.6 Programmable Interval Timer

- Supports AMBA 2.0 APB bus
- Supports up to four multi-function timers
- Each multi-function timer provides six usage scenarios (combinations of the timer and PWM)
- Programmable source of timer clock
- Timers can pause with external interrupt

3.7 AUX-ADC

- Large input voltage ranges 0-3.3 V
- Large input resistance, at least 1 Mohm
- Single ended input or differential input

- Measurement error, <±20mV
- Smaller area
- Self-calibration

3.8 Watchdog Timer Controller

- Supports AMBA 2.0 APB bus
- Provides combinations of interrupt and reset when the watchdog timer expires
- Provides a write-protection mechanism for the Control/Restart Registers
- Programmable source of timer clock
- Configurable magic numbers for write-protection of registers and restart of the timer
- Watchdog timer can pause with external interrupt

3.9 Real-time Clock

- APB interface for register accesses
- Configurable counter size
- Periodic interrupts: half-second, second, minute, hour, and day
- Programmable alarm interrupt
- Hardware digital trimming to compensate for inaccuracies of the external clock source

3.10 Interrupt Source

ECR6600 supports up to 32 interrupt sources, which are used for the following peripherals:

- UART
- IIC
- SPI
- WDT
- PIT
- WIFI

4 Specifications

4.1 Recommended Operating Conditions

Table 4.1 Operating Conditions

Parameter	Pin Name	Minimum	Typical	Maximum	Unit
Operating voltage	VBAT-pin	3	3.3	3.6	V
Operating temperature		-40		105	℃

4.2 Current Consumption

Table 4.2 Current Consumption Performance Specification

Test Condition	Minimum	Typical	Maximum	Unit
TX 802.11b, CCK 1Mbps, POUT=+17dBm		246		mA
TX 802.11b, CCK 11Mbps, POUT=+17dBm		242		mA
TX 802.11b, CCK 1Mbps, POUT=+20dBm		270		mA
TX 802.11b, CCK 11Mbps, POUT=+20dBm		266		mA
TX 802.11g, OFDM 6Mbps, POUT=+17dBm		208		mA
TX 802.11g, OFDM 54Mbps, POUT=+14dBm		169		mA
TX 802.11g, OFDM 54Mbps, POUT=+17dBm		192		mA
TX 802.11n, MCS0, POUT=+17dBm		210		mA
TX 802.11n, MCS7, POUT=+13dBm		181		mA

Test Condition	Minimum	Typical	Maximum	Unit
TX 802.11n, MCS7, POUT=+17dBm		204		mA
TX 802.11ax, MCS7, POUT=+13dBm		174		mA
TX 802.11ax, MCS7, POUT=+17dBm		210		mA
TX 802.11ax, MCS0, POUT=+17dBm		204		mA
RX 802.11b, -80dBm		30.9		mA
RX 802.11g, -70dBm		30.6		mA
RX 802.11n, -65dBm		30.3		mA
RX 802.11ax		30.3		mA
Light sleep mode		50		uA
Deep sleep mode		6.5		uA
DTIM1		3		mA
DTIM3		1		mA
SHUTDOWN		< 1		uA
TX BLE,POUT = 10 dBm		100		mA
RX BLE		30		mA

4.3 DC Electrical Characteristics

Table 4.3 DC Electrical Specification

Parameter		Minimum	Nominal	Maximum	Unit
C_{IN} Pin capacitance			2		pf
V_{IH} High-level input voltage		0.7vdd		vdd	V
V_{IL} Low-level input voltage		0		0.3vdd	
I_{IH} High-level input current		-10		10	uA
I_{IL} Low-level input current		-10		10	uA
V_{OH} High-level output voltage		0.9vdd			V
V_{OL} Low-level output voltage				0.1vdd	V
I_{OH} High-level source current	4 mA	2	3.2	5	mA

I_{OL} Low-level sink current	4 mA	4	5.2	7	mA
R_{PU} Pull-up resistor		66K	81.1k	110k	Ω
R_{PD} Pull-down resistor		55k	62.7k	82.5k	Ω

4.4 WLAN Receiver Characteristics

Table 4.4 WLAN Receiver Performance Specification

Parameters	Condition	Minimum	Typical	Maximum	Unit
Sensitivity	802.11b 1M		-96		dBm
	802.11b 11M		-88		dBm
	802.11g 54M		-76		dBm
	802.11n MCS7 HT20		-72		dBm
	802.11n MCS7 HT40		-69		dBm
	802.11ax MCS7 HT20		-71		dBm

4.5 WLAN Transmitter Characteristics

Table 4.5 WLAN Transmitter Performance Specification

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Power control rang			6		dB
Power control resolution			1		dB
Max output power	802.11b 11Mbps		17	20	dBm
	802.11g 54Mbps		14	17	dBm
	802.11n HT20 MCS7		13	16.9	dBm
	802.11n HT40		13	17.2	dBm

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
	MCS7				
	802.11ax HT20 MCS7		13	16.9	dBm
EVM	802.11n HT20 MCS7		-30		dB
	802.11ax HT20 MCS7		-30		dB

4.6 BLE RX Performance

Table 4.6 BLE Receiver Performance Specification

Test Item		Standard (dBm)	Channel(dBm)		
			CH0	CH19	CH39
Sensitivity >30% packet	1Mbps	-70	-93.5	-93	-92.8
	2Mbps	-70	-91	-91	-91

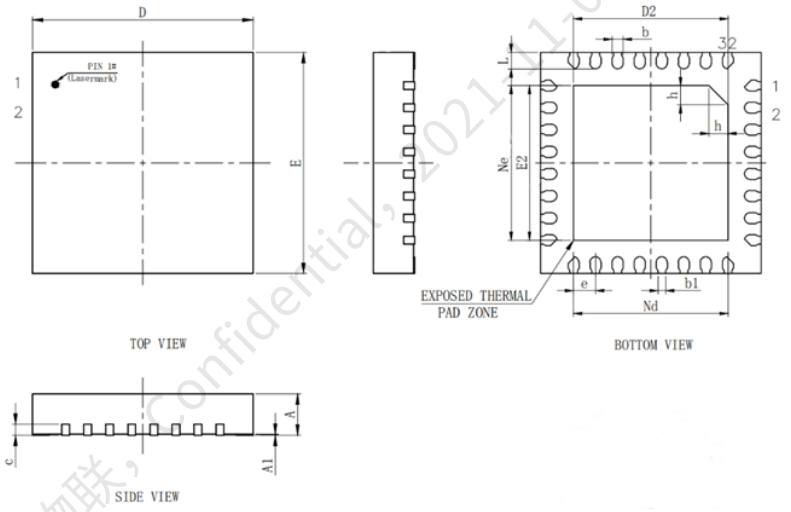
4.7 BLE TX Performance

Table 4.7 BLE Transmitter Performance Specification

Test Item		Standard (dBm)	Channel(dBm)		
			CH0	CH19	CH39
Output power	PAVG	10 V±1 V	10.25	10.19	9.59
	PPK	10 V±1 V	10.99	10.91	10.3

5 Package Information

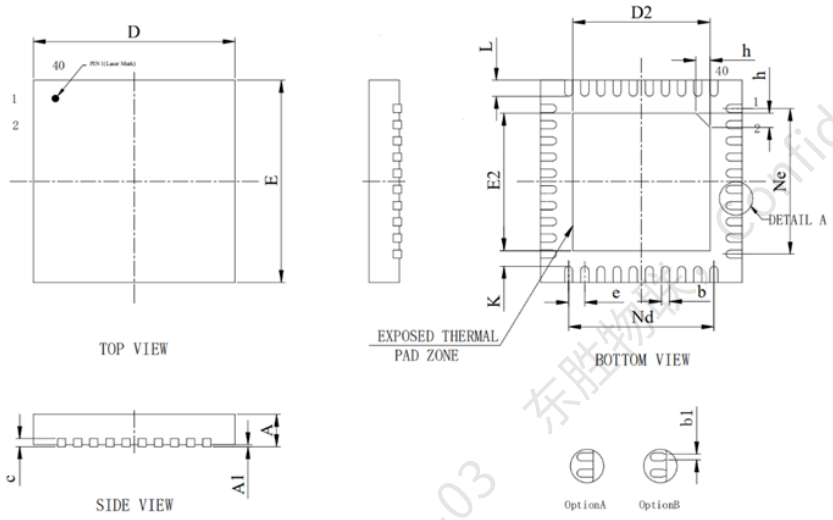
ECR6600 series had two packages, QFN32 and QFN 40. Figure 5.1 shows the mechanical drawing for the QFN32 package.



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	△
	0.85	0.90	0.95	△
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.14REF			
c	0.18	0.20	0.25	
D	3.90	4.00	4.10	
D2	2.70	2.80	2.90	
e	0.40BSC			
Ne	2.80BSC			
Nd	2.80BSC			
E	3.90	4.00	4.10	
E2	2.70	2.80	2.90	
L	0.25	0.30	0.35	
h	0.30	0.35	0.40	
L/F载体尺寸	122X122			

Figure 5.1 QFN32L/D Package

Figure 5.2 shows the mechanical drawing for the QFN40 packages.



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	3
	0.85	0.90	0.95	4
A1	—	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.14REF			
c	0.18	0.20	0.25	
D	4.90	5.00	5.10	
D2	3.30	3.40	3.50	
e	0.40BSC			
Nd	3.60BSC			
E	4.90	5.00	5.10	
E2	3.30	3.40	3.50	
Ne	3.60BSC			
L	0.35	0.40	0.45	
K	0.20	—	—	
h	0.30	0.35	0.40	
L/F载体尺寸 (mil)	150*150			

Figure 5.2 QFN40L/D Package

5.1 Pinout (Top View)

Figure 5.3 shows the pinout of ECR6600-40D/40L with 40-pin QFN.

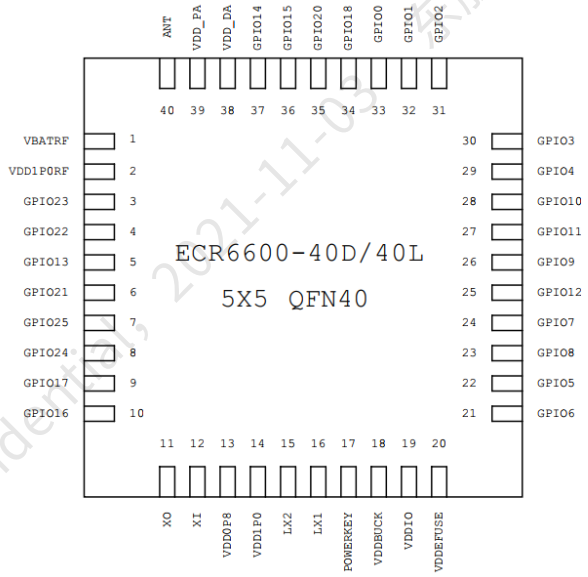


Figure 5.3 ECR6600-40D/40L 40-pin QFN

Figure 5.4 shows the pinout of ECR6600-TS2D with 32-pin QFN.

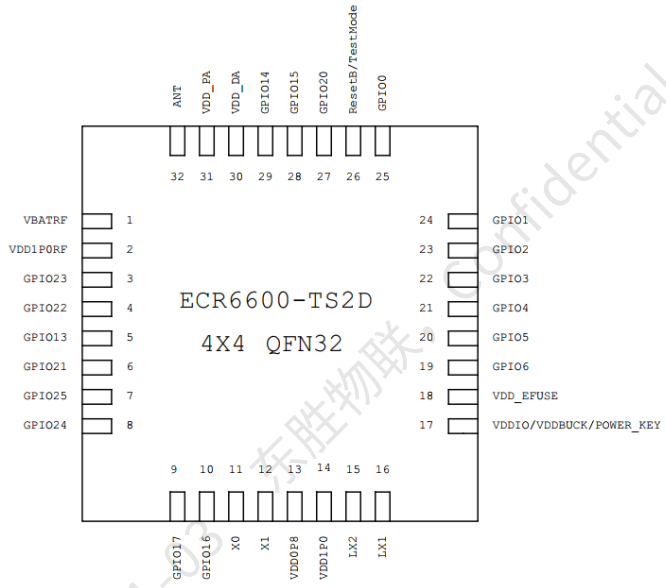


Figure 5.4 ECR6600-TS2D 32-pin QFN

Figure 5.5 shows the pinout of ECR6600-TS2L with 32-pin QFN.

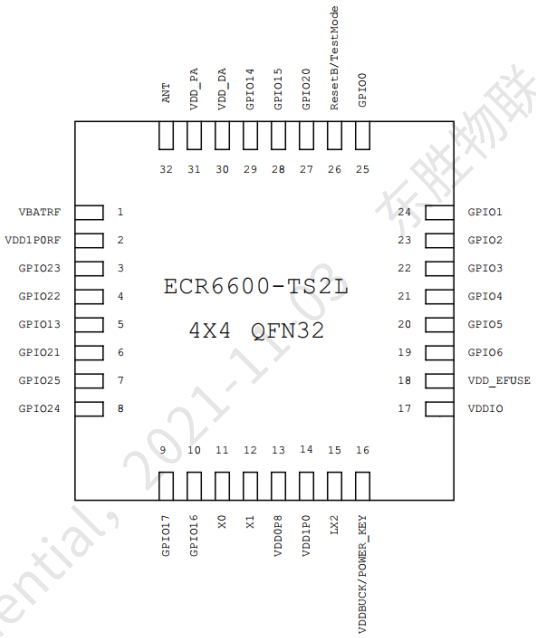


Figure 5.5 ECR6600-TS2L 32-pin QFN

5.2 Pin Description

Table 5.1 ECR6600-40D/40L QFN40 Pin Description

Pin	Name	Description
1	VDD_BAT	VDD_BAT1 and VDD BAT2, for RF BG, LP BG/LDO ETC
2	VDD_1p0RF	BUCK feedback
3	GPIO23	SD_H_DATA1/UART1_RTS/PWM_CTRL1/I2S_TXSCK
4	GPIO22	SD_H_DATA0/UART0_TXD/PWM_CTRL0/I2S_TXWS
5	GPIO13	SD_H_CLK/UART2_TXD/ I2C_SCL/I2S_RXD
6	GPIO21	SD_H_CMD/UART0_RXD/I2C_SDA/I2S_TXD
7	GPIO25	SD_H_DATA3/PWM_CTRL3/I2C_SDA
8	GPIO24	SD_H_DATA2/UART1_CTS/PWM_CTRL2/I2S_MCLK
9	GPIO17	WAKEUP/UART2_RXD/PWM_CTRL5/SPI1_WP/I2S_TXWS
10	GPIO16	TESTMODE/UART1_CTS/ IR_OUT/PWM_CTRL2

Pin	Name	Description
11	XTAL_O	XTAL P
12	XTAL_I	XTAL N
13	VDD_0P8	Digital power supply
14	VDD_1P0	SIMO output for analog, the typical value is 1.0 V. Add 0.1 uF capacitor to VDD_1P0 pin as close as possible.
15	LX2	SIMO inductance. Add 1 uH power inductance as close as possible. In LDO mode, LX2 is the regulator power supply input, LX1 is floating.
16	LX1	
17	POWERKEY	Chip power key
18	VDD_BUCK	VDD BUCK 3.3V
19	VDDIO	IO POWER 3.3V
20	VDD_EFUSE	eFuse program power, the power is 1.8V.
21	GPIO6	UART0_TXD/32K_CLK_OUT/XTAL_O_32k/I2S_RXSCK/COLD_RESET
22	GPIO5	UART0_RXD/40M_CLK_OUT/XTAL_I_32k /I2S_RXWS/IR_OUT
23	GPIO8	SD_DATA2/MSPI_HOLD
24	GPIO7	SD_DATA3/MSPI_MOSI
25	GPIO12	SD_CMD/MSPI_WP
26	GPIO9	SD_CLK/MSPI_CLK
27	GPIO11	SD_DATA0/MSPI_MISO
28	GPIO10	SD_DATA1/MSPI_CS0
29	GPIO4	TRST/ UART0_RTS/PWM_CTRL4/SPI1_CS1/MSPI_CS1
30	GPIO3	TDI/ UART0_CTS/PWM_CTRL3/SPI1_MISO/I2C_SDA
31	GPIO2	TDO/ UART1_TXD/PWM_CTRL2/SPI1_MOSI/I2C_SCL
32	GPIO1	TMS/ UART1_RXD/PWM_CTRL1/SPI1_CS0/I2S_RXD
33	GPIO0	TCK/ UART2_TXD/PWM_CTRL0/SPI1_CLK/I2S_TXSCK
34	GPIO18	RESET_B/UART1_RTS/SPI1_HOLD/I2C_SCL/I2S_TXD/aux_3/vout_in

Pin	Name	Description
35	GPIO20	PWM_CTRL3/AUX_2/VOUT_IP/I2S_MCLK
36	GPIO15	BOOTMODE1/AUX_1/VOUT_QN/PWM_CTRL5/I2S_TXWS
37	GPIO14	BOOTMODE0/AUX_0/VOUT_QP/ PWM_CTRL4/I2S_TXD
38	VDD_DA	Analog power for DA, the typical power is 3.3V
39	VDD_PA	Analog power for PA, the typical power is 3.3V
40	LNA	

Table 5.2 ECR6600-TS2D QFN32 Pin Description

Pin	Name	Description
1	VDD_BAT	VDD_BAT1 and VDD BAT2, for RF BG, LP BG/LDO ETC
2	VDD_1p0RF	BUCK feedback
3	GPIO23	SD_H_DATA1/UART1_RTS/PWM_CTRL1/I2S_TXSCK
4	GPIO22	SD_H_DATA0/UART0_TXD/PWM_CTRL0/I2S_TXWS
5	GPIO13	SD_H_CLK/UART2_TXD/ I2C_SCL/I2S_RXD/dpll_80M_o
6	GPIO21	SD_H_CMD/UART0_RXD/I2C_SDA/I2S_TXD
7	GPIO25	SD_H_DATA3/phy_entrx/ PWM_CTRL3 /!phy_entrx /I2C_SDA
8	GPIO24	SD_H_DATA2/ UART1_CTS/ PWM_CTRL2/ I2S_MCLK
9	GPIO17	WAKEUP/UART2_RXD/PWM_CTRL5/SPI1_WP/I2S_TXWS
10	GPIO16	UART1_CTS/ IR_OUT/PWM_CTRL2
11	XTAL_O	XTAL P
12	XTAL_I	XTAL N
13	VDD_0P8	Digital power supply
14	VDD_1P0	SIMO output for analog, the typical power is 1.0 V, add 0.1 uF capacitor to VDD_1P0 pin as close as possible.
15	LX2	SIMO inductance, add 1 uH power inductance as close as

Pin	Name	Description
16	LX1	possible. In LDO mode, LX2 is the regulator power supply input, LX1 is floating.
17	POWERKEY /VDDIO/VDD_ BUCK/	IO power is 3.3 V/VDD_BUCK/Chip power key
18	VDD_EFUSE	eFuse Program power is 1.8 V
19	GPIO6	UART0_TXD/32K_CLK_OUT/XTAL_O_32k/I2S_RXSCK/COLD_R ESET
20	GPIO5	UART0_RXD/40M_CLK_OUT/XTAL_I_32k /I2S_RXWS/IR_OUT
21	GPIO4	TRST/ UART0_RTS/PWM_CTRL4/SPI1_CS1/MSPI_CS1
22	GPIO3	TDI/ UART0_CTS/PWM_CTRL3/SPI1_MISO/I2C_SDA
23	GPIO2	TDO/ UART1_TXD/PWM_CTRL2/SPI1_MOSI/I2C_SCL
24	GPIO1	TMS/ UART1_RXD/PWM_CTRL1/SPI1_CS0/I2S_RXD
25	GPIO0	TCK/ UART2_TXD/PWM_CTRL0/SPI1_CLK/I2S_TXSCK
26	RESET_B/TEST MODE	TESTMODE/RESET_B/UART1_RTS/SPI1_HOLD/I2C_SCL/I2S_TX D/aux_3/vout_in
27	GPIO20	PWM_CTRL3/AUX_2/VOUT_IP/I2S_MCLK
28	GPIO15	BOOTMODE1/AUX_1/VOUT_QN/PWM_CTRL5/I2S_TXWS
29	GPIO14	BOOTMODE0/AUX_0/VOUT_QP/ PWM_CTRL4/I2S_TXD
30	VDD_DA	Analog power for DA, the typical power is 3.3 V
31	VDD_PA	Analog power for PA, the typical power is 3.3 V
32	LNA	

Table 5.3 ECR6600-TS2L QFN32 Pin Description

Pin	Name	Description
1	VDD_BAT	VDD_BAT1 and VDD BAT2, for RF BG, LP BG/LDO ETC
2	VDD_1p0RF	BUCK feedback

Pin	Name	Description
3	GPIO23	SD_H_DATA1/UART1_RTS/PWM_CTRL1/I2S_TXSCK
4	GPIO22	SD_H_DATA0/UART0_TXD/PWM_CTRL0/I2S_TXWS
5	GPIO13	SD_H_CLK/UART2_TXD/ I2C_SCL/I2S_RXD/dpll_80M_o
6	GPIO21	SD_H_CMD/UART0_RXD/I2C_SDA/I2S_TXD
7	GPIO25	SD_H_DATA3/phy_entrx/ PWM_CTRL3 /!phy_entrx /I2C_SDA
8	GPIO24	SD_H_DATA2/ UART1_CTS/ PWM_CTRL2/ I2S_MCLK
9	GPIO17	WAKEUP/UART2_RXD/PWM_CTRL5/SPI1_WP/I2S_TXWS
10	GPIO16	UART1_CTS/ IR_OUT/PWM_CTRL2
11	XTAL_O	XTAL P
12	XTAL_I	XTAL N
13	VDD_0P8	Digital power supply
14	VDD_1P0	SIMO output for analog, the typical power is 1.0 V, add 0.1 uF capacitor to VDD_1P0 pin as close as possible.
15	LX2	LDO mode regulator power supply
16	VDD_BUCK/POWERKEY	VDD_BUCK/Chip power key
17	VDDIO	IO power is 3.3 V
18	VDD_EFUSE	eFuse Program power is 1.8 V
19	GPIO6	UART0_TXD/32K_CLK_OUT/XTAL_O_32k/I2S_RXSCK/COLD_RESET
20	GPIO5	UART0_RXD/40M_CLK_OUT/XTAL_I_32k /I2S_RXWS/IR_OUT
21	GPIO4	TRST/ UART0_RTS/PWM_CTRL4/SPI1_CS1/MSPI_CS1
22	GPIO3	TDI/ UART0_CTS/PWM_CTRL3/SPI1_MISO/I2C_SDA
23	GPIO2	TDO/ UART1_TXD/PWM_CTRL2/SPI1_MOSI/I2C_SCL
24	GPIO1	TMS/ UART1_RXD/PWM_CTRL1/SPI1_CS0/I2S_RXD
25	GPIO0	TCK/ UART2_TXD/PWM_CTRL0/SPI1_CLK/I2S_TXSCK

Pin	Name	Description
26	RESET_B/TEST MODE	TESTMODE/RESET_B/UART1_RTS/SPI1_HOLD/I2C_SCL/I2S_TXD/aux_3/vout_in
27	GPIO20	PWM_CTRL3/AUX_2/VOUT_IP/I2S_MCLK
28	GPIO15	BOOTMODE1/AUX_1/VOUT_QN/PWM_CTRL5/I2S_TXWS
29	GPIO14	BOOTMODE0/AUX_0/VOUT_QP/ PWM_CTRL4/I2S_TXD
30	VDD_DA	Analog power for DA, the typical power is 3.3 V
31	VDD_PA	Analog power for PA, the typical power is 3.3 V
32	LNA	

6 Order Information

Table 6.1 Order Information

Part Number	Package	Description	Ambient Operating Temperature
ECR6600-40D	QFN40 5x5	Single band 1x1 11AX, non-sip, DC-DC	-40~+105℃
ECR6600-40L	QFN40 5x5	Single band 1x1 11AX, non-sip, LDO	-40~+105℃
ECR6600-TS2D	QFN32 4x4	Single band 1x1 11AX, sip 2M, DC-DC	-40~+105℃
ECR6600-TS2L	QFN32 4x4	Single band 1x1 11AX, sip 2M, LDO	-40~+105℃