ESWIN

ECR6600 WIFI6
SINGLE-CHIP 802.11b/g/n/ax 1T1R
WLAN + BLE SoC

Hardware Reference Design User Guide

Rev 5.0.1
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Revision history

Revision	Release Date	Summary
1.0	2021/4/10	Initial draft
2.0	2021/4/17	1:Modify Bootmode Testmode and ResetB description 2:Modify Pin Number description
3.0	2021-4-27	1：GPIO13 FUN4 change IRout to UART_TXD 2: GPIO16 FUN3 change bledebug0 to PWM_CTRL2
4.0	2021-8-11	Add Power on sequence and Power off sequence
5.0	2021-8-21	1:Delete 32Pin LDO mode and DCDC mode , use T mode 2:update Boot mode sequence

ECR6600 Reference Design

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ECR6600 Reference Design

1. Overview

ESWIN ECR6600 series are highly integrated single-chip controllers enabling low power 802.11ax Wireless LAN(WLAN) network and BLE combo. It meets the continuous demand for ever efficient power usage, compact design and reliable performance in the industry. It works in the 2.4GHz ISM frequency band.

With its complete and self-contained Wi-Fi networking capabilities, ECR6600 can perform either as a standalone application, or a slave to a host MCU. When ECR6600 hosts an application, it promptly boots up from the external flash. Its integrated high-speed cache optimizes the system's performance and memory.

ECR6600 can be applied to any micro-controller design as a Wi-Fi adaptor through SDIO interfaces.

Besides the Wi-Fi 6 features, ECR6600 also integrates an enhanced version of Andes D10 32-bit processor and on-chip SRAM. It can be interfaced with external sensors and other devices through the GPIOs, resulting in low development cost at early stage and minimum footprint. Software Development Kit (SDK) provides sample codes for various applications.

ECR6600 integrates antenna switches, RF balun, power amplifier, low-noise receive amplifier, filters and power management modules. The compact design minimizes the PCB size and the external circuitry.

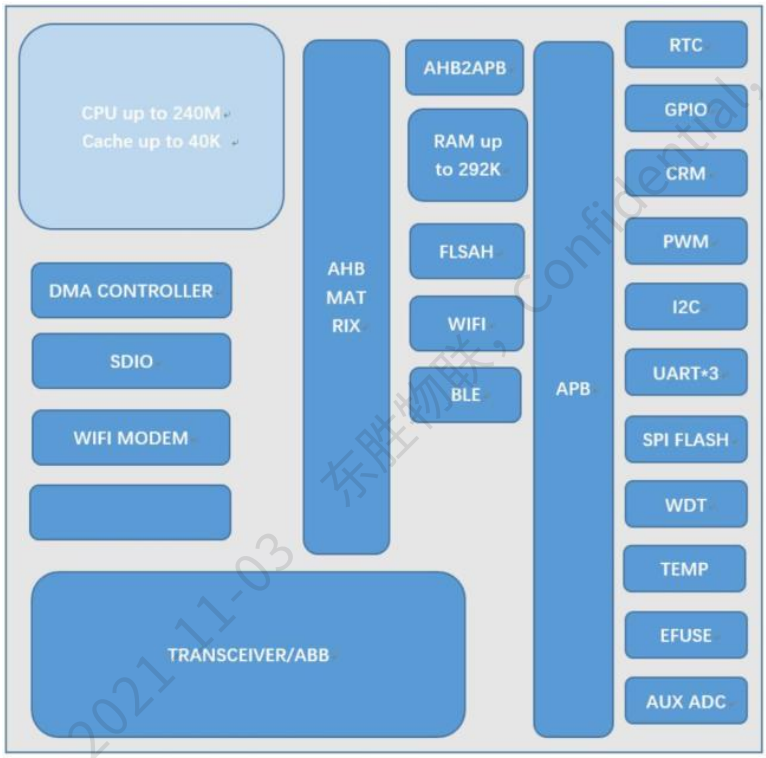


Figure 1.1 SOC Block Diagram

2. Specificition

Categories	Items	Parameters
WIFI	Standard	FCC/CE/TELEC/SRRC
	Protocols	802.11 b/g/n/ax
	Frequency range	2.4G~2.5G (2400~2483.5)MHz
	Tx Power	802.11b (11Mbps) : 17dBm
		802.11g (54Mbps) : 14dBm
		802.11n (MCS7 20MHz) : 13dBm
		802.11n (MCS7 40MHz) : 13dBm
		802.11ax (MCS7): 13dBm
	Rx Sensitivity	802.11b (11Mbps) : -90dBm
		802.11g (54Mbps) : -76dBm
		802.11n (MCS7 20MHz) : -72dBm
		802.11n (MCS7 40MHz) : -69dBm
		802.11ax (MCS7) : -70dBm
	Antenna	On-board, external, IPEX connector, ceramic chip
BLE	Tx Power	1Mbps:10dBm
		2Mbps:10dBm
		LE mode(S=8):10dBm
	Rx Sensitivity	1Mbps: -93dBm
		2Mbps:-91dBm
Hardware	Peripheral	● SDIO:50MHz SDIO2.0 Host and SDIO 2.0 Slave ● UART:3 ● SPI:2 ● I2C:2 ● I2S:1 ● GPIO:25(maximum) ● PWM:6 ● AuxADC:4 ● Crystal:26MHz and 40MHz
	Operating voltage	2.7V~3.6V
	Operating current	30mA(Rx mode)
	Operating temperature range	-40°C~105°C
	Storage temperature range	-40°C~105°C
	Package size	32pin(4mm*4mm) 40pin(5mm*5mm)

3. Pin Definition and Pin Multiplexing

3.1 Pin Layout for ECR6600

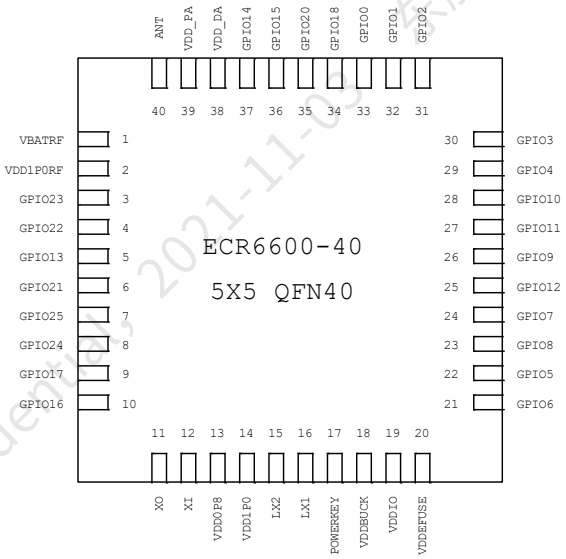


Figure 3.1.1 40pin Pin Layout

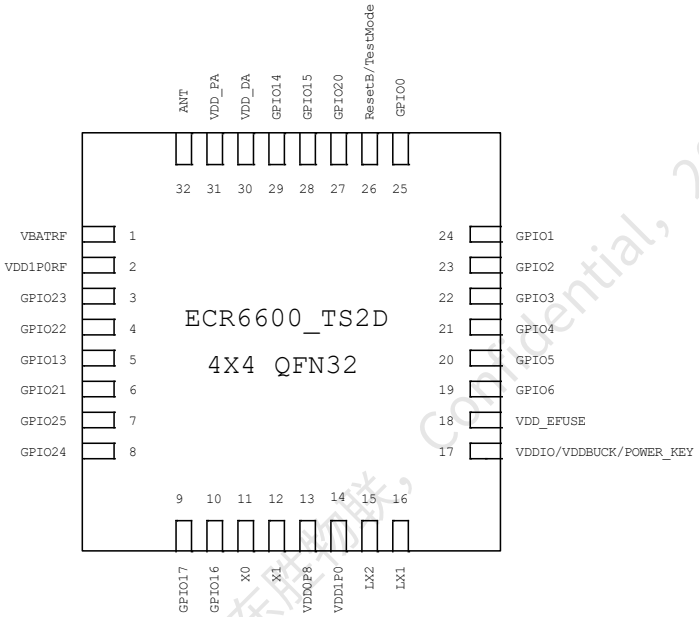


Figure 3.1.3 ECR6600T DCDC Layout

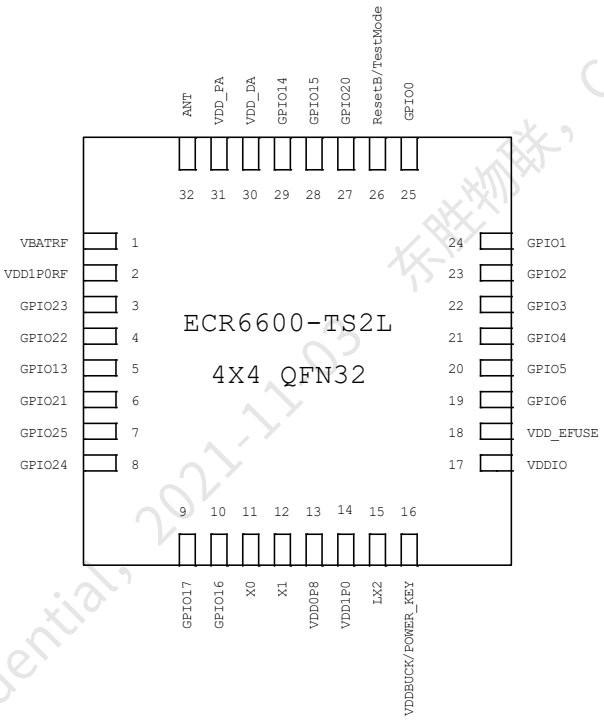


Figure 3.1.4 ECR6600T LDO Layout

3.2 Pin Definition

Table 3.2.1 ECR6600 40PIN function

PIN	Name	Type	Function
1	VDD_BAT	PI	VDD_BAT1 AND VDD BAT2,FOR RF BG, LP BG/LDO ETC
2	VDD_1p0RF	PI	VCC1V0 For Analog supply
3	GPIO23	IO	SD_H_DATA1/UART1_RTS/PWM_CTRL1/I2S_TXSCK
4	GPIO22	IO	SD_H_DATA0/UART0_TXD/PWM_CTRL0/I2S_TXWS
5	GPIO13	IO	SD_H_CLK/UART2_TXD/ I2C_SCL/I2S_RXD
6	GPIO21	IO	SD_H_CMD/UART0_RXD/I2C_SDA/I2S_TXD
7	GPIO25	IO	SD_H_DATA3/PWM_CTRL3/I2C_SDA
8	GPIO24	IO	SD_H_DATA2/UART1_CTS/PWM_CTRL2/I2S_MCLK
9	GPIO17	IO	WAKEUP/UART2_RXD/PWM_CTRL5/SPI1_WP/I2S_TXWS
10	GPIO16	IO	NC/UART1_CTS/ IR_OUT/PWM_CTRL2
11	XTAL_O	AO	XTAL P
12	XTAL_I	AI	XTAL N
13	VDD_0P8	PO	DIGITAL POWER SUPPLY
14	VDD_1P0	PO	SIMO output for Analog, typical is 1.0V, please add 0.1uF capacitor to VDD_1P0 pin as close as possible.
15	LX2	AI	

16	LX1	AI	SIMO inductance, please add 1uH power inductance as close as possible, when the LDO mode, LX2 is the regulator power supply input, LX1 Floating
17	POWERKEY	AI	Chip Power key
18	VDD_BUCK	PI	VDD BUCK 3.3V
19	VDDIO	PI	IO POWER 3.3V
20	VDD_EFUSE	PI	EFUSE PROGRAM POWER 1.8V
21	GPIO6	IO	UART0_TXD/32K_CLK_OUT/XTAL_O_32k/I2S_RXSCK/COLD_RESET
22	GPIO5	IO	UART0_RXD/40M_CLK_OUT/XTAL_I_32k /I2S_RXWS/IR_OUT
23	GPIO8	IO	SD_DATA2/MSPI_HOLD
24	GPIO7	IO	SD_DATA3/MSPI_MOSI
25	GPIO12	IO	SD_CMD/MSPI_WP
26	GPIO9	IO	SD_CLK/MSPI_CLK
27	GPIO11	IO	SD_DATA0/MSPI_MISO
28	GPIO10	IO	SD_DATA1/MSPI_CS0
29	GPIO4	IO	TRST/ UART0_RTS/PWM_CTRL4/SPI1_CS1/MSPI_CS1
30	GPIO3	IO	TDI/ UART0_CTS/PWM_CTRL3/SPI1_MISO/I2C_SDA
31	GPIO2	IO	TDO/ UART1_TXD/PWM_CTRL2/SPI1_MOSI/I2C_SCL
32	GPIO1	IO	TMS/ UART1_RXD/PWM_CTRL1/SPI1_CS0/I2S_RXD
33	GPIO0	IO	TCK/ UART2_TXD/PWM_CTRL0/SPI1_CLK/I2S_TXSCK
34	GPIO18	IO	TestMode/RESET_B
35	GPIO20	IO	PWM_CTRL3/AUX_2/VOUT_IP/I2S_MCLK
36	GPIO15	IO	BOOTMODE1/AUX_1/VOUT_QN/PWM_CTRL5/I2S_TXWS
37	GPIO14	IO	BOOTMODE0/AUX_0/VOUT_QP/ PWM_CTRL4/I2S_TXD
38	VDD_DA	PI	ANALOG POWER FOR DA, TYPICAL 3.3V
39	VDD_PA	PI	ANALOG POWER FOR PA, TYPICAL 3.3V
40	LNA	PI	TRSwitch RF output/input

Table 3.2.3 ECR6600T_DCDC 32PIN function

PIN	Name	Type	Function
1	VDD_BAT	PI	VDD_BAT1 AND VDD BAT2,FOR RF BG, LP BG/LDO ETC
2	VDD_1p0RF	PI	VCC1V0 For Analog supply
3	GPIO23	IO	UART1_RTS/PWM_CTRL1/I2S_TXSCK
4	GPIO22	IO	UART0_TXD/PWM_CTRL0/I2S_TXWS
5	GPIO13	IO	UART2_TXD/ I2C_SCL/I2S_RXD
6	GPIO21	IO	UART0_RXD/I2C_SDA/I2S_TXD
7	GPIO25		SD_H_DATA3/PWM_CTRL3/I2C_SDA

8	GPIO24		SD_H_DATA2/UART1_CTS/PWM_CTRL2/I2S_MCLK
9	GPIO17	IO	WAKEUP/UART2_RXD/PWM_CTRL5/SPI1_WP/I2S_TXWS
10	GPIO16	IO	UART1_CTS/ IR_OUT/PWM_CTRL2
11	XTAL_O	AO	XTAL P
12	XTAL_I	AI	XTAL N
13	VDD_0P8	PO	DIGITAL POWER SUPPLY SIMO output for Analog, typical is 1.0V, please add 0.1uF capacitor to VDD_1P0 pin as close as possible.
14	VDD_1P0	PO	
15	LX2	AI	SIMO inductance, please add 1uH power inductance as close as possible, when the LDO mode, LX2 is the regulator power supply input, LX1 Floating
16	LX1	AI	SIMO inductance, please add 1uH power inductance as close as possible, when the LDO mode, LX2 is the regulator power supply input, LX1 Floating
17	VDDIO	PI	IO POWER 3.3V/VDD_BUCK/PWR_KEYON
18	VDD_EFUSE	PI	EFUSE PROGRAM POWER 1.8V
19	GPIO6	IO	UART0_TXD/32K_CLK_OUT/XTAL_O_32k/I2S_RXSCK/COLD_RESET
20	GPIO5	IO	UART0_RXD/40M_CLK_OUT/XTAL_I_32k /I2S_RXWS/IR_OUT
21	GPIO4	IO	TRST/ UART0_RTS/PWM_CTRL4/SPI1_CS1/MSPI_CS1
22	GPIO3	IO	TDI/ UART0_CTS/PWM_CTRL3/SPI1_MISO/I2C_SDA
23	GPIO2	IO	TDO/ UART1_TXD/PWM_CTRL2/SPI1_MOSI/I2C_SCL
24	GPIO1	IO	TMS/ UART1_RXD/PWM_CTRL1/SPI1_CS0/I2S_RXD
25	GPIO0	IO	TCK/ UART2_TXD/PWM_CTRL0/SPI1_CLK/I2S_TXSCK
26	ResetB/ TestMode	IO	TESTMODE/RESET_B
27	GPIO20	IO	PWM_CTRL3/AUX_2/VOUT_IP/I2S_MCLK
28	GPIO15	IO	BOOTMODE1/AUX_1/VOUT_QN/PWM_CTRL5/I2S_TXWS
29	GPIO14	IO	BOOTMODE0/AUX_0/VOUT_QP/ PWM_CTRL4/I2S_TXD
30	VDD_DA	PI	ANALOG POWER FOR DA, TYPICAL 3.3V
31	VDD_PA	PI	ANALOG POWER FOR PA, TYPICAL 3.3V
32	LNA	PI	TRSwitch of RF output

Table 3.2.4 ECR6600T_LDO 32PIN function

PIN	Name	Type	Function
1	VDD_BAT	PI	VDD_BAT1 AND VDD BAT2,FOR RF BG, LP BG/LDO ETC
2	VDD_1p0RF	PI	VCC1V0 For Analog supply
3	GPIO23	IO	UART1_RTS/PWM_CTRL1/I2S_TXSCK
4	GPIO22	IO	UART0_TXD/PWM_CTRL0/I2S_TXWS

5	GPIO13	IO	UART2_TXD/ I2C_SCL/I2S_RXD
6	GPIO21	IO	UART0_RXD/I2C_SDA/I2S_TXD
7	GPIO25		SD_H_DATA3/PWM_CTRL3/I2C_SDA
8	GPIO24		SD_H_DATA2/UART1_CTS/PWM_CTRL2/I2S_MCLK
9	GPIO17	IO	WAKEUP/UART2_RXD/PWM_CTRL5/SPI1_WP/I2S_TXWS
10	GPIO16	IO	UART1_CTS/ IR_OUT/PWM_CTRL2
11	XTAL_O	AO	XTAL P
12	XTAL_I	AI	XTAL N
13	VDD_0P8	PO	DIGITAL POWER SUPPLY SIMO output for Analog, typical is 1.0V, please add 0.1uF capacitor to VDD_1P0 pin as close as possible.
14	VDD_1P0	PO	
15	LX2	AI	SIMO inductance, please add 1uH power inductance as close as possible, when the LDO mode, LX2 is the regulator power supply input, LX1 Floating
16	VDD_BUCK _PWR_KEY	AI	VDD_BUCK/PWR_KEYON
17	VDDIO	PI	IO POWER 3.3V
18	VDD_EFUSE	PI	EFUSE PROGRAM POWER 1.8V
19	GPIO6	IO	UART0_TXD/32K_CLK_OUT/XTAL_O_32k/I2S_RXSCK/COLD_RESET
20	GPIO5	IO	UART0_RXD/40M_CLK_OUT/XTAL_I_32k /I2S_RXWS/IR_OUT
21	GPIO4	IO	TRST/ UART0_RTS/PWM_CTRL4/SPI1_CS1/MSPI_CS1
22	GPIO3	IO	TDI/ UART0_CTS/PWM_CTRL3/SPI1_MISO/I2C_SDA
23	GPIO2	IO	TDO/ UART1_TXD/PWM_CTRL2/SPI1_MOSI/I2C_SCL
24	GPIO1	IO	TMS/ UART1_RXD/PWM_CTRL1/SPI1_CS0/I2S_RXD
25	GPIO0	IO	TCK/ UART2_TXD/PWM_CTRL0/SPI1_CLK/I2S_TXSCK
26	ResetB/ TestMode	IO	TESTMODE/RESET_B
27	GPIO20	IO	PWM_CTRL3/AUX_2/VOUT_IP/I2S_MCLK
28	GPIO15	IO	BOOTMODE1/AUX_1/VOUT_QN/PWM_CTRL5/I2S_TXWS
29	GPIO14	IO	BOOTMODE0/AUX_0/VOUT_QP/ PWM_CTRL4/I2S_TXD
30	VDD_DA	PI	ANALOG POWER FOR DA, TYPICAL 3.3V
31	VDD_PA	PI	ANALOG POWER FOR PA, TYPICAL 3.3V
32	LNA	PI	TRSwitch of RF output

3.3 Pin MultiPlexing

Table 3.3.1 GPIO20

Truth table	Function name	Function

000	PWM_CTRL3	Pulse Width Modulation 3
001	GPIO20	General purpose use 20
010	Auxadc2	ADC2 input for external signal, please make sure the external signal at ADC input is under 3.3V, If the ADC input signal is above 3.3V, please make sure the ADC DIV set to 4. The resistance of AuxADC input should be far less than 1Mohm, which is AuxADC DIV resistance.
011	I2S_MCLK	Integrated inter-chip Sound MCLK

Table 3.3.2 GPIO14

Truth table	Function name	Function
000	Bootmode0	Boot select mode 0
001	GPIO14	General purpose use 14
010	Auxadc0	External ADC 0 input
011	PWM_CTRL0	Pulse Width Modulation 0
100	I2S_TXD	Integrated inter chip Sound TXD

Table 3.3.3 GPIO15

Truth table	Function name	Function
000	Bootmode1	Boot select mode 1
001	GPIO15	General purpose use 15
010	Auxadc1	ADC1 input for external signal
011	PWM_CTRL1	Pulse Width Modulation 1
100	I2S_TXWS	Integrated inter-chip Sound TXWS

Table 3.3.4 GPIO16

Truth table	Function name	Function
000	NC	For ECR6600T This Function is NC
001	GPIO16	General purpose use 16
010	UART1_CTS	UART1 CTS
011	IR_OUT	Infrared Radiation OUT
100	PWM_CTRL2	Pulse Width Modulation 2

Table 3.3.5 GPIO17

Truth table	Function name	Function
000	WAKEUP	Wakeup from sleep status. This can be configured as active high or active low
001	GPIO17	General purpose use 17
010	UART2_RXD	UART2 RXD

011	SPI1_WP	SPI1 write protection active low
100	PWM_CTRL1	Pulse Width Modulation 1
101	I2S_TXWS	Integrated inter-chip Sound TXWS
110	BLE_DEBUG[2]	BLE_DEBUG 2

Table 3.3.6 ResetB

Truth table	Function name	Function
000	TestMode	For ECR6600 Fun000 is ResetB , For ECR6600T Fun000 is TestMode, Fun001 is ResetB
001	Reset_B	Reset is active low , in Normal case please pull up 4.7Kohm ResetB to High TestMode low is DFT mode
010	UART1_RTS	UART1 RTS
011	SPI1_HOLD	SPI1 suspension of communication active low
100	I2C_SCL	Inter- Integrated Circuit SCL
101	I2S_TXD	Integrated inter-chip Sound TXD
110	AuxADC[3]	ADC 3 input for external signal
110	BLE_DEBUG[1]	BLE_DEBUG 1

Table 3.3.7 GPIO0

Truth table	Function name	Function
000	JTAG_TCK	JTAG TCK
001	GPIO0	General purpose use 0
010	UART2_TXD	UART2 TXD
011	SPI1_CLK	SPI1 CLK
100	PWM_CTRL0	Pulse Width Modulation 0
101	I2S_TXSCK	Integrated inter-chip Sound TXSCK
110	BLE_DEBUG[3]	BLE_DEBUG 3

Table 3.3.8 GPIO1

Truth table	Function name	Function
000	JTAG_TMS	JTAG TMS
001	GPIO1	General purpose use 1
010	UART1_RXD	UART1 RXD
011	SPI1_CS0	SPI1 CS0
100	PWM_CTRL1	Pulse Width Modulation 1
101	I2S_RXD	Integrated inter-chip Sound RXD
110	BLE_DEBUG[4]	BLE_DEBUG 4

Table 3.3.9 GPIO2

Truth table	Function name	Function
000	JTAG_TDO	JTAG TDO
001	GPIO2	General purpose use 2
010	UART1_TXD	UART1 TXD
011	SPI1_MOSI	SPI1 MOSI
100	PWM_CTRL2	Pulse Width Modulation 2
101	I2C_SCL	Inter- Integrated Circuit SCL
110	BLE_DEBUG[5]	BLE_DEBUG 5

Table 3.3.10 GPIO3

Truth table	Function name	Function
000	JTAG_TDI	JTAG TDI
001	GPIO3	General purpose use 3
010	UART0_CTS	UART0 CTS
011	SPI1_MISO	SPI1 MISO
100	PWM_CTRL3	Pulse Width Modulation 3
101	I2C_SDA	Inter- Integrated Circuit SDA
110	BLE_DEBUG[6]	BLE_DEBUG 6

Table 3.3.11 GPIO4

Truth table	Function name	Function
000	JTAG_TRST	JTAG TRST
001	GPIO4	General purpose use 4
010	UART0_RTS	UART0 RTS
011	SPI1_CS2	SPI1 CS2
100	PWM_CTRL0	Pulse Width Modulation 0
101	PSRAM_CS	MPSI_CS1 use for PSRAM_CS
110	BLE_DEBUG[7]	BLE_DEBUG 7

Table 3.3.12 GPIO5

Truth table	Function name	Function
000	UART0_RXD	UART0 RXD
001	GPIO5	General purpose use 5
010	40M_CLK_OUT	40MHz XTAL_P
011	IR_OUT	Infrared Radiation OUT
100	I2S_RXWS	Integrated inter-chip Sound RXWS
101	XTAL_I_32K	32KHz XTAL_N

Table 3.3.13 GPIO6

Truth table	Function name	Function
000	UART0_TXD	UART0 TXD
001	GPIO6	General purpose use 6
010	COLD_RESET	
011	32K_OUT(32K_CLK_OUT)	
100	I2S_RX_SCK	Integrated inter-chip Sound RX_SCK
101	XTAL_O_32K	32KHz XTAL_P

Table 3.3.14 GPIO7

Truth table	Function name	Function
000	SD_DATA0	SDIO slave DATA 0
001	GPIO7	General purpose use 7
010	MSPI_MOSI	MSPI MOSI

Table 3.3.15 GPIO8

Truth table	Function name	Function
000	SD_DATA3	SDIO slave DATA 3
001	GPIO8	General purpose use 8
010	MSPI_HOLD	MSPI HOLD

Table 3.3.16 GPIO9

Truth table	Function name	Function
000	SD_CLK	SDIO slave CLK
001	GPIO9	General purpose use 9
010	MSPI_CLK	MSPI CLK

Table 3.3.17 GPIO10

Truth table	Function name	Function
000	SD_CMD	SDIO slave data CMD
001	GPIO10	General purpose use 10
010	MSPI_CS0	MSPI CS0

Table 3.3.18 GPIO11

Truth table	Function name	Function
000	SD_DATA1	SDIO slave DATA 1
001	GPIO11	General purpose use 11
010	MSPI_MISO	MSPI MISO

Table 3.3.19 GPIO12

Truth table	Function name	Function
000	SD_DATA2	SDIO slave DATA2
001	GPIO12	General purpose use 12
010	MSPI_WP	MSPI Write protection

Table 3.3.20 GPIO13

Truth table	Function name	Function
000	SD_H_CLK	SDIO host CLK
001	GPIO13	General purpose use 13
010	UART2_TXD	UART2 RXD
011	I2C_SCL	Inter- Integrated Circuit SCL
100	I2S_RXD	Integrated inter-chip Sound RXD
101	DPLL_80M_O	DPLL_80M_Opuput

Table 3.3.21 GPIO21

Truth table	Function name	Function
000	SD_H_CMD	SDIO host CMD
001	GPIO21	General purpose use 21
010	UART0_RXD	UART0 RXD
011	I2C_SDA	Inter- Integrated Circuit SDA
100	I2S_TXD	Integrated inter-chip Sound TXD

Table 3.3.22 GPIO22

Truth table	Function name	Function
000	SD_H_DATA0	SDIO host data 0
001	GPIO22	General purpose use 22
010	UART0_TXD	UART0 TXD
011	PWM_CTRL0	Pulse Width Modulation 0
100	I2S_TXWS	Integrated inter-chip Sound TXWS

Table 3.3.23 GPIO23

Truth table	Function name	Function
000	SD_H_DATA1	SDIO host data 1
001	GPIO23	General purpose use 23
010	UART1_RTS	UART1 RTS
011	PWM_CTRL1	Pulse Width Modulation 1
100	I2S_TXSCK	Integrated inter-chip Sound TX_SCK

Table 3.3.24 GPIO24

Truth table	Function name	Function
000	SD_H_DATA2	SDIO host data 2
001	GPIO24	General purpose use 24
010	UART1_CTS	UART1 CTS
011	PWM_CTRL2	Pulse Width Modulation 2
100	I2S_MCLK	Integrated inter-chip Sound MCLK

Table 3.3.25 GPIO25

Truth table	Function name	Function
000	SD_H_DATA3	SDIO host data 3
001	GPIO25	General purpose use 25
011	PWM_CTRL3	Pulse Width Modulation 3
101	I2C_SDA	Inter- Integrated Circuit SDA

4. Schematic Checklist

The highly integrated design of ECR6600 reduces the number of the off-chip components required.

To pair with the ECR6600, fewer than several resistors and capacitors, 1 crystal oscillator are needed to make a complete module with wireless communication capability. The following is a detailed description of the schematic and layout designs of ECR6600, which ensures the optimum functionality.

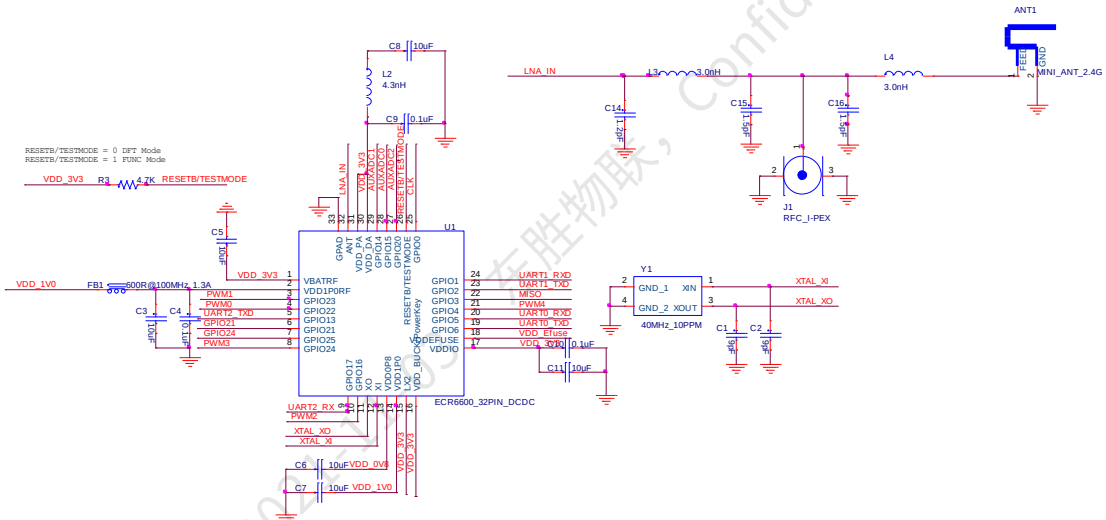


Figure 4.1 Schematic for 32pin LDO mode

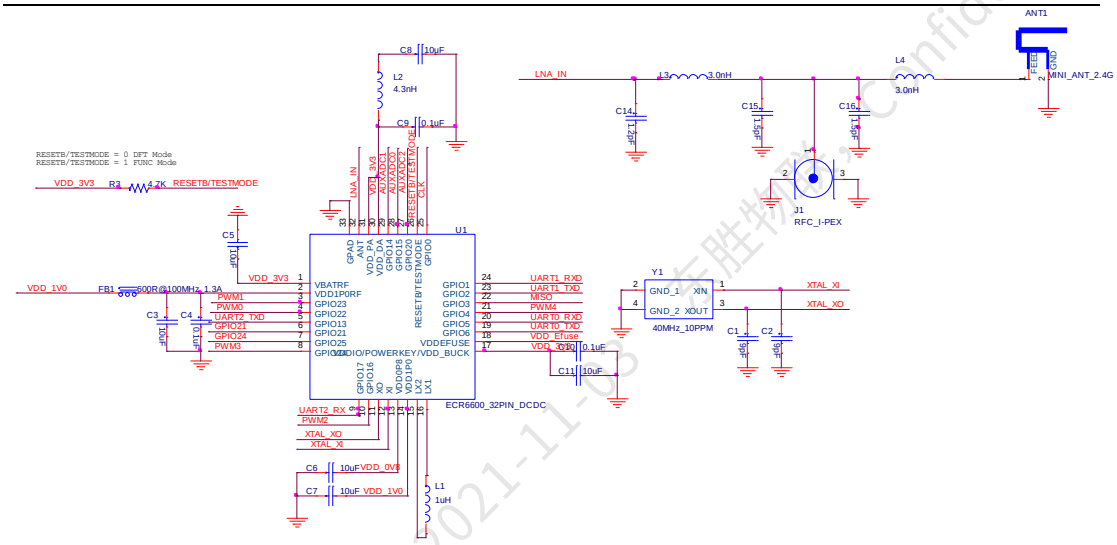


Figure 4.2 Schematic for 32pin DCDC mode

4.1 Power Supply

4.1.1 Analog Power Supply

ECR6600 has three analog pins for its power supplies: Pin1, Pin30, Pin31 for the power supplies for the internal Bandgap, PA, and DA respectively; the required voltage range for the analog power supply pins is 2.7V~ 3.3V.

Note that the PA and DA is the mainly Power consumption, During the trx switch the Power consumption of PA and DA is very High, it will lead the voltage on PA and DA unstable, it recommend add an additional 10μF capacitor with a 0603 or 0805 footprint is required along with the 0.1μF capacitor with a 0402 footprint to be placed next to the power supply pins.

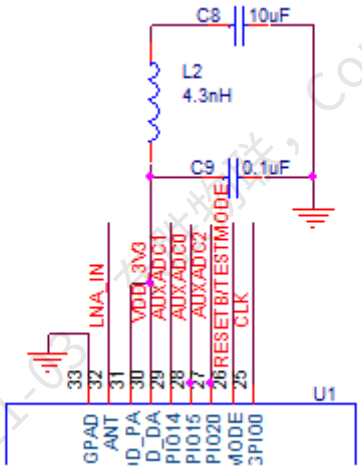


Figure4.3 Power supply for Analog

4.1.2 DCDC Mode for Digital and Analog Core Supply

The ECR6600 implements SIMO (Single-Inductor-Multiple-Outputs), which generates 1.0V supply for its analog circuitry and 0.8V supply for its digital circuitry. With the DCDC mode, the power conversion efficiency varies with the inductance value. It is recommended the optimal inductance value of 1uH be used, and the DC resistance of the inductor should be less than 100m ohm. The topology of SIMO is shown in the figure below.

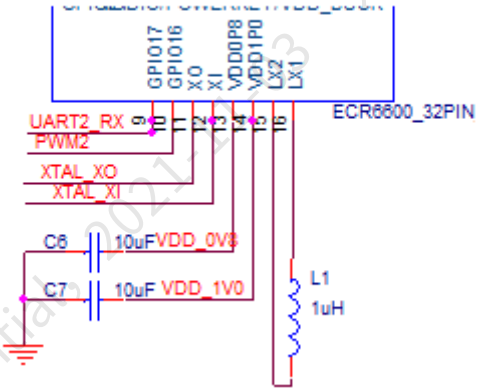


Figure4.4 Power supply for DCDC

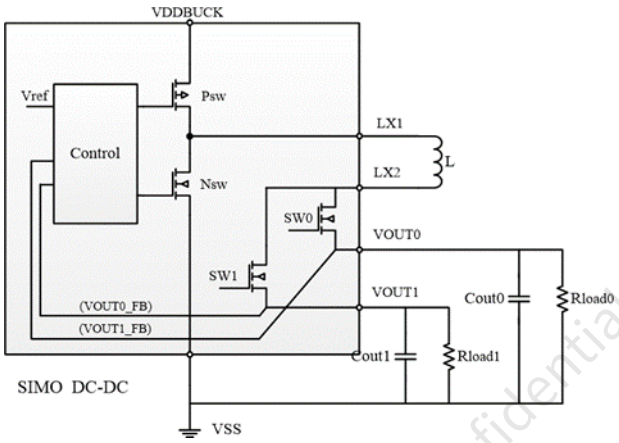


Figure4.5 SIMO topology for DCDC

4.1.3 LDO Mode for the Digital and Analog Core Supplies

The ECR6600 also supports LDO mode, which can generate 1.0V for analog and 0.8V for Digital. In LDO mode, the external inductor could be eliminated. The LX1 pin should be NC. The LX2 pin should connect with an external 3.3V supply, with a 10uF external capacitor placed at the LX2 pin, as close as possible.

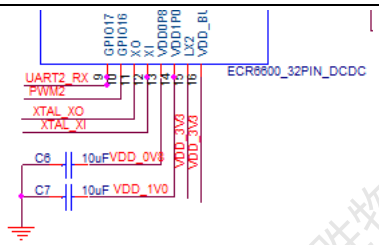


Figure4.6 Power supply for LDO

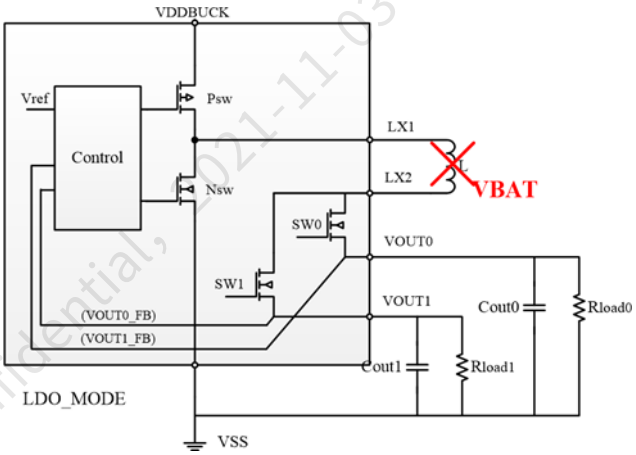


Figure4.7 topology for LDO mode

4.1.4 IO Power Supply

The ECR6600 VDDIO pin is used for SOC IO Pad and Flash, with the typical voltage of 3.3V. After SOC is brought up, the VDDIO_SW is enabled, and the IO voltage supplies the SOC. This will decrease the Current when the SOC is power off. The Flash_SW can be programed by FW, and supply to the SIP Flash.

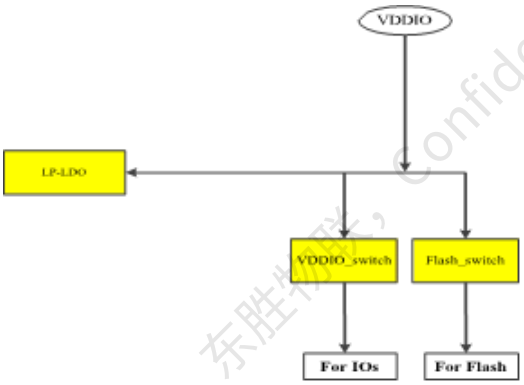


Figure4.8 topology for VDDIO

The ECR6600 VDD_Efuse pin is used for SOC Efuse programming. The typical voltage at this pin for effuse programming is 1.8V. For the rest of the time, the VDD_Efuse pin should remain NC.

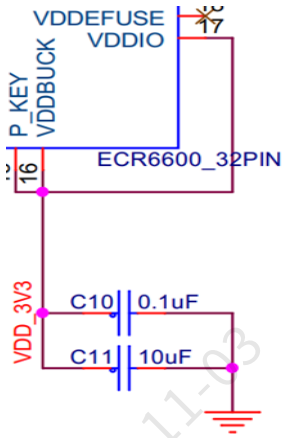


Figure4.9 Power supply for VDDIO

4.2 Power-on Sequence and Power-off Sequence

ECR6600 chip is powered by a 3.3V external supply. The chip should be activated after the turn on sequence.

The turn on sequence is

1) keyon pad high turns on BGP， BGP_OK outputs high when BGP is stable.
2) VBAT compare outputs a signal POR when VBAT>2.5V.
3) turn on 32k_osc and dig_lp_ldo.
4) After 8 cycles, release cold reset if the voltage of battery is ok.
5) Release isolation of PMU when Dig_lp_ldo stable , enable 32kH RC oscillator.
6) PMU controller control PMU, turn on buck and other LDO, turn on CPU system.
7) The cpu set ps_hold register equal one to keep BGP_EN equal one.

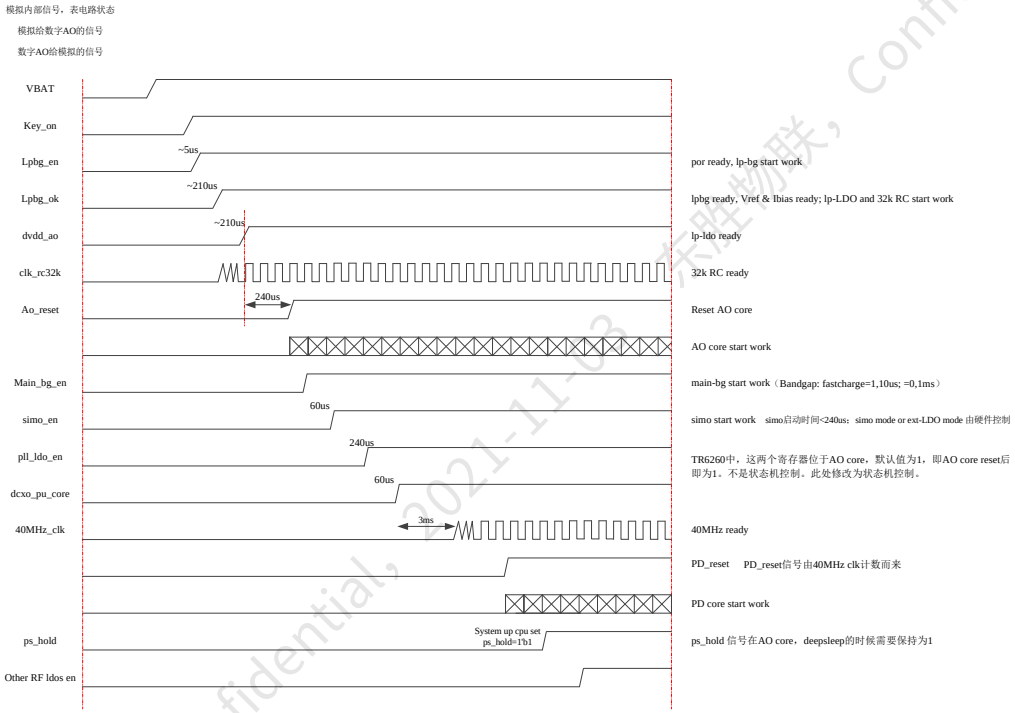


Figure 4-2-1 Power on Sequence

The turn off sequence is

1) CPU cut the supply of RF/ABB.

2) CPU save context into flash if IOT mode; if slave mode, the date will processed by host.

3) CPU set shutdown mode to the register of PCU.

4) PCU initiate shutdown process, turn off clock, isolation, reset;then send pwr_ctrl==2'b00 to pmu_ctrl FSM.

5) Pmu_ctrl FSM clear ps_hold, shutdown bgp dig_lp_ldo, turn off process finished.

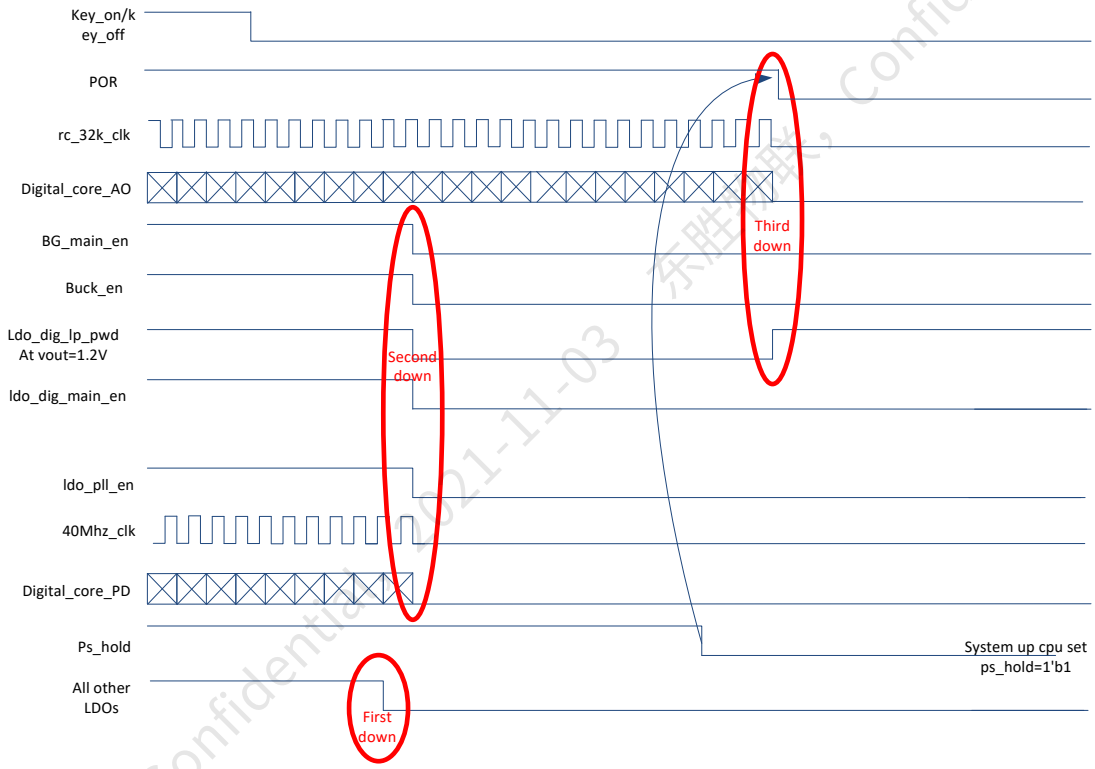


Figure 4-2-2 Power off Sequence

4.3 Flash

The SIP flash used on ECR6600 is an 2MB SPI Flash. It supports XIP mode with SPI0(MSPI) which is occupied by CPU Read and Write. In this scenario the MSPI is not a General SPI mode. For general SPI mode, please re-assign to other SPI port.

4.4 Crystal Oscillator

ECR6600 can support both 26MHz and 40MHz crystal oscillators. The accuracy of the crystal oscillators output frequency should be within ± 10 ppm. And the operating temperature range should be between -20°C and 105°C.

In circuit design, capacitor C1 and C2, which are connected to the ground, are added to the input and output terminals of the crystal oscillator respectively. The values of the two capacitors can be flexible, ranging from 6 pF to 22 pF. However, the specific capacitance values of C1 and C2 depend on the further testing of and adjustment to the overall performance of the whole circuit. Normally, the capacitance values of C1 and C2 should be made sure that the typical frequency offset of the system is the minimal offset.

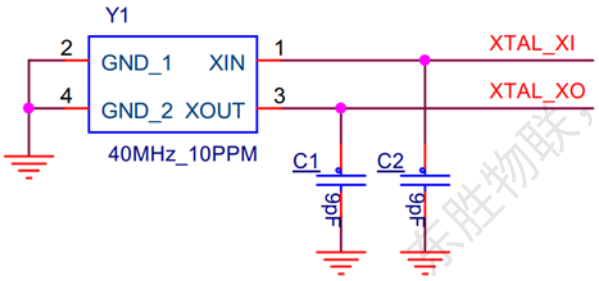


Figure4.10 ECR6600 Crystal Oscillator

4.5 BootMode, TestMode and ResetB

4.5.1 BootMode

The BOOT process is described below.

- After power-on and reset, Andes CPU executes the Bootrom program from the zero address;
- The Bootrom program initializes the C execution environment, and select the BOOT mode by reading the value of the register corresponding to the BOOT pin;
- The system startup process can be roughly divided into two mode.
  - Startup mode: start up from Flash, and complete normal version startup; The system will detect whether the spi-flash is empty and firmware version is valid. If valid, the CPU will load and run the Uboot to boot firmware version; if not, it will enter the process of firmware burning.
  - Download mode: download the firmware version from the external hardware interface, and burn it into SPI-FLASH to complete version upgrade.

    Download the Uboot into IRAM by UART, and the CPU jumps to IRAM to run Uboot;

    Uboot downloads firmware version by UART, and burn it into SPI-FLASH.

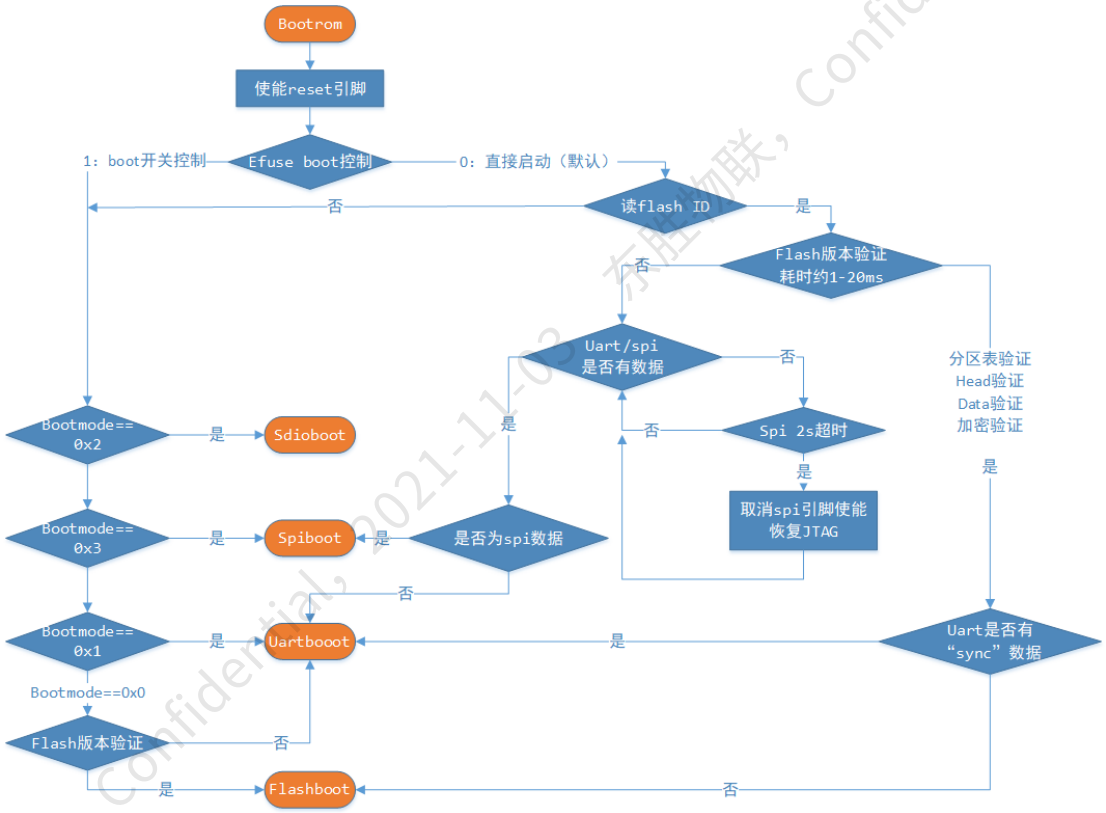


Figure 4.11 startup general flow diagram

4.5.1 Efuse Boot Control

If efuse Boot Control bit in effuse table is 0, Then Bootrom will initial flash download uboot and image file from UART to flash, if UART has no data over than 2 second, then the pinmux for SPI Flash will change to Jtag mode.

4.5.2 ATE Bootmode truth table

The Boot mode truth table is as follow

Table 4.1 BOOTMODE truth table

Truth table[BootMode1:0]	Bootmode manner
00	SPI Flash Boot
01	UART Boot
10	SDIO Boot
11	SPI Boot

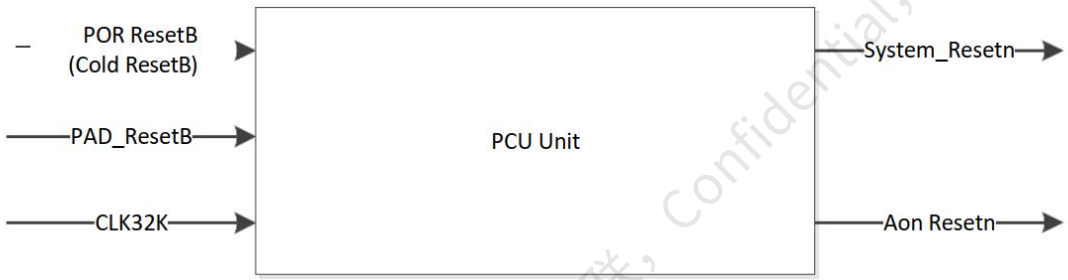
Table 4.2 BOOTMODE pin configuration

BOOTMODE	first boot	second boot	description
0 (Flash boot)	Detect in-chip version. If it's valid, run the code in the flash.(User mode)	If empty or invalid, jump to UART boot mode and run.	1.When provided to users, the version detection is OK,start up directly from FLASH. It improves system startup speed and user experience. 2 .If the result of the version detection is invalid version or

			non-version, boot will jump to uart boot mode. This is convenient for production and software debugging.
1 (UART boot)	Download Uboot from UART and run it.(research and development mode).	If it is timeout to download, run the Flash code directly.	Force UART open to communicate with host to complete version burning and upgrade. It can also be called factory/fixture/maintenance mode.
2 (SDIO boot)	Download the firmware from SDIO to memory and run it directly.		There is no second boot, and startup needs to get the firmware version through SDIO. It can also be called throughout mode
3 (SPI boot)	Download the firmware from SPI to memory and run it directly.		There is no second boot, and startup needs to get the firmware version through SPI. It can also be called throughout mode

4.5.3 ResetB

The System Reset is as Follow, after Power on, the POR will generate Cold ResetB, and reset the system. The PAD_ResetB can also reset the system, It can reset the PD core, and the cold Reset can reset the AO core and PD core. The System reset is Synchronized Asynchronous Reset, It will generate Bus Reset first and then Generate CPU reset.



4.5.4 TestMode

TestMode is used for DFT test, when the Testmode is High, Then the chip will work as test mode. In normal operation mode, the Testmode should tie to low or floating.

4.6 RF

The impedance looking into the ECR6600 PA RF port is near 50Ω, so the impedance of the transmission line should be 50ohm for both Tx and Rx. It is recommended a PI network be placed near the RF port, which can eliminate the 2nd harmonic of the Tx output signal tone.

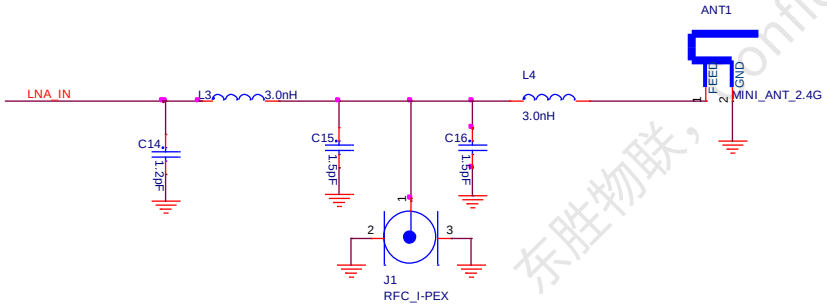


Figure4.12 ECR6600 RF Transmission Line

5. PCB Layout Design

5.1 Layout Design

The PCB has four layers:

- The first layer is the TOP layer for the signal lines and the surface components.
- The second layer is the GND layer, where no signal lines are laid to ensure a complete GND plane.
- The third layer is the POWER layer where only power lines can be placed. It is acceptable to place some signal lines under unavoidable circumstances.
- The fourth layer is the BOTTOM layer. Only signal lines can be laid. Placing components on this layer is not recommended.

5.2 Power Supply Design

The 3.3V power lines are highlighted in yellow in Figure 5.1 The width of the power lines should be greater than 15 mils. Before the power lines reach the analog power-supply pins (including Pin1, 3, 4, 28, 29) of ECR6600, a 10μF 0402 or 0603 capacitor (C6 in Figure 4.3) should be added. The capacitor should be placed close to the analog power-supply pins of the ECR6600.Power lines should be placed on the third layer. When the power lines reach the pins of the chipset, vias are needed so that the power lines can go through the layers and connect to the pins of the chipset on the TOP layer. The diameter of the via holes should exceed the width of the power lines and the diameter of the drill should be a little larger than the radius of the vias.

The Vias on the Chipset Ground should as much as possible, it is recommended at least 16, the more the better.

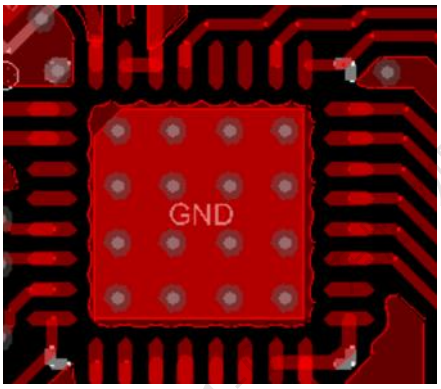


Figure 5.1 Vias on GND PAD

5.3 The crystal oscillator Design

The crystal oscillator should be placed as close to the XTAL pins as possible (without the traces between the crystal oscillator and the XTAL pin being too long). It is a good practice to use via stitching around the clock trace to reduce the ground-plane impedance.

There should be no vias on the input and output traces, which means that the traces cannot cross layers. In addition, the input and output traces should not be routed over one another, not even on different layers.

Do not route high-frequency digital signal lines under the crystal oscillator. It is best not to route any signal line under the crystal oscillator. The larger the copper area on the top layer is the better. As the crystal oscillator is a sensitive component, do not place any magnetic components nearby that may cause interference, for example, power-switching converter components or unshielded inductors.

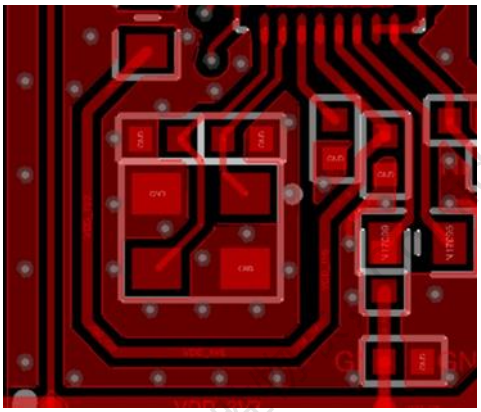


Figure 5.2 Layout for DCXO

5.4 The RF Design

The characteristic RF impedance is 50Ω. The ground plane should has a good reflow path, The RF trace should be as short as possible with dense ground via stitching around it for isolation. The width of RF lines should be no less than 6 mils, while a width of over 10 mil is better. π-type matching circuitry

should be reserved on the RF trace and placed close to the RF pin.

There should be no vias for the RF trace. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.

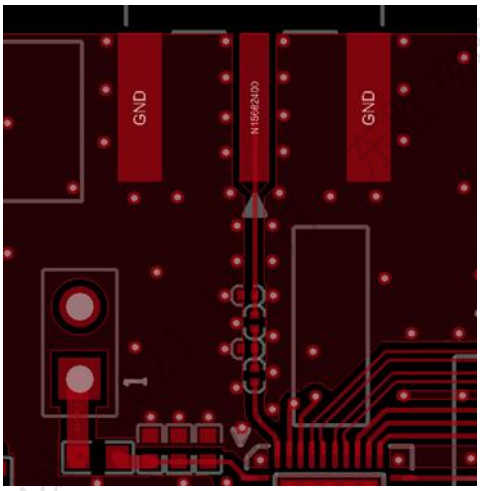


Figure 5.3 Layout for RF port