TR6260-S1

DATASHEET

802.11b/g/n Wi-Fi Single Chip

Release Notes

Data	Version	Release Notes
2018.10	V1.0	release
2018.12	V2.0	Update 3.6 chapter
2019.5	V2.1	Update pinlist and package information

Contents

1. Overview

The SoC is a 2.4GHz IEEE 802.11b/g/n Wi-Fi single chip solution with standard security features. With optimized power and RF performance, robustness, versatility, reliability, various power profiles, full features and functions, the chip is designed for a wide variety of applications, including Smart home, Wearable devices and IoT (Internet of Things).

It integrates a 32-bit microcontroller, 802.11b/g/n Wi-Fi baseband, a 2.4GHz RF transceiver with antenna switch, RF balun, PA (power amplifier), LNA (low noise receive amplifier) and filters, ample memory space, a general-purpose ADC(Analog-to-Digital Converter), 6-channel PWM(Pulse Width Modulation), flexible I/O interfaces, and multi-stage power management module. With the highly-integrated SoC, few external components and minimal PCB(Printed Circuit Board) area are needed to build Wi-Fi applications.

The SoC has many features of the state-of-the-art low power chips, such as good resolution clock gating, advanced management of multi-stage power modes, and dynamic power scaling.

The chip uses CMOS for single-chip fully-integrated radio and Baseband, and also integrates advanced calibration circuitries that allow the solution to dynamically adjust itself to remove external circuit imperfections or adjust to changes in external conditions.

1.1 Wi-Fi

- 802.11 b/g/n/i
- 802.11 n (2.4 GHz), up to 150 Mbps
- 802.11 e: QoS for wireless multimedia technology
- WMM-PS, UAPSD

- A-MPDU and A-MSDU aggregation
- Block ACK
- Wi-Fi Protected Access (WPA)/WPA2/WPA2-Enterprise/Wi-Fi Protected Setup (WPS)
- SoftAP mode
- BT-Coexistence interface

1.2 MCU and Advanced Features

1.2.1 CPU and Memory

- 32-bit, up to 160MHz
- Instruction cache controller with 8KB cache RAM memory
- support XIP(executed in place)
- Flash, 1 Mbytes

1.2.2 Clocks and Timers

- PLL to generate a high frequency clock (typically 160 MHz)
- Internal 32kHz RC oscillator
- External 40 MHz crystal oscillator

1.2.3 Advanced Peripheral Interfaces

- Up to 16 GPIOs depending on package option
- 1 x I2C Master/Slave
- 1 x I2S Master/Slave
- 2 x SPIs Master/Slave
- 3 x UART interfaces with hardware flow control

- SDIO 2.0(up to 4bit) @ 50MHz
- Up to 6-channel HW PWM output
- 4-channel ADC with 14-bit ENOB
- 1 PGA

1.2.4 Security

- IEEE 802.11 standard security features all supported, including CCMP, WPA/WPA2
- eFuse encryption
- Cryptographic hardware acceleration:
  – AES
  – Random Number Generator (RNG)

1.3 Application

- Generic low power IoT sensor hub
- Generic low power IoT loggers
- Video streaming from camera
- Over The Top (OTT) devices
- Wi-Fi enabled speech recognition devices
- Smart power plugs
- Home automation
- Mesh network
- Industrial wireless control
- Baby monitors
- Wearable electronic devices

• Wi-Fi location-aware devices

• Security ID tags

• Healthcare

– Proximity and movement monitoring trigger devices

– Temperature sensing loggers

2. Block Diagram

2.1 Function block diagram

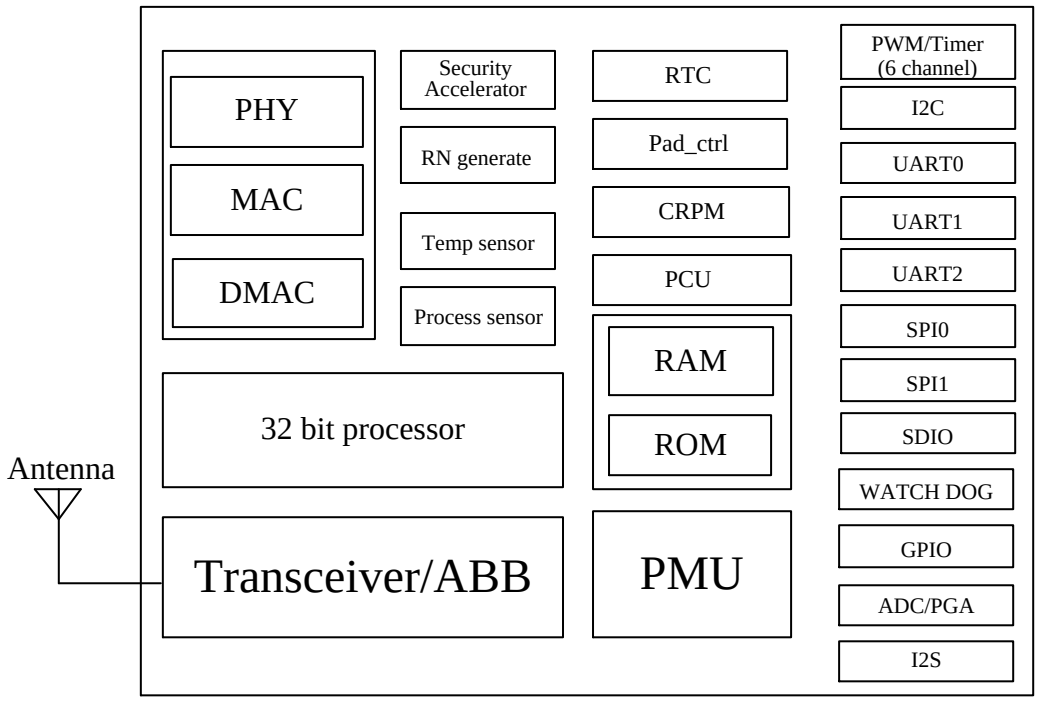


Figure 2-1 TR6260 functional block diagram

2.2 CPU and Memory

2.2.1 CPU

Basic Features:

• 16/32 general purpose 32-bit registers

• 5-stage pipeline with extensive clock-gating

- Dynamic branch prediction
- 16/32/64/128-entry BTB
- Return address stack
- 2/4 entries
- Vector interrupts for internal/external interrupt controller
- 2/6/10/16/24/32 hardware vector interrupt signals
- Fixed/Programmable interrupt level
- Edge/Level interrupt trigger type
- 2/3 HW-level nested interruption
- Address space up to 4GB
- Radix-4 divider support
- HW stack protection support
- Processor Status bus support
- PowerBrake support

2.2.2 Internal Memory

TR6260's internal memory includes:

- RAM
- ROM
- bits of eFuse

2.2.3 External Flash and SRAM

TR6260 supports 1MB or 2MB external QSPI Flash

2.3 Timers and Watchdogs

2.3.1 Watchdog Timers

The watchdog timer provides a two-stage mechanism to prevent a system from lock-up. The first stage is called “interrupt stage”. If the watchdog interrupt is enabled and the watchdog timer is not restarted during the interrupt stage, the interrupt signal, wdt_int , will be asserted. The second stage, reset stage, begins right after the interrupt stage. If the watchdog reset is enabled and the watchdog timer is not restarted during the reset stage, the reset signal, wdt_rst , will be asserted.

2.4 System Clocks

2.4.1 CPU Clock

Upon reset, an external crystal clock source 40MHz is selected as the default CPU clock. The external crystal clock source also connects to a PLL to generate a high frequency clock (typically 160 MHz).Depending on the application the CPU clock frequency can auto switch in 160MHz,80 MHz,40MHz and 32KHz.

2.4.2 RTC Clock

The RTC clock from internal RC oscillator (typically about 32.75 KHz).The internal RC clock can be calibration by the 40MHz from the external crystal.

2.5 Radio

The TR6260 radio consists of the following main blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

2.5.1 2.4 GHz Receiver

The 2.4 GHz receiver down-converts the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with 2 high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits and baseband filters are integrated within TR6260.

2.5.2 2.4 GHz Transmitter

The 2.4 GHz transmitter up-converts the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high powered Complementary Metal Oxide Semiconductor (CMOS) power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling state-of-the-art performance of

delivering +18.5 dBm of average power for 802.11b transmission and +14 dBm for 802.11n transmission. Additional calibrations are integrated to cancel any imperfections of the radio, such as:

- Carrier leakage
- I/Q phase matching
- Baseband nonlinearities
- RF nonlinearities
- Antenna matching

These built-in calibration routines reduce the amount of time and required for product test and make test equipment unnecessary.

2.5.3 Clock Generator

The clock generator generates quadrature 2.4 GHz clock signals for the receiver and transmitter. All components of the clock generator are integrated on the chip, including all inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms to ensure the best performance of the receiver and transmitter.

2.6 Wi-Fi

Wi-Fi Baseband block

- Full IEEE 802.11b/g/n legacy compatibility with enhanced performance.
- Support 20/40MHz channel with optional SGI (64QAM Modulation).
- 802.11b modulations:DSSS with DBPSK/DQPSK, 1Mbps/2Mbps, and CCK, 5.5, 11Mbps.
- 802.11g modulations: OFDM with BPSK/QPSK/16QAM/64QAM, 6, 9, 12, 18, 24, 36, 48, 54 Mbps, 20MHz channel.
- 802.11n modulations : OFDM with BPSK/QPSK/16QAM/64QAM, MCS0 ~ 400ns GI, 6.5/7.2, 13/14.4, 19.5/21.7, 26/28.9, 39/43.3, 52/57.8, 58.5/65, 65/72.2Mbps, 20MHz channel.
- Bit rate: up to 150 Mbps with 40MHz and MCS7 in 11n.
- NonHT, HTMF operation.
- Greenfield detection.

MAC feature

- IEEE 802.11i. Inline ciphering module (supports HW engine for CCMP, WAPI, ..), supports optional stand-alone ciphering operation with BUS interface.
- IEEE 802.11 z/w/d/r/k.
- WMM, Wi-Fi direct.
- SoftAP.
- WMM-PS/TLDS/NAN.

• AMPDU/AMSDU aggregation including block ACK.

2.7 Low-Power Management

With the advanced power management technologies, TR6260 can switch between different power modes.

• Power mode

– SHUTDOWN mode

– DEEPSLEEP mode

– LIGHTSLEEP mode

– IDLE mode

3. Peripheral Interface

3.1 General Purpose Input / Output Interface (GPIO)

TR6260 has up to 24 GPIO pins which can be assigned to various functions by programming the appropriate registers. There are several kinds of GPIOs: digital only GPIOs, analog enabled GPIOs, capacitive touch enabled GPIOs, etc. Analog enabled GPIOs can be configured as digital GPIOs. Capacitive touch enabled GPIOs can be configured as digital GPIOs.

Each digital enabled GPIO can be configured to internal pull-up or pull-down, or set to high impedance. When configured as an input, the input value can be read through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts. In short, the digital IO pins are bi-directional, non-inverting and tri-state, including input and output buffer with tri-state control. These pins can be multiplexed with other functions, such as the SDIO interface, UART, SPI, etc. For low power operations, the GPIOs can be set to hold their states.

3.2 Analog-to-Digital Converter (ADC)

TR6260 integrates 12-bit SigmaDelta ADCs and supports measurements on 4 channels (analog enabled pins) to sample battery voltage, temperature sensor and external analog input.

3.3 SD/SDIO/MMC Host Controller

This SDIO can act as SDIO/SD/MMC device, with connecting to SDIO host. CPU can write or read SDIO register and The CPU or DMAC can write or read SDIO data .An SD/SDIO/MMC host/slave controller is available which supports the following features:

- Secure Digital memory (SD mem Version 3.0 and Version 3.01)
- Secure Digital I/O (SDIO Version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA Version 1.1)
- Multimedia Cards (MMC Version 4.41, eMMC Version 4.5 and Version 4.51)

The controller allows clock output at up to 80 MHz and in three different data-bus modes: 1-bit, 4-bit and 8-bit. It supports two SD/SDIO/MMC4.41 cards in 4-bit data-bus mode. It also supports one SD card operating at 1.8 V level.

3.4 Universal Asynchronous Receiver Transmitter (UART)

TR6260 has three UART interfaces, i.e. UART0 , UART1 and UART2, which provide asynchronous communication (RS232 and RS485) or IrDA support, and communicate at up to 5 Mbps. 2 UARTs provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). All

of the interfaces can be accessed by the DMA controller or directly by CPU.

3.5 I2C Interface

TR6260 has I2C bus interfaces which can serve as I2C master or slave depending on the user's configuration. The I2C interfaces support:

- Standard mode (100 kbit/s)
- Fast mode (400 kbit/s)
- Up to 5 MHz, but constrained by SDA pull up strength
- 7-bit/10-bit addressing mode
- Dual addressing mode

Users can program command registers to control I2C interfaces to have more flexibility.

3.6 I2S Interface

TR6260 supports both I2S host and I2S slave functions.The function of I2S interface can be realized by software programming. The I2S master BCLK supports 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz. The interface supports 16/32 bit per channel, the data format can be configured as 8/16/20/24/32bit per channel or decided by software.

3.7 Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) controller can be used for driving digital motors and smart lights. The controller consists of PWM timers, the PWM operator and a dedicated capture sub-module. Each timer provides timing in synchronous or independent form, and each PWM operator generates the

waveform for one PWM channel. The dedicated capture sub-module can accurately capture external timing events.

3.8 Serial Peripheral Interface (SPI)

SPI is a Serial Peripheral Interface (SPI) controller which serves as a SPI master or a SPI slave. As a SPI master, the controller connects various SPI devices. As a SPI slave, the controller responds to the master requests for data exchange.this system support 2 spi interface.

The SPI controller can act as a SPI master initiating SPI transfers on the SPI bus. The SPI transfer format and interface timing are programmable via the APB programing port.

The SPI controller can also act as SPI slaves and accepts common commands. In addition, the controller supports user-defined commands where the slave data field format is defined by the transfer control register.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Type	Max	Unit
Input low voltage	VIL	-0.3		0.3*VIO	V
Input high voltage	VIH	0.7*VDDIO	3.3	3.6	V
Output low voltage	VOL	-0.3		0.3*VIO	V
Output high voltage	VOH	0.7*VDDIO		3.6	V
Input pin capacitance	Cpad			2	pF

VDDIO	VIO	3.0	3.3	3.6	V
Maximum driver capability	IMAX			12	mA
Operation temperature range	TSTR	-40		105	℃

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Parameter	Symbol	Min	Type	Max	Unit
Battery regulator supply voltage	VBAT	3.0	3.3	3.6	V
IO supply voltage	VIO	1.8	3.3	3.6	V
Operating temperature range	TOPR	-40		105	℃
CMOS low level input voltage	VIL	0		0.3*VIO	V
CMOS high level input voltage	VIH	0.7*VIO		VIO	V
CMOS threshold voltage	VTH		0.5 VIO		V

4.3 Power Consumption Specifications

Table 4-3 Power Consumption Specifications

Parameter	Type	Unit
Tx 802.11b, Pout=0dBm	60.0	mA
Tx 802.11b, CCK 11Mbps, POUT=+18.5dBm	230.0	mA
Tx 802.11g, OFDM 54Mbps, POUT=+16dBm	165.0	mA
Tx 802.11n, MCS7, POUT=+14dBm	160.0	mA
Rx 802.11b, 1024 bytes packet length, -80dBm	60.0	mA
Rx 802.11g, 1024 bytes packet length, -70dBm	60.0	mA
Rx 802.11n, 1024 bytes packet length, -65dBm	60.0	mA
Light sleep	1.0	mA

Deep sleep	12.0	uA
DTIM4	1.0	mA
POWER OFF	0.4	uA

4.4 RX Specifications

Table 4-4 RX Specifications

Parameter	Symbol	Min	Type	Max	Unit	Test Conditions/Comments
RECEIVER RF						
Center Frequency		2412		2484	MHz	
Support Channel BandWidth		20		40	MHz	
Gain Min.			0		dB	
Gain Max			65		dB	
Gain Step			1		dB	
Noise Figure				5	dB	Max Gain
Third-Order Input Intermodulation Intercept Point				-5	dBm	
Second-Order Input Intermodulation Intercept Point				45	dBm	
LO Leakage			-90		dBm	
Quadrature Gain Error			0.5		dB	
Quadrature Phase Error			1		deg	

EVM			-28		dB	
Input S11			-10		dB	
RX Sensitivity						
1Mbps CCK			-97.0		dBm	
11Mbps CCK			-88.0		dBm	
6Mbps OFDM			-91.0		dBm	
54Mbps OFDM			-74.0		dBm	
HT20,MCS0			-90.7		dBm	
HT20,MCS7			-70.6		dBm	
HT40,MCS0			-86.6		dBm	
HT40,MCS7			-69.0		dBm	
Maximum Receive Level			0		dBm	
Rx Blocking Requirements			TBD			
Rx power on settle time						
Rx AGC time			<4		us	
Rx settle time when gain adjusted			<300		ns	
Rx RSSI accuracy			3		dB	

4.5 TX Specifications

Table 4-5 TX Specifications

Parameter	Sym bol	Min	Type	Max	Unit	Test Conditions/Com ments
TRANSMITTER						
Power Control Range			30		dB	
Power Control Resolution			1		dB	
Support Channel BandWidth		20		40	MHz	
Output S22		-8	-10		dB	
Max Output Power		16.0	17.5	20.0	dBm	1Mbps CCK
		13.0	13.5	14.0	dBm	6Mbps OFDM
		12.0	12.5	13.0	dBm	HT20,MCS0
EVM				-30	dB	HT20,MCS7
				-30	dB	HT20,MCS0
Tx 2^{nd} and 3^{rd} harmonic emission				-45	dBc/ Mhz	

4.6 LO Specifications

Table 4-6 LO Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Com ments
Frequency Range	FVCO	6400		6800	MHz	
Frequency Offset		-10		10	ppm	
Frequency Step				9.6	Hz	80MHz reference clock mode

Integrated Phase Noise			0.5		°	RMS, from 1kHz to 100MHz
PLL locking time				20	us	
Start time			50		ms	The time from Reset to send the first data packet

5. Pin definition

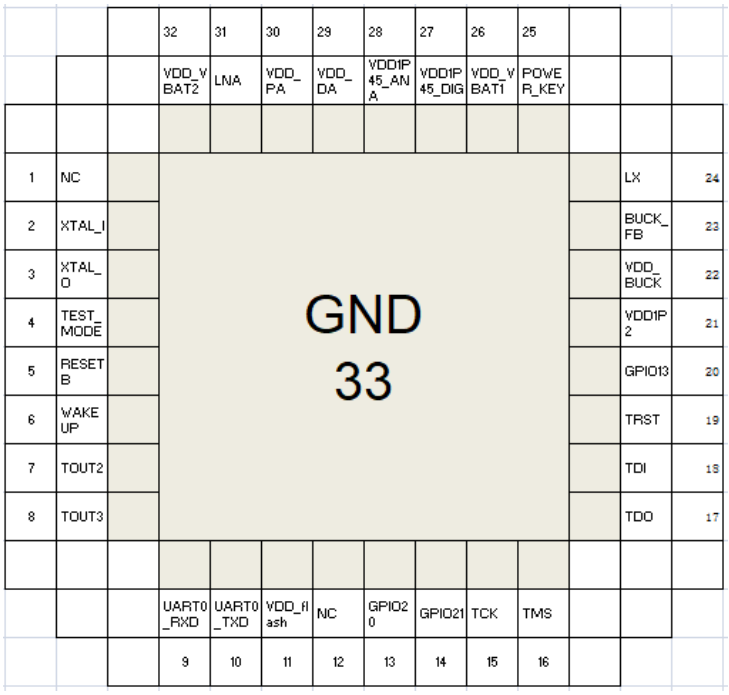


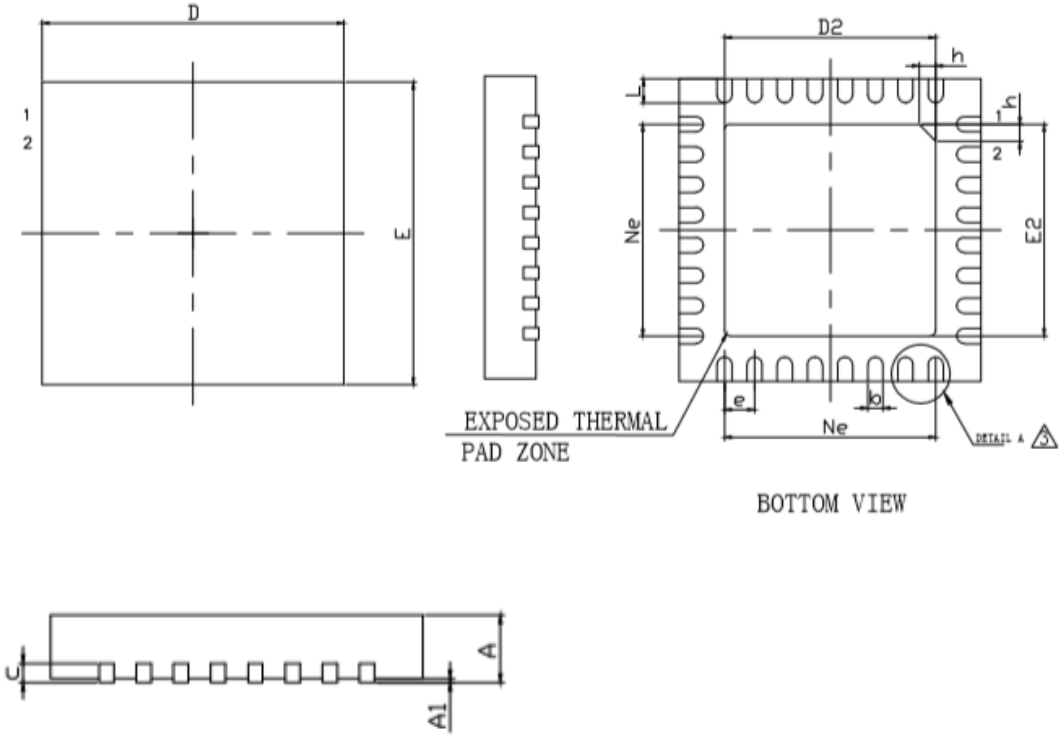
Figure 5-1 TR6260-S1-V1 Pin definition

Pin	Name	Type	Function
1	NC		
2	XTAL_I	AI	40M XTAL N
3	XTAL_O	AI	40M XTAL P
4	TEST_MODE	I/O	TESTMODE=1 will enter DFT

			TESTMODE=0 normal mode
5	RESETB	I	RESETB
6	WAKEUP	I/O	WAKEUP GPIO17
7	TOUT2	AI/DI/DO	ADC IN2, GPIO14
8	TOUT3	AI/DI/DO	ADC IN3, GPIO15
9	UART0_RXD	I/O	UART0 RXD,GPIO5
10	UART0_TXD	I/O	UART0_TXD,GPIO6
11	VDD_FLASH	I/O	Flash Power supply, 3.3V, please add 0.1uF on it
12	NC	I/O	NC
13	GPIO20	I/O	GPIO20
14	GPIO21	I/O	GPIO21
15	TCK	I/O	JTAG TCK, GPIO0
16	TMS	I/O	JTAG TMS, GPIO1
17	TDO	I/O	JTAG TDO, GPIO2
18	TDI	I/O	JTAG TDI,GPIO3
19	TRST	I/O	JTAG reset,GPIO4
20	GPIO13	I/O	GPIO13, 32K_CLK_OUT
21	VDD_1P2_1	PO	Digital Main LDO, Please add 1uF capacitor to this pin
22	VDD_BUCK	PI	BUCK POWER Supply, Please add 10uf+0.1uf capacitor to this pin
23	BUCK_FB	PI	BUCK POWER Feedback
24	LX	PI	1V45 Buck switch
25	POWERKEY	AI	Chip Power key, add to 3.3V

26	VDD_VBAT1	PI	Low power LDO power supply, typical is 3.3V, please add 0.1uf to this pin
27	VDD_1P45_DIG	PI	1.45V power supply , please connect to Buck FB(pin) if DCDC is used, please add 0.1uf capacitor to this pin. A bead between pin23 and VDD_1P45_DIG is recommended.
28	VDD_1P45_ANA	PI	1.45V power supply , please connect to Buck FB(pin) if DCDC is used, please add 4.7Uf+0.1uf capacitor to this pin. A bead between pin23 and VDD_1P45_ANA is recommended.
29	VDD_DA	PI	Analog Power for DA, typical 3.3V,please add 1Uf+10Nf capacitor to pin 37 , the place is as close as possible
30	VDD_PA	PI	Analog Power for PA, typical 3.3V,please add 10Uf+10Nf capacitor to pin 37 , the place is as close as possible
31	LNA	AI/AO	TRSwitch in
32	VDD_VBAT2	PI	BandGap LDO power supply, typical is 3.3V, please add 0.1uf to this pin

6. Package Information



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	2
	0.85	0.90	0.95	3
A1	—	0.02	0.05	
b	0.18	0.25	0.30	
c	0.18	0.20	0.25	
D	4.90	5.00	5.10	
D2	3.40	3.50	3.60	
e	0.50BSC			
Ne	3.50BSC			
E	4.90	5.00	5.10	
E2	3.40	3.50	3.60	
L	0.35	0.40	0.45	
h	0.30	0.35	0.40	
L/F载体尺寸	150x150		130x130	

Figure 6-1 TR6260-S1-V1 package Information