Design, reliability evaluation, and hardening of vision-oriented hardware accelerators

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Outline

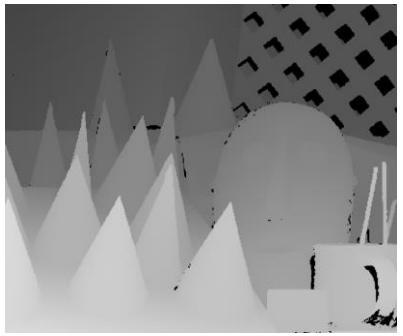
1. Introduction

- Stereo vision technique

Left Image

Right Image

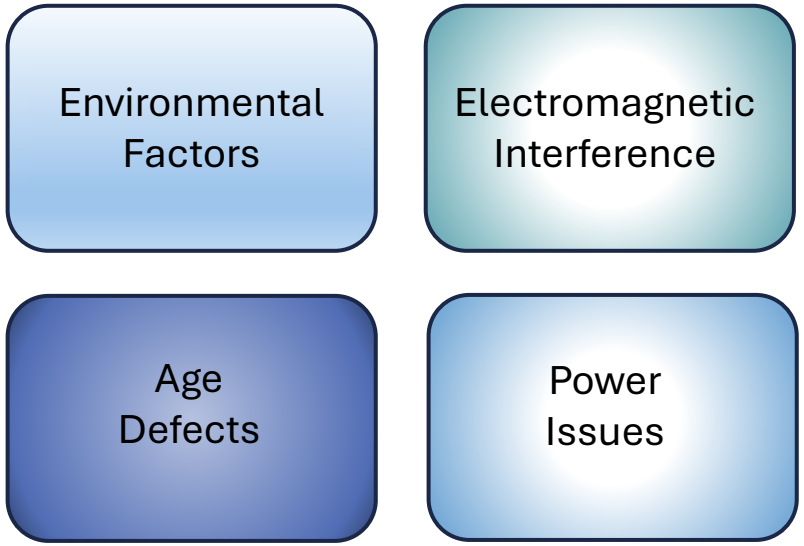
Ground-truth

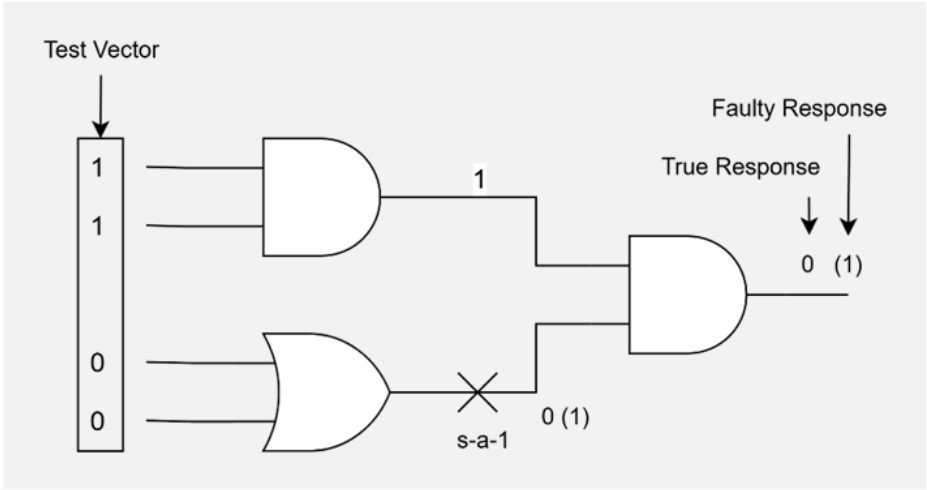


- The applications: ADAS, industrial automation, drones…

1. Introduction - Reliability

- Hardware can fail.
- The faults can compromise the reliability of safety-critical systems.





Goal of the thesis

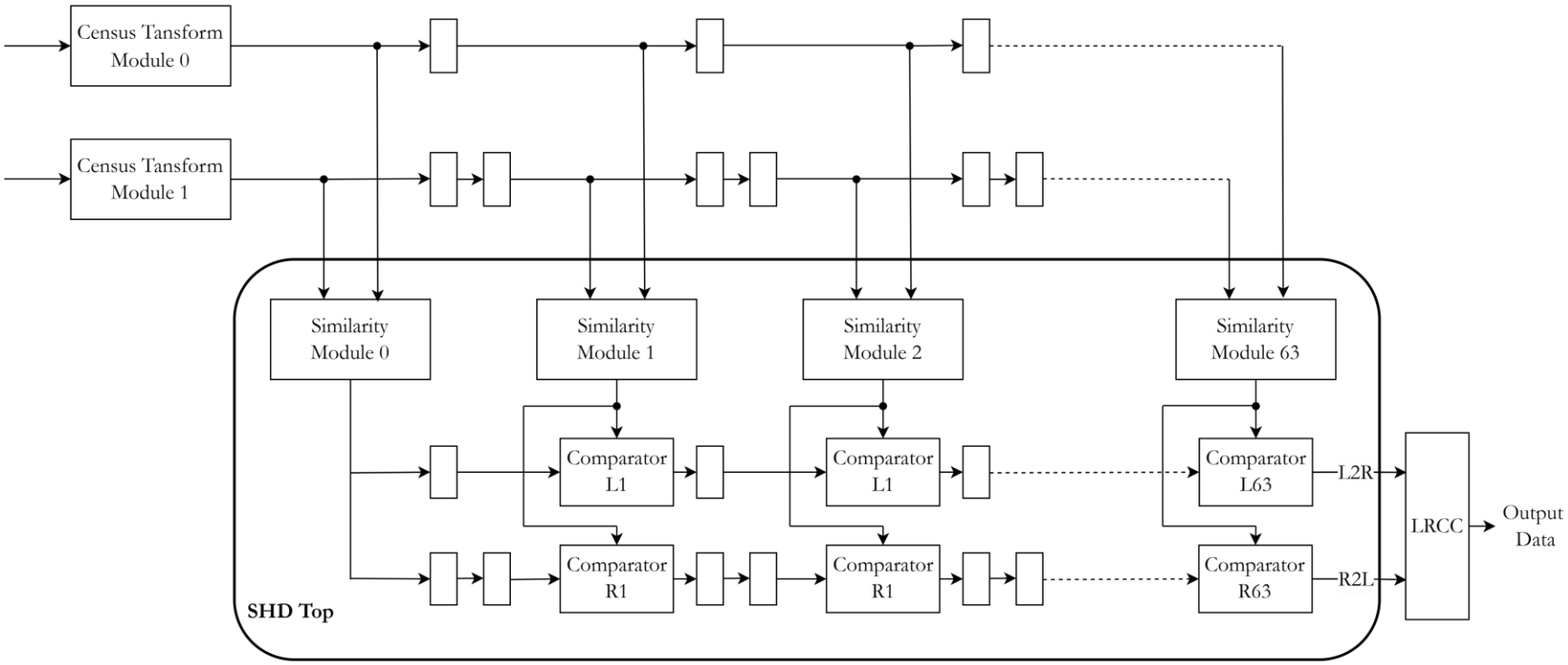
Analysis of the stereo vision accelerator under permanent and transient fault models using simulation and emulation-based strategies.

Outline

1. Introduction
2. **Stereo Vision Core**
3. Reliability Assessment Approach
4. Experimental Results
5. Conclusion and Future Work

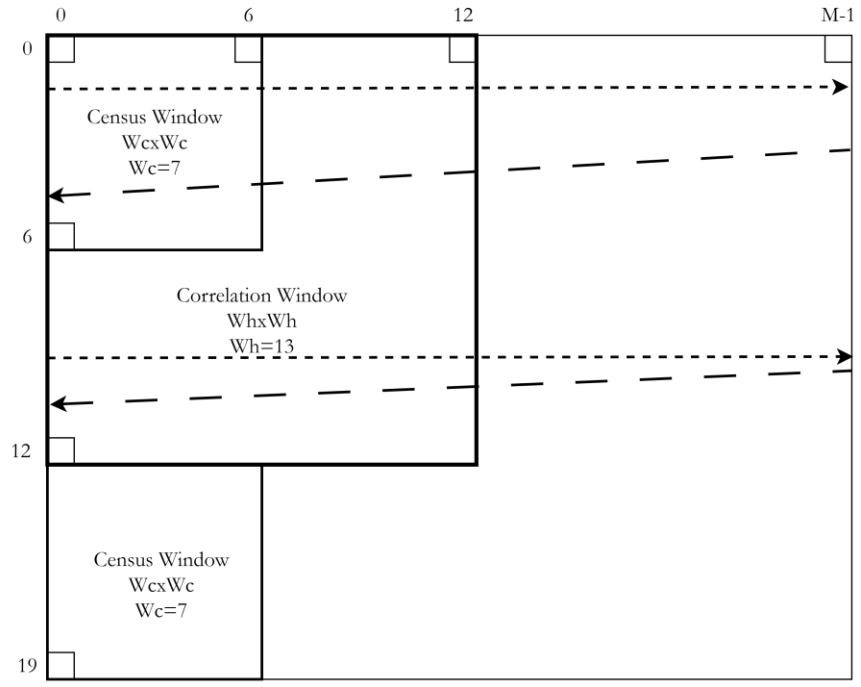
2. Stereo Matching Core

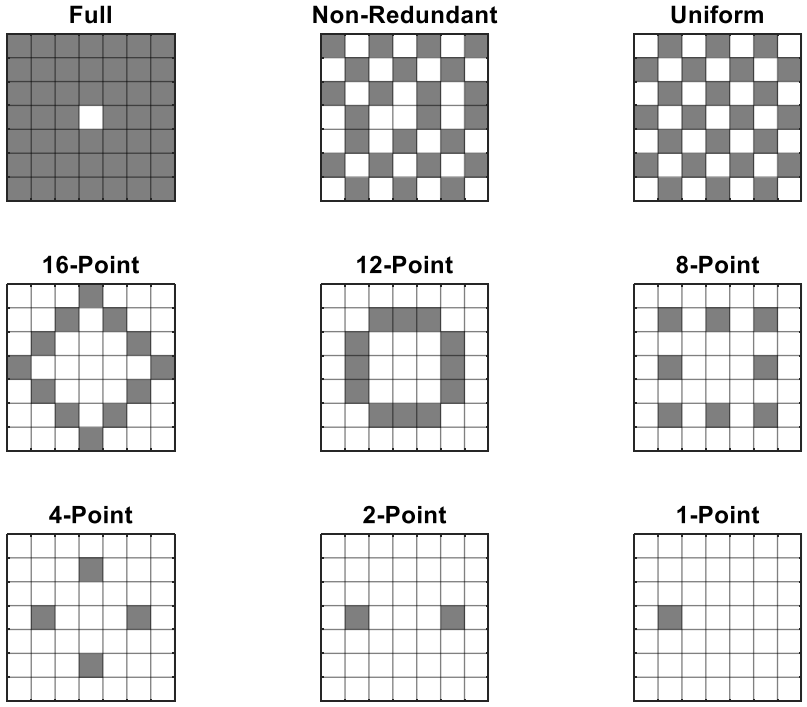
- The architecture of the stereo vision accelerator based on census transform.



2. Census Transform

- Nine kernel configurations, three window sizes: 5x5, 7x7, and 9x9.





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3. Reliability Assessment - Approaches

Simulation-based

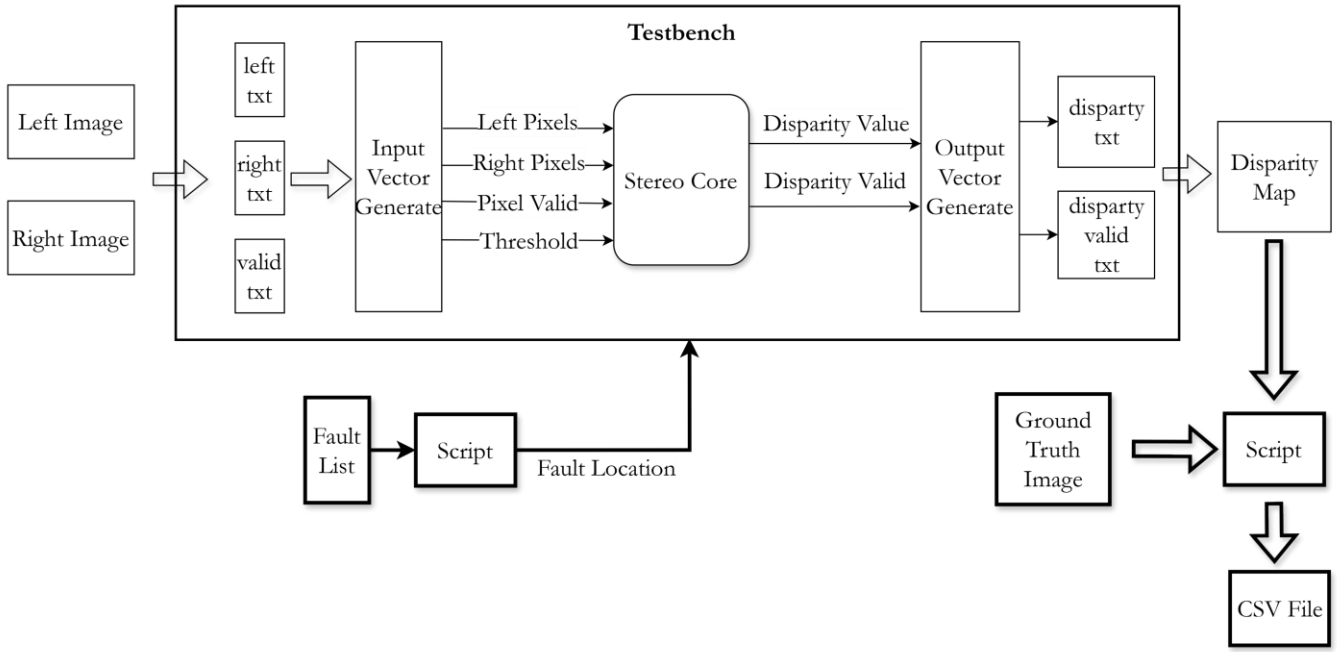
- Questa simulator
  - Stuck at fault with commands
  - RTL fault injection

Emulation-based

- Verilator for the fault injection
  - Open Source
  - Verilog Compatibility
  - High-Speed Simulation
- Hyper-FPGA
  - FPGA and CPU
  - High-Performance Computing

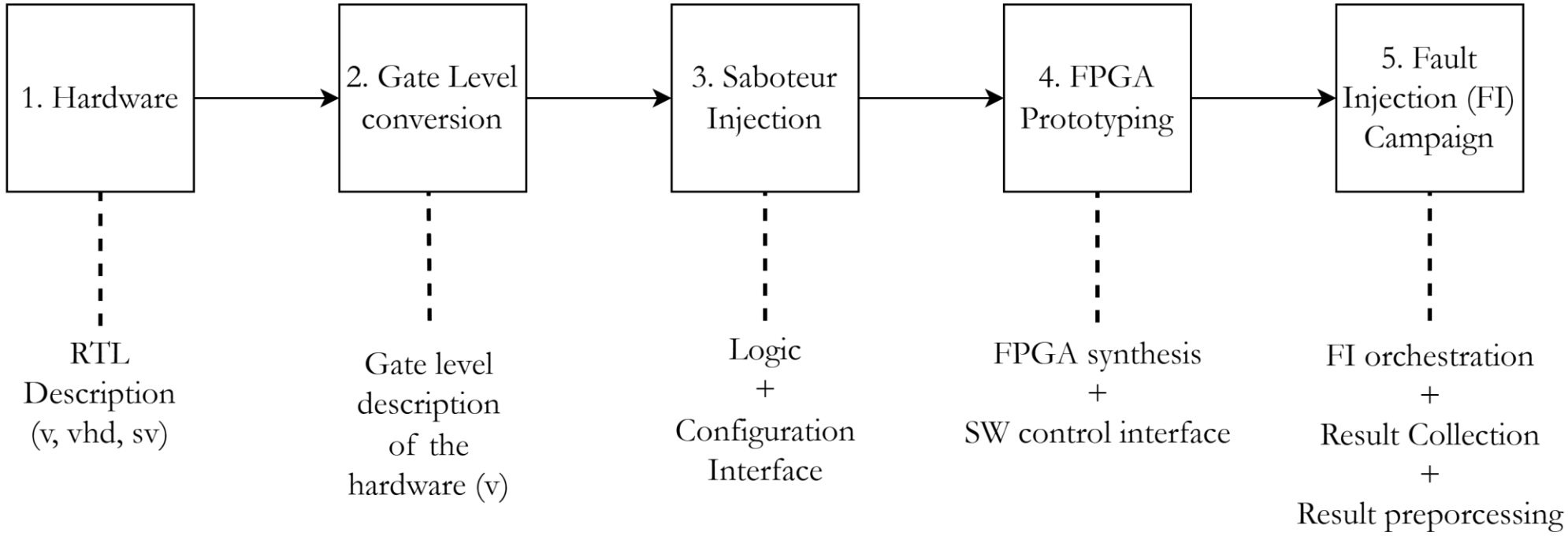
3.1. Simulation-based Strategy

- Fault injection environment by using Questa simulator.
- The Python script for the statistics calculation.
- The metrics: Accuracy, PSNR, and SNR.



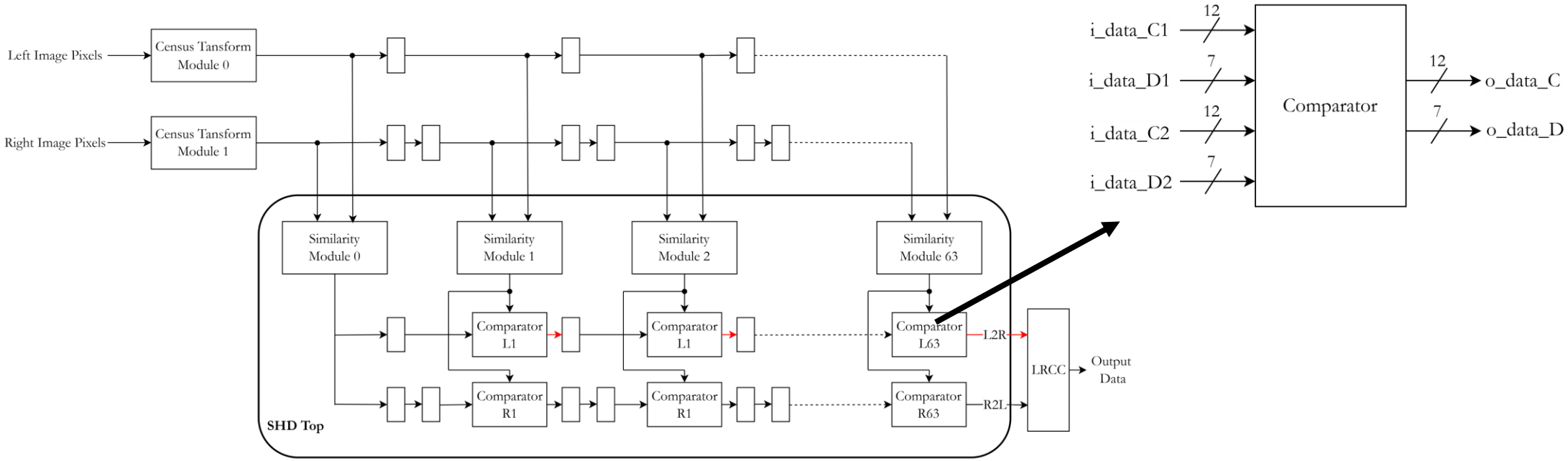
3.2. Emulation-based Strategy

- The strategy to implement the accelerator in the FPGA.



3.2. Emulation-based Strategy: Hardware

- The selected component for the fault injection: Comparator module
- The fault list length is 2394.



3.2. Emulation-based Strategy: Gate-level conversion

- Yosys can translate between different hardware description languages.
- Advantage of using gate-level netlist.

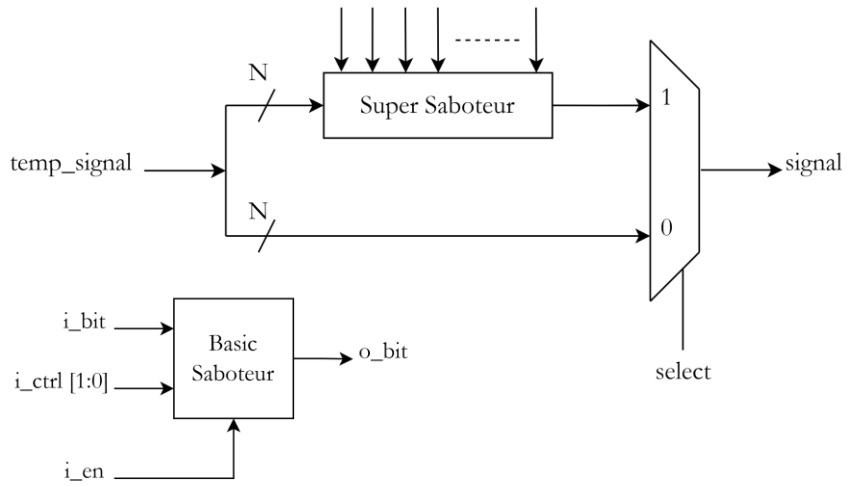
```vhdl
library IEEE; use IEEE.STD_LOGIC_1164.ALL;

entity mux2x1 is
          Port ( a   : in STD_LOGIC;
                 b   : in STD_LOGIC;
                 sel : in STD_LOGIC;
                 y   : out STD_LOGIC
               );
end mux2x1;

architecture rtl of mux2x1 is
begin
    y <= a when sel = '0' else b;
end rtl;
```

```verilog
module mux2x1 (
    input wire a,
    input wire b,
    input wire sel,
    output wire y
);

    wire sel_n, and_a, and_b;

    not  (sel_n, sel);
    and  (and_a, a, sel_n);
    and  (and_b, b, sel);
    or   (y, and_a, and_b);

endmodule
```

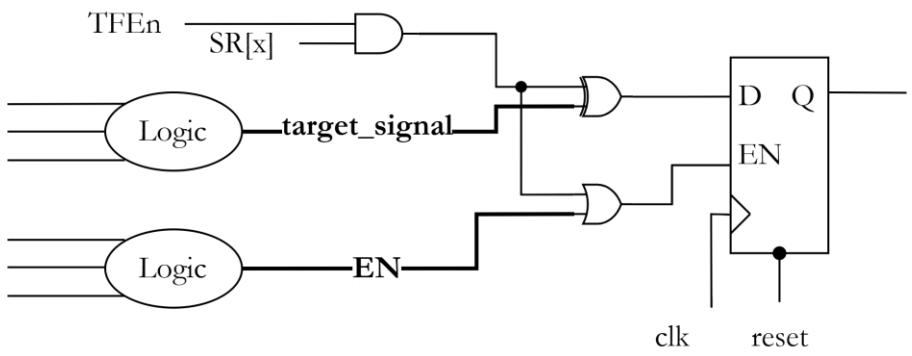
3.2. Emulation-based Strategy: Saboteur Injection

- Python script: inserting the logic, creating a report

- Saboteur
  - Stuck-at-fault, bit flip
  - Combinational logic

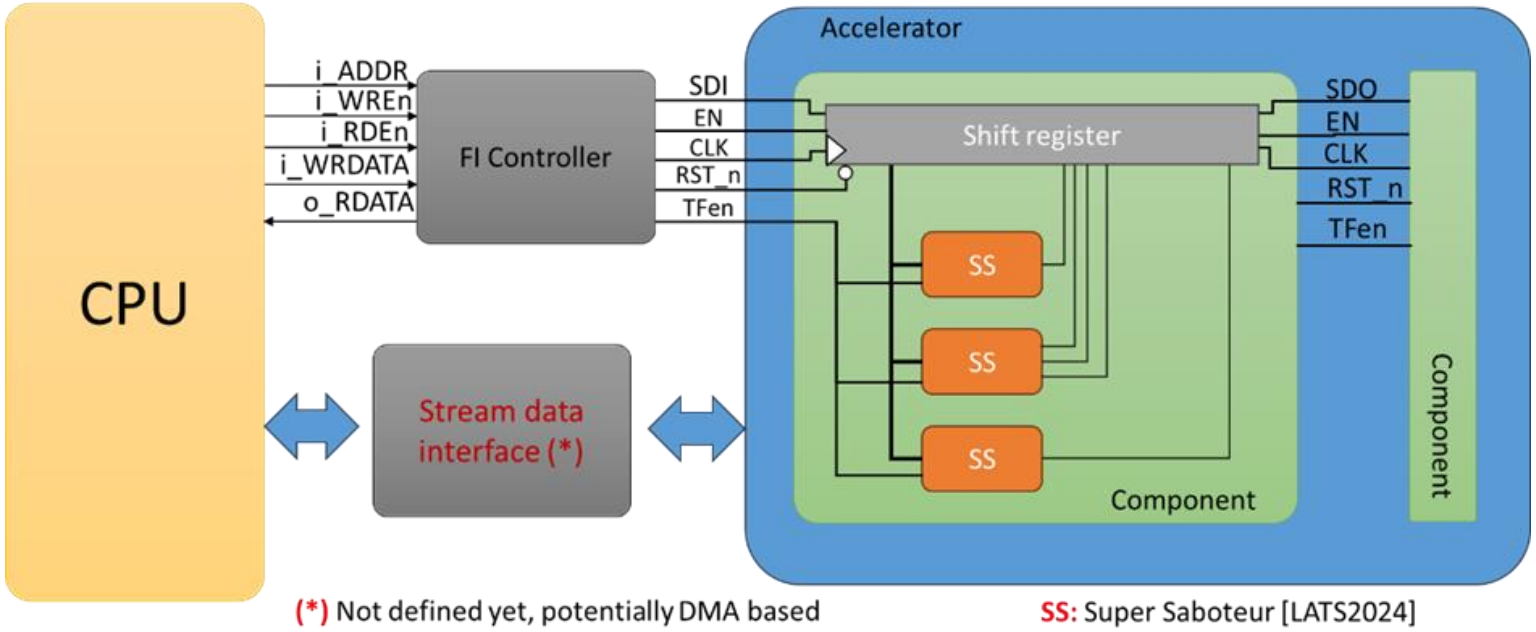


- Single Event Upset (SEU)
  - Transient fault
  - Sequential logic



3.2. Emulation-based Strategy: FPGA Prototyping

- The accelerator with saboteurs
- The controller establishes a handshake protocol.
- The stream data interface is for image transfer.



3.2. Emulation-based Strategy: FI Campaign

- Designer can select:
  - Target bit/s,
  - Fault type,
  - Image.

- The designer can perform post-processing.

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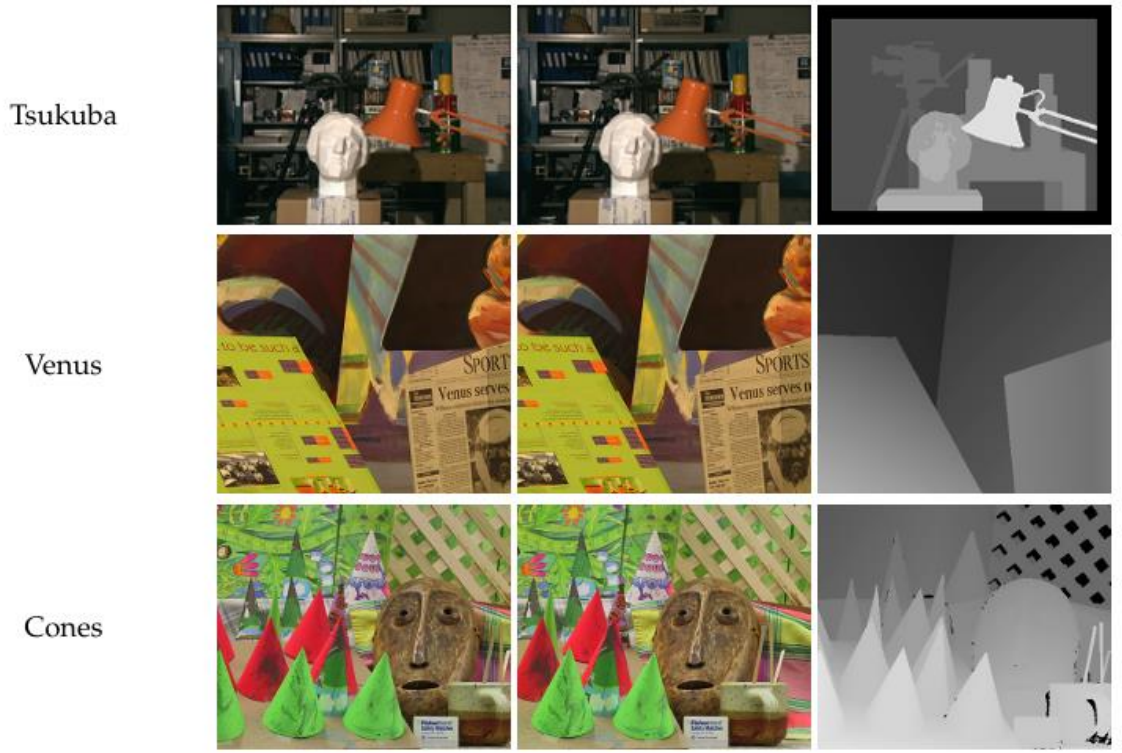
3. Reliability Assessment Approach
4. **Experimental Results**
5. Conclusion and Future Work

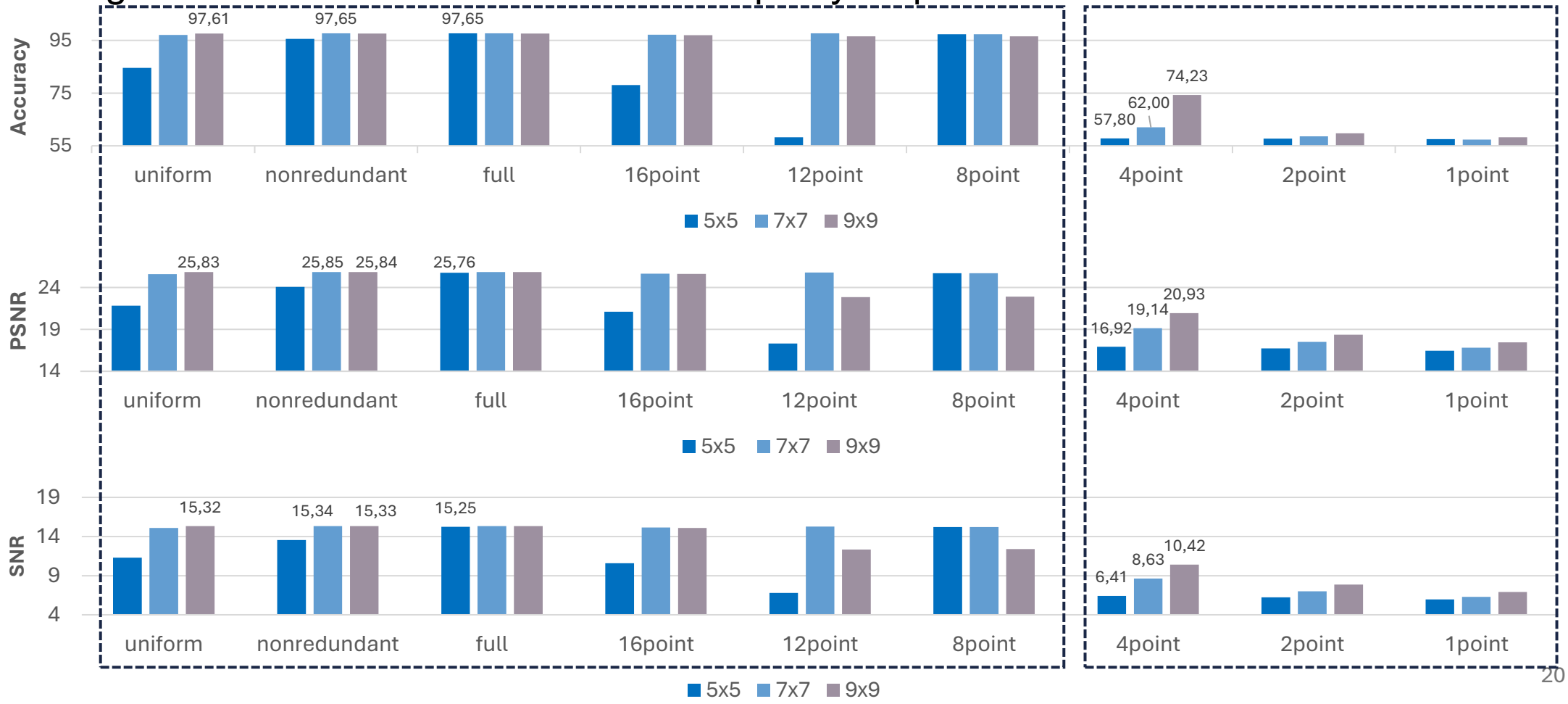
4. Experimental Results

- Middelbury stereo dataset: Tsukuba, Venus, and Cones.
- Fault-free & faulty simulation results for the Venus image.
- Faulty simulations based on:
  - Uniform configuration
  - 7x7 window size



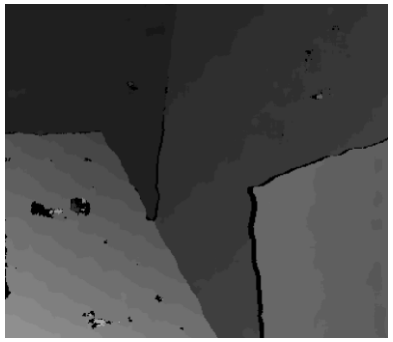
4.1. Fault-free Simulation Results

- The golden results for the accelerators' disparity maps.

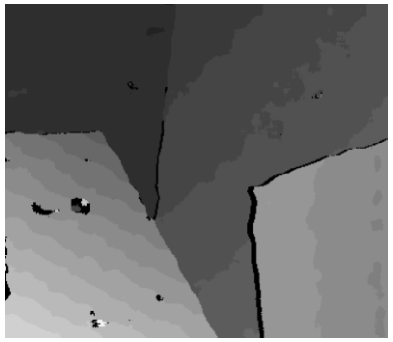


4.1. Fault-free Simulation Results

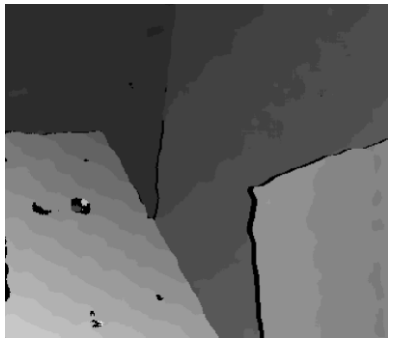
- Comparison between uniform and 1-point designs.



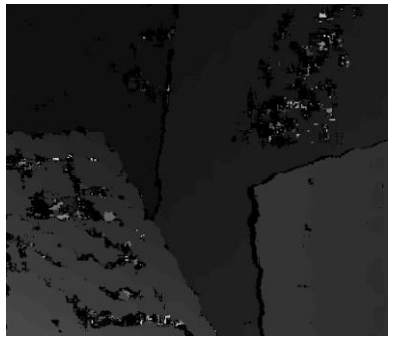
Uniform, 5x5
84.57%



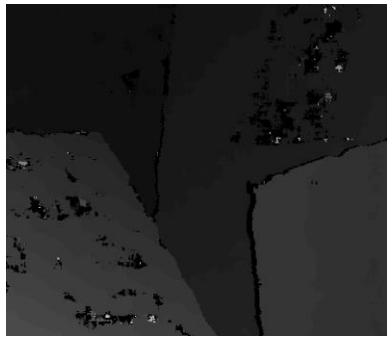
Uniform, 7x7
97.03%



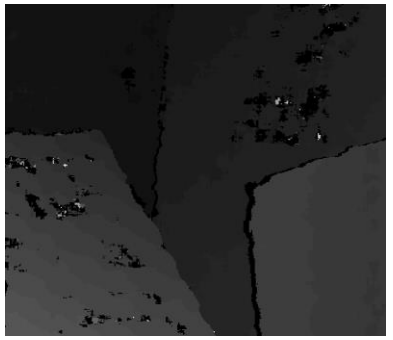
Uniform, 9x9
97.61%



1-point, 5x5
57.56%



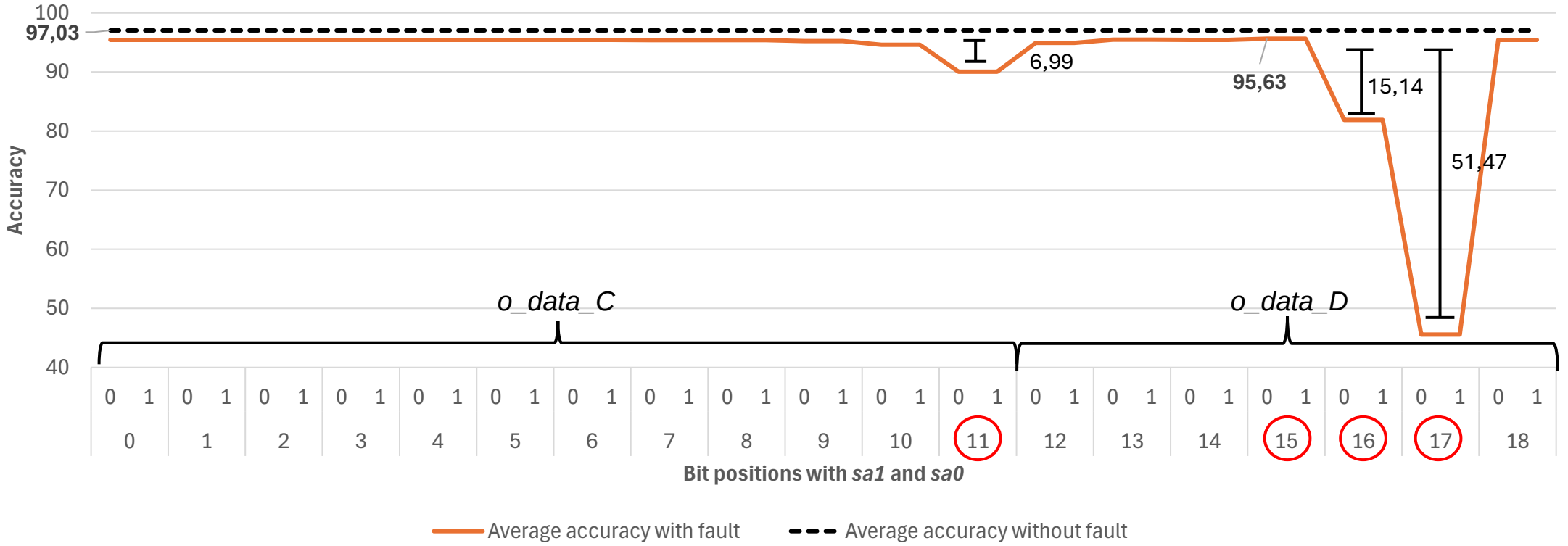
1-point, 7x7
57.40%



1-point, 9x9
58.56%

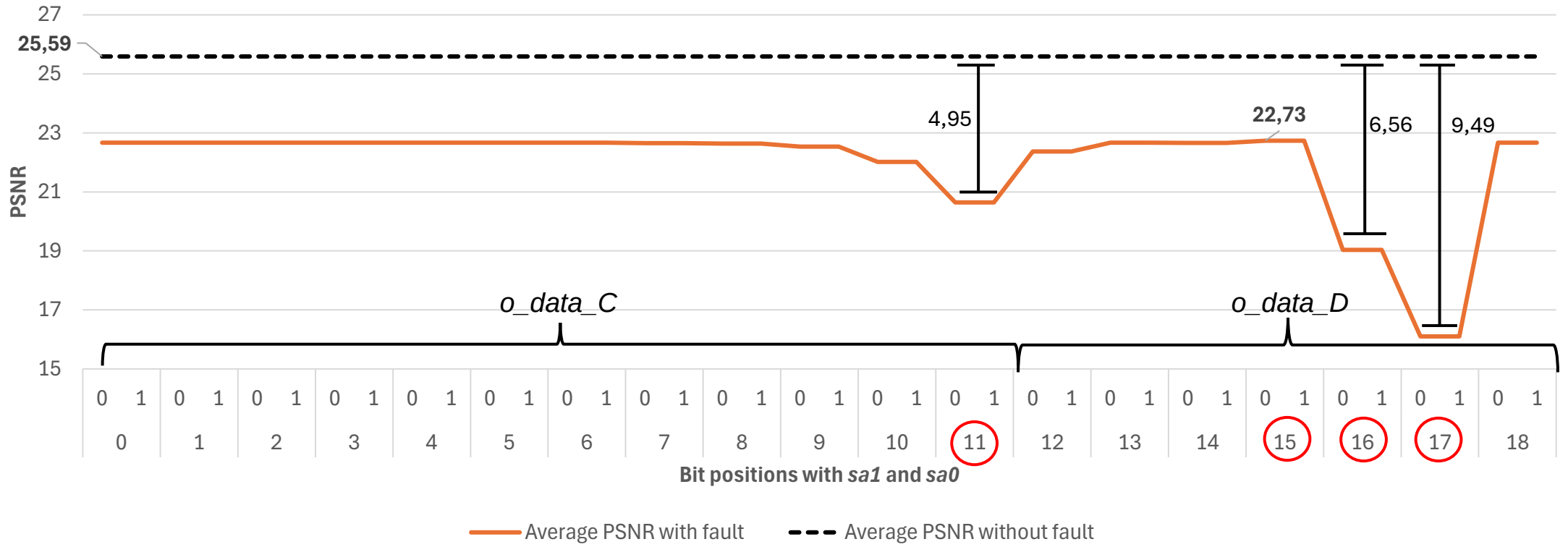
4.2. Faulty Simulation: Accuracy

- The average accuracy, for each bit position across all 63 components under SA faults.



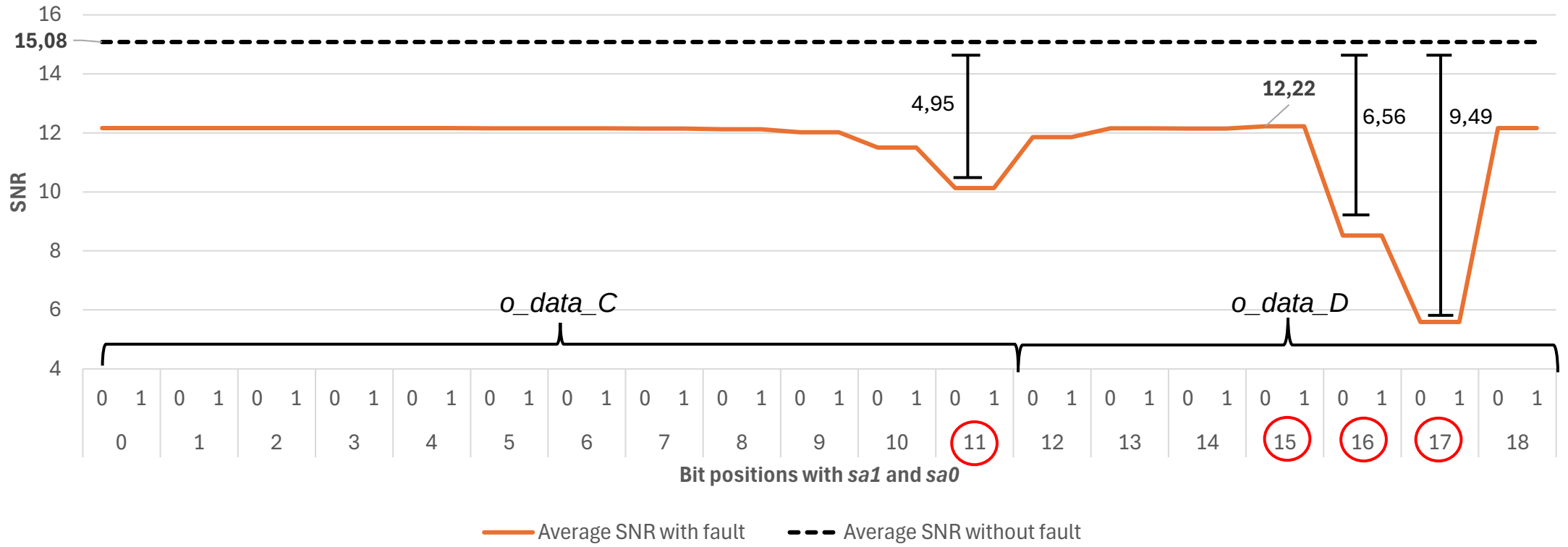
4.2. Faulty Simulation: PSNR

- The average PSNR, for each bit positions across all 63 components under SA faults.



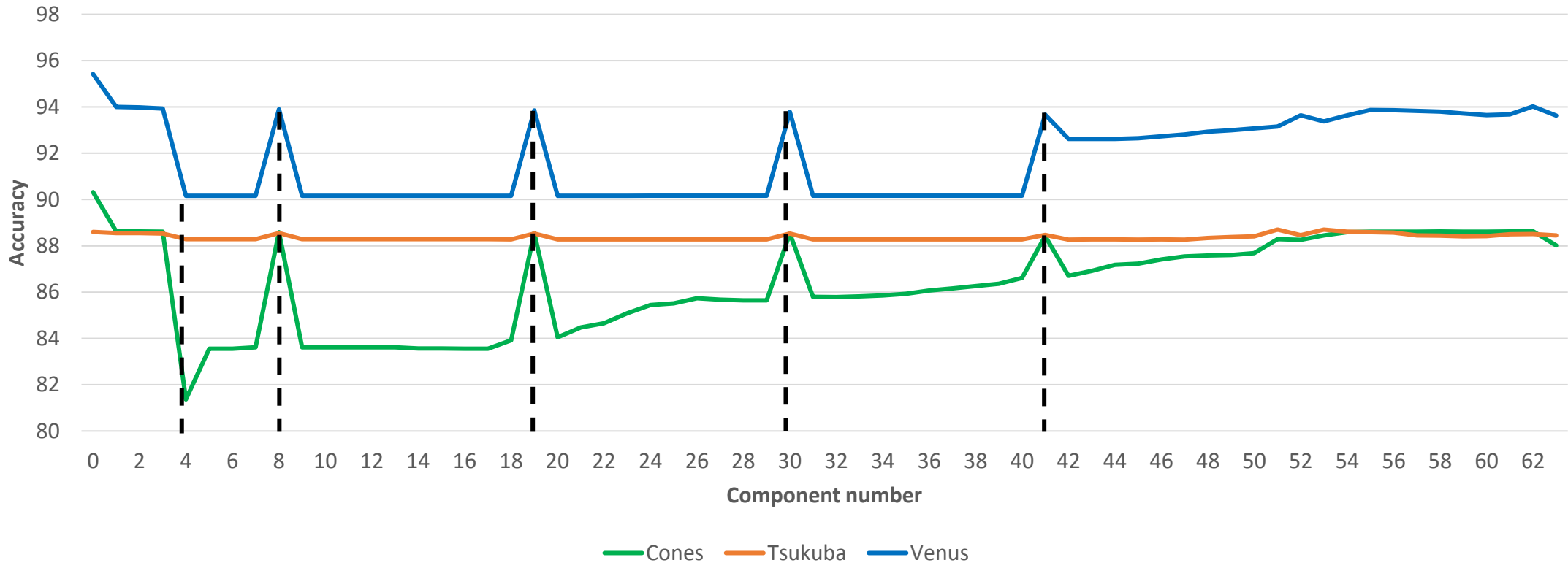
4.2. Faulty Simulation: SNR

- The average SNR, for each bit positions across all 63 components under SA faults.



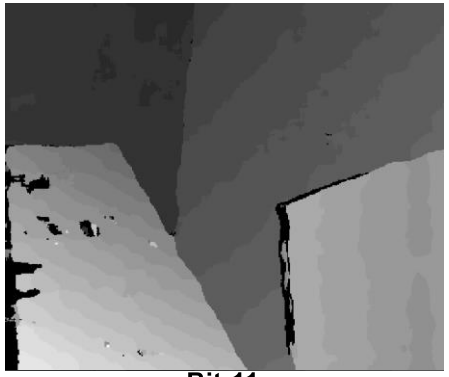
4.2. Faulty Simulation: Through the components

- The average of the 19 bits, including SA0 and SA1, for each of the 63 components.
- The components 4, 8, 19, 30, and 41.

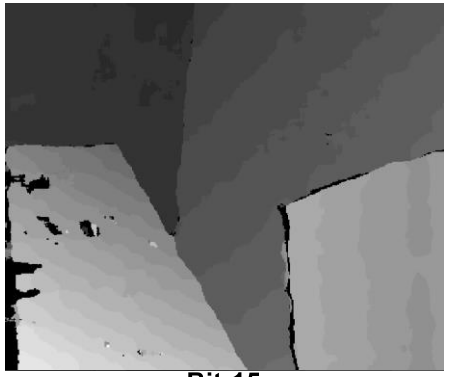


4.2. Faulty Simulation: The worst-case example

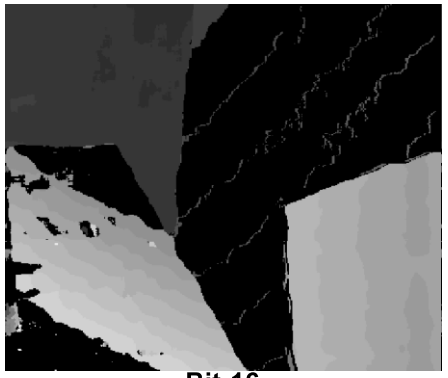
- Golden values for the design were:
  - Accuracy: 97.03%
  - PSNR: 25.59 dB
  - SNR: 15.08 dB



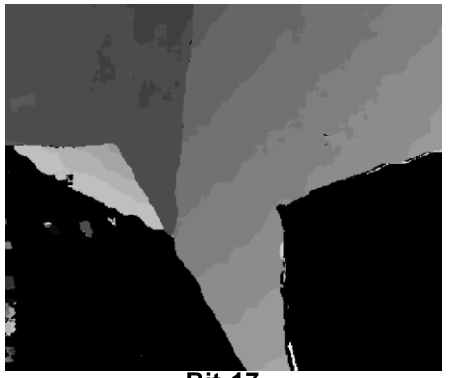
Bit-11
Accuracy: 90.04%
PSNR: 20.64 dB
SNR: 10.13 dB



Bit-15
Accuracy: 95.63%
PSNR: 22.73 dB
SNR: 12.22 dB



Bit-16
Accuracy: 81.89%
PSNR: 19.03 dB
SNR: 8.52 dB



Bit-17
Accuracy: 45.56%
PSNR: 16.10 dB
SNR: 5.59 dB

4.3. Simulation Times

- Emulation-based strategy (the Verilator) is more time-efficient.

- The elapsed time depends on the image size.

	Fault-free	**Faulty**
Simulation-based	~ 6-8 min for 1 design	650 faults => 50-70 hours
Emulation-based (the Verilator)	~ 10-20 sec for 1 design	2394 faults => 4-6 hours

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5.1. Conclusion

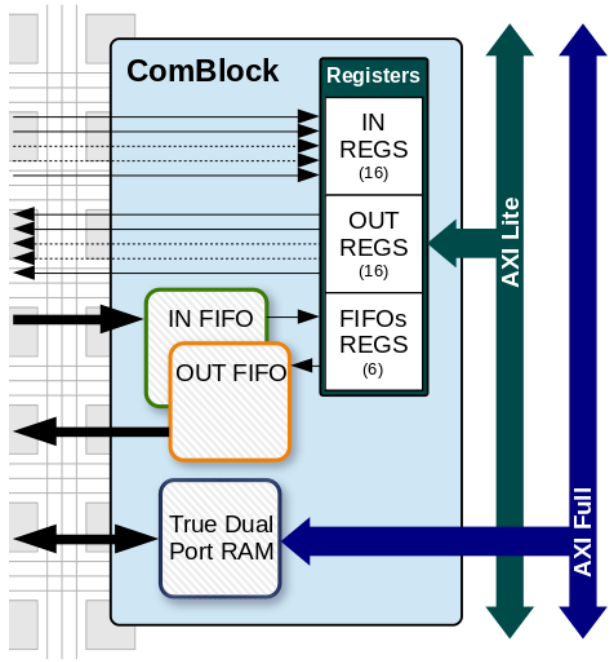
- In this project, we aimed to measure the reliability of the stereo vision accelerator under permanent faults.

- We developed two strategies and worked on their implementation.

- The bit positions that consistently fall below the average accuracy have always been the most significant bits, with an average drop of 38.04%.

5.2. Future Work

- The target FPGA is the hyper-FPGA cluster from ICTP MLAB.
- The accelerator integration: the ComBlock.
- The stream data interface.



Thank you

April 2025