

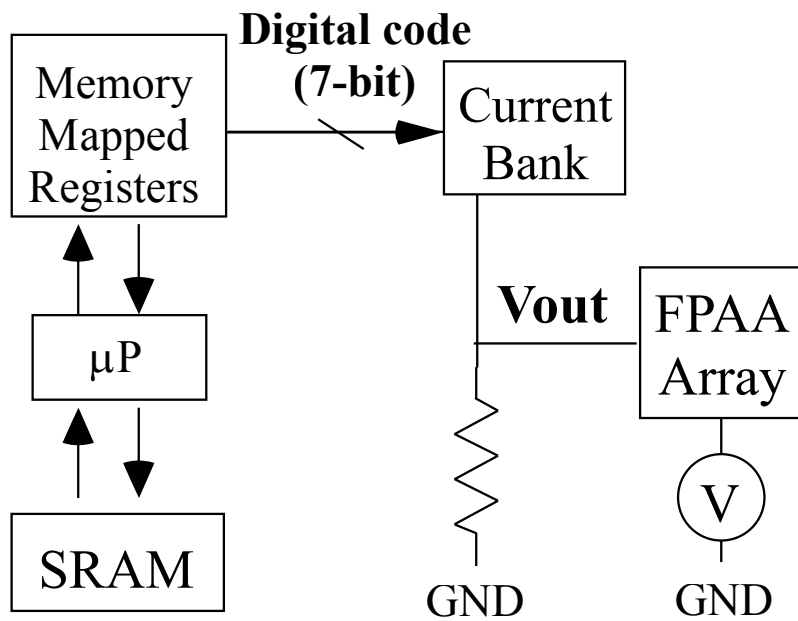
Block name: GENARB\_f

Number of inputs: 0

Number of outputs: 1

Parameter list: Waveform Variable name, Sample rate

Block description: Arb Waveform (Arbitrary waveform generator) blocks, consisting of a current bank and a resistor, interface with the  $\mu$ P through memory mapped registers. The input is compiled as a vector on the SRAM. Run mode assembly code sends the input vector uploaded on SRAM to a memory mapped register at a given frequency.



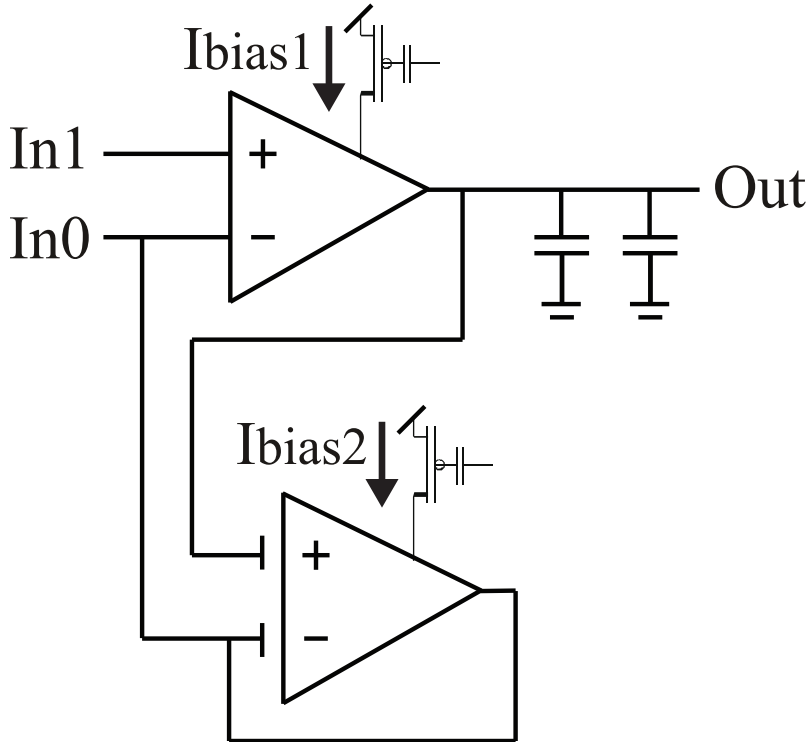
Block name: L\_SenseAmp

Number of inputs: 2

Number of outputs: 1

Parameter list: L\_SenseAmp\_ota0\_ibias, L\_SenseAmp\_fgota0\_ibias, L\_SenseAmp\_fgota0\_pbias, L\_SenseAmp\_fgota0\_nbias, L\_SenseAmp\_cap0, L\_SenseAmp\_cap1

Block description: A Current Sense Amplifier block using an OTA, an FG OTA, and two capacitors. Ibias1 is L\_SenseAmp\_ota0\_ibias, which has a default value of  $2\mu\text{A}$ . Ibias2 is L\_SenseAmp\_fgota0\_ibias, which has a default value of  $2\mu\text{A}$ . The FGOTA's pbias is L\_SenseAmp\_fgota0\_pbias, which has a default value of  $2\mu\text{A}$ . The FGOTA's nbias is L\_SenseAmp\_fgota0\_nbias, which has a default value of  $2\mu\text{A}$ . It has two capacitor variables, which are L\_SenseAmp\_cap0 and L\_SenseAmp\_cap1.



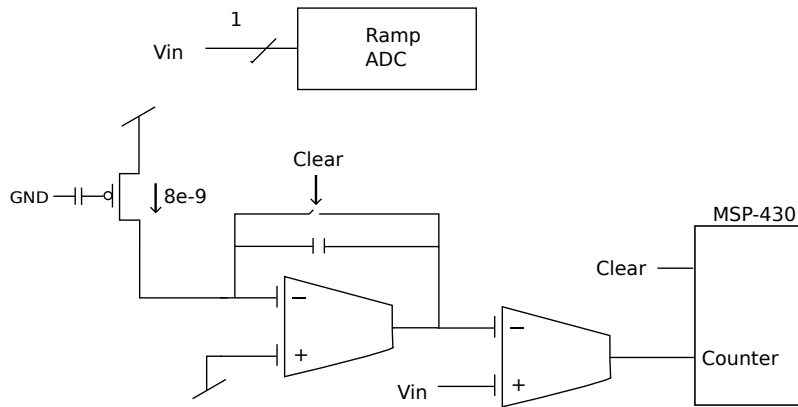
Block name: Ramp\_ADC

Number of inputs: 1

Number of outputs: 0

Parameter list: NA

Block description: Single slope Analog to digital Converter. The input is to a FG comparator, which allows for higher dynamic range. The input current to the integrator is via a FG transistor and is set to 8nA. Advanced users could change this from inside the block definition to change number of bits and speed of the ADC. The counter is implemented on the processor on-chip. Take DATA button is used to get the output of the Ramp ADC. The output is stored in a .csv file called Results.csv. One can use the command `Out=csvRead('Results.csv')` to store it in a variable inside scilab. RAMP ADC performs data acquisition with a fixed sampling rate depending on the input voltage (100us maximum time between samples). Hence the sampling rate of the system will be determined by the sampling rate of the DAC (ARB GEN block).



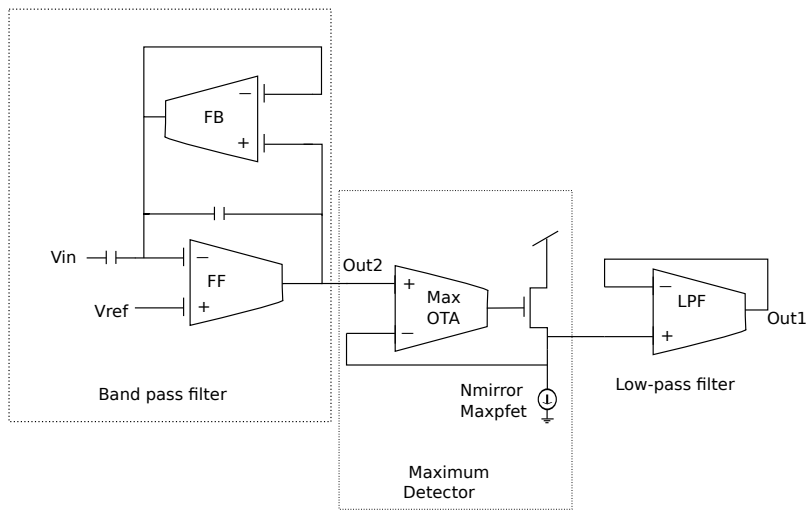
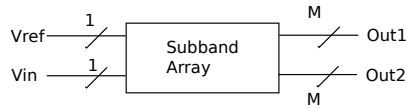
Block name: SubbandArray

Number of inputs: 2

Number of outputs: 2

Parameter list: num\_of\_blk, SubbandArray\_Maxpfet,  
SubbandArray\_FBbias, SubbandArray\_FBpbias, SubbandArray\_FBnbias,  
SubbandArray\_FFbias, SubbandArray\_FFpbias, SubbandArray\_FFnbias,  
SubbandArray\_Maxota, SubbandArray\_LPF, SubbandArray\_FFcap,  
SubbandArray\_FBcap

Block description: Analog Front-end used to extract frequency spectrum of a signal. The block consists of band-pass filter, maximum detector and Low-pass filter. Inputs are all connected to one node. Outputs are vectorized to have M.



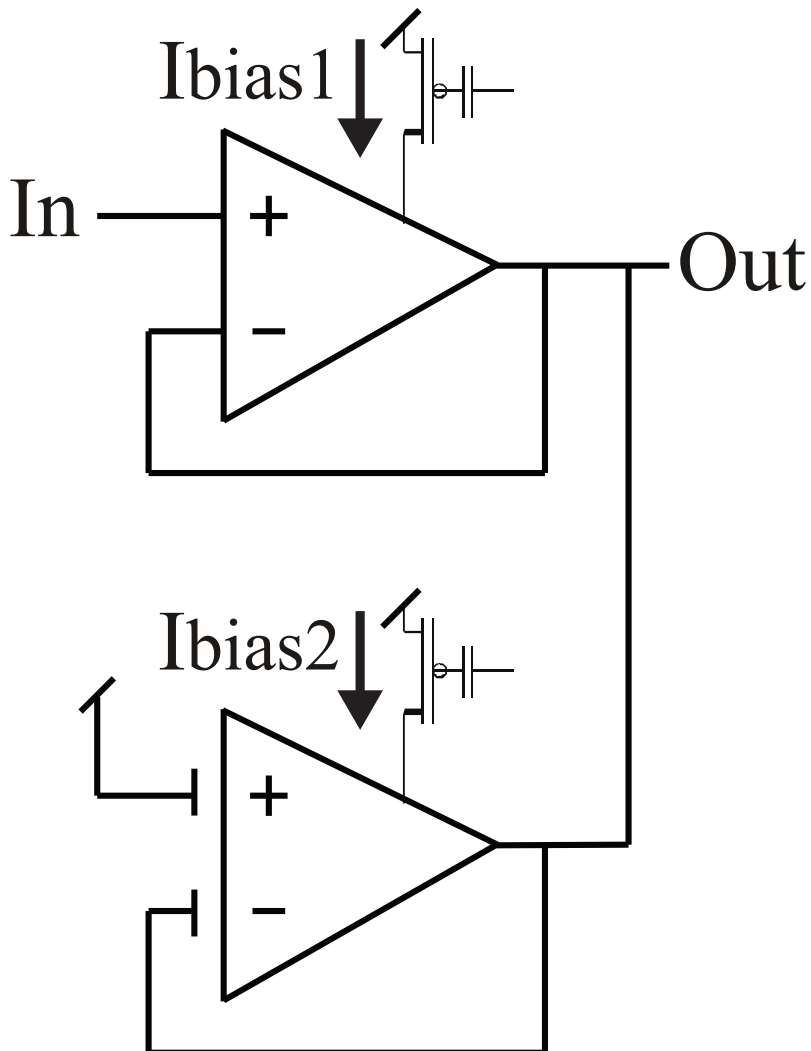
Block name: VolDivide1

Number of inputs: 1

Number of outputs: 1

Parameter list: VolDivide1\_ota0\_ibias, VolDivide1\_fgota0\_ibias, VolDivide1\_fgota0\_pbias, VolDivide1\_fgota0\_nbias

Block description: A Voltage divider block using an OTA and an FG OTA. Ibias1 is VolDivide1\_ota0\_ibias, which has a default value of  $2\mu\text{A}$ . Ibias2 is VolDivide1\_fgota0\_ibias, which has a default value of  $2\mu\text{A}$ . The FGOTA's pbias is VolDivide1\_fgota0\_pbias, which has a default value of  $2\mu\text{A}$ . The FGOTA's nbias is VolDivide1\_fgota0\_nbias, which has a default value of  $2\mu\text{A}$ .



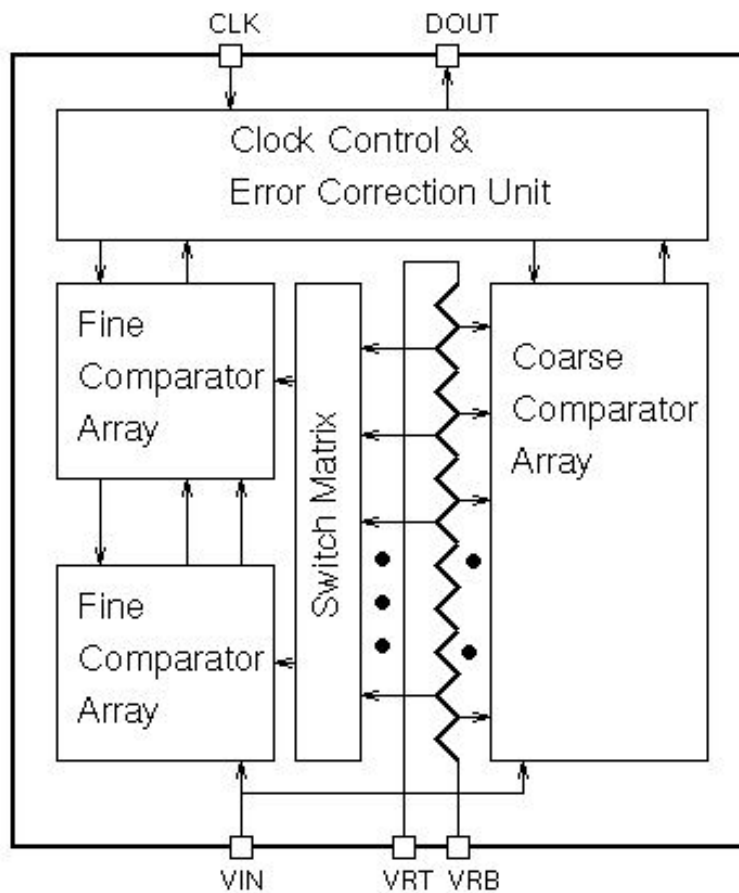
Block name: adc\_ip

Number of inputs: 1

Number of outputs: 0

Parameter list: none

Block description: ADC (8bit 20MHz) is an 8-bit CMOS A/D converter (TAD3308A), which is a TSMC IP block. The cell receives analog input signal and decodes to digital output signals. Sampling rate is controlled by the clock input signal.



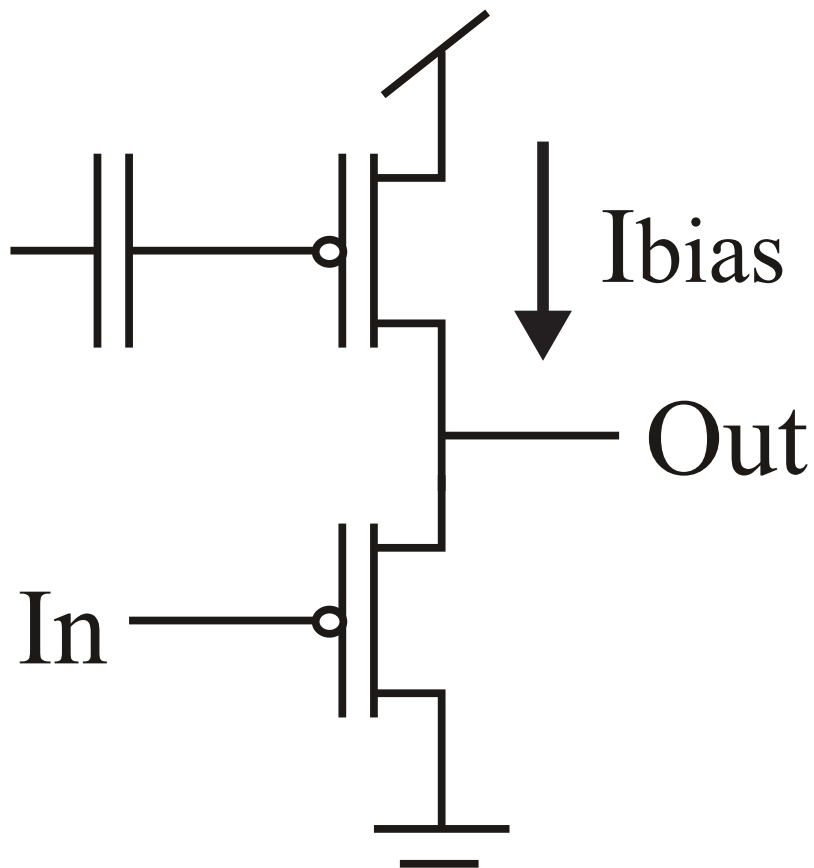
Block name: common\_drain

Number of inputs: 1

Number of outputs: 1

Parameter list: common\_drain\_fgswc\_ibias

Block description: A common drain circuit using a pFET and FG device. The parameter, common\_drain\_fgswc\_bias, sets the bias current, which has a default value of 50nA.



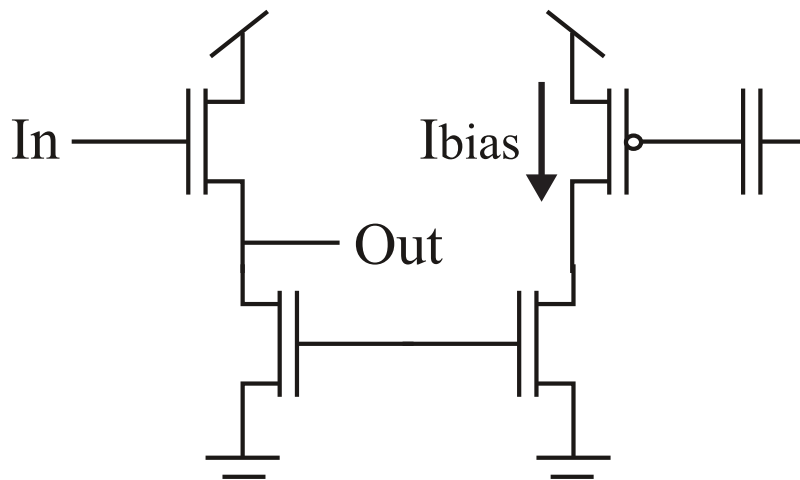
Block name: common\_drain\_nfet

Number of inputs: 1

Number of outputs: 1

Parameter list: common\_drain\_nfet\_ibias

Block description: A common drain circuit using a nfet and a current mirror with a FG device setting the bias current. The parameter, common\_drain\_nfet\_ibias, sets the bias current, which has a default value of 50nA.





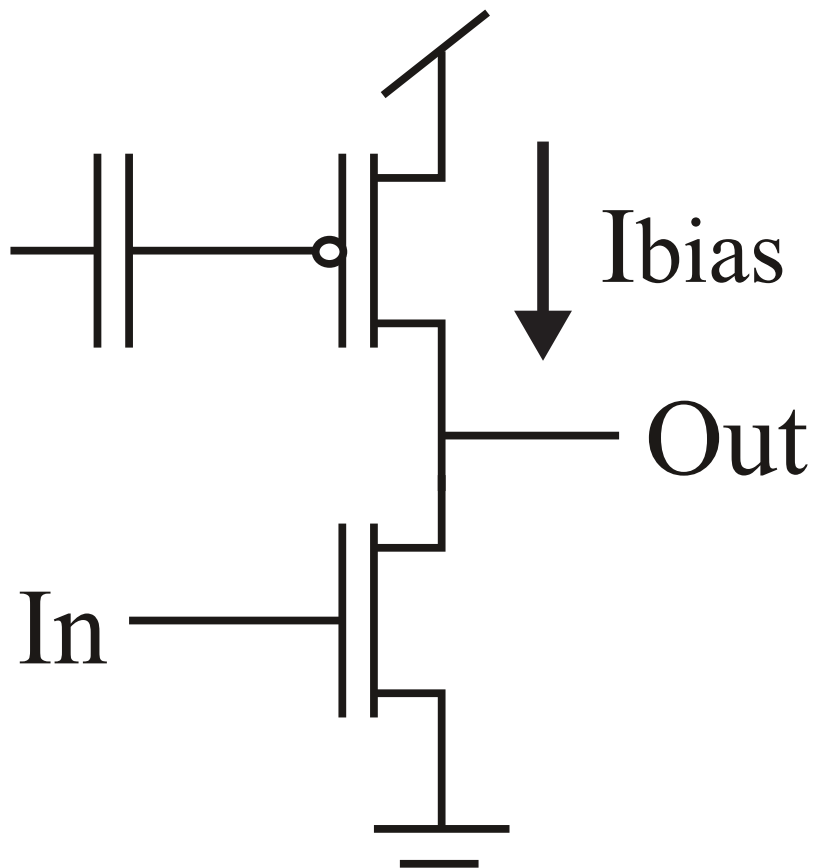
Block name: common\_source

Number of inputs: 1

Number of outputs: 1

Parameter list: common\_source\_ibias

Block description: A common source circuit using a nFET and FG device. The parameter, common\_source\_ibias, sets the bias current, which has a default value of 50nA.



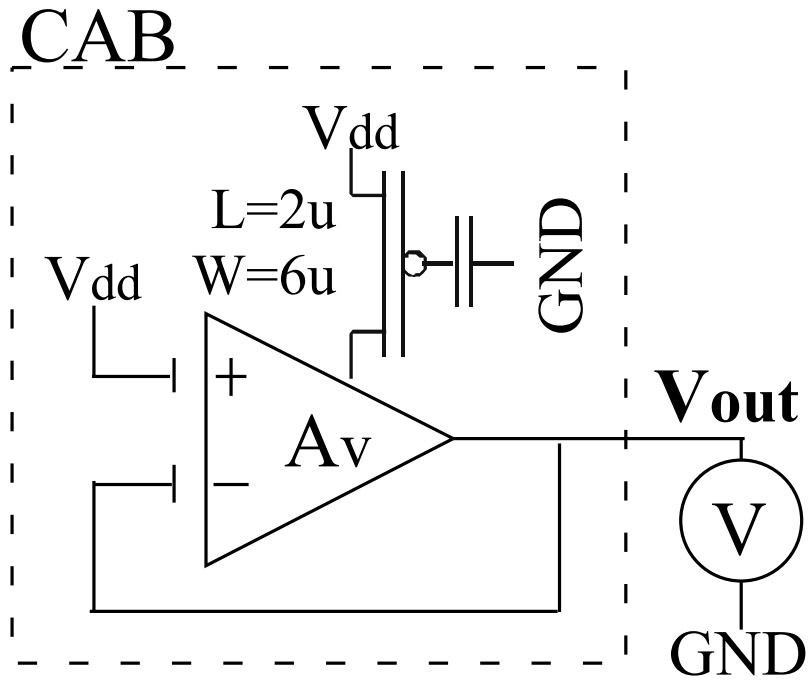
Block name: dc\_in

Number of inputs: 0

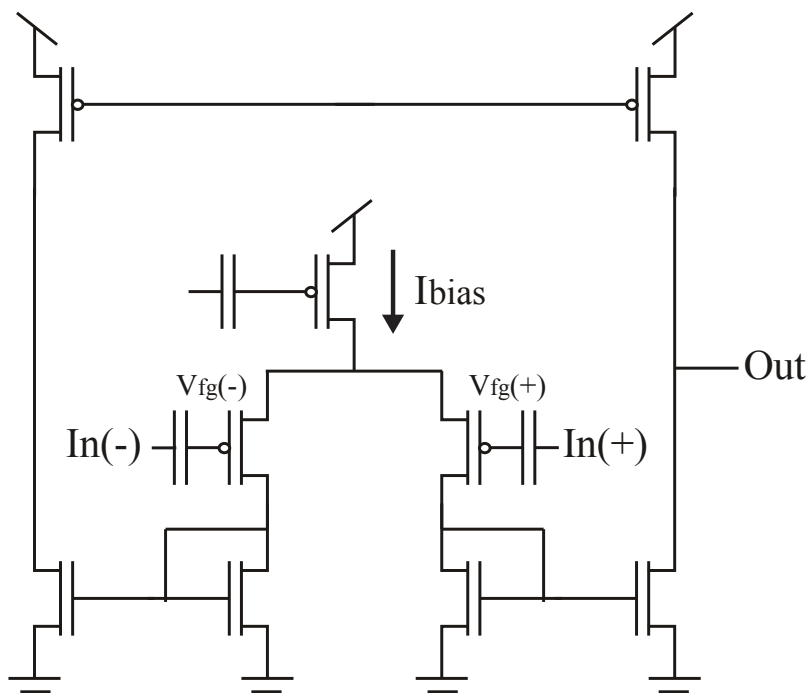
Number of outputs: 1

Parameter list: DC Value

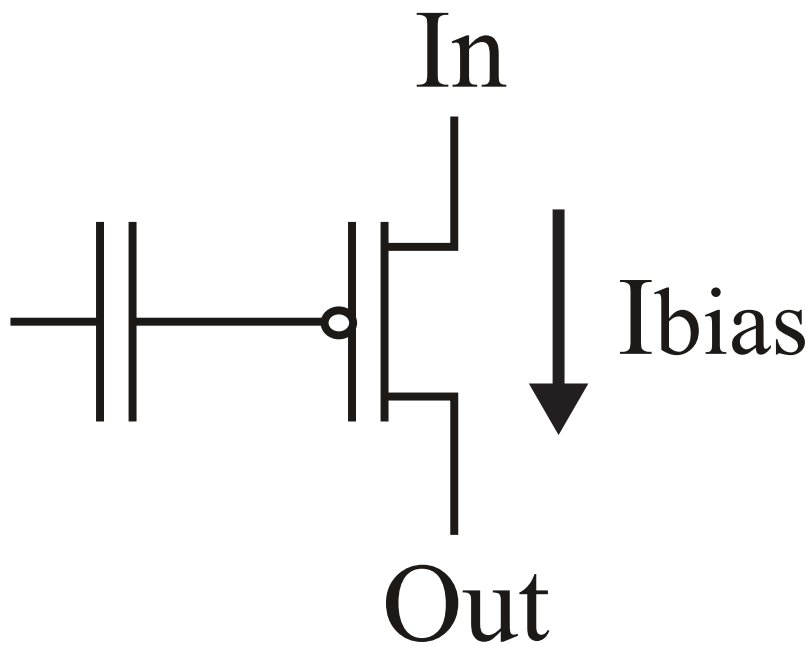
Block description: DC Voltage: A compiled block in a CAB to set a DC voltage, comprises of an FG OTA in a unity-gain follower configuration.



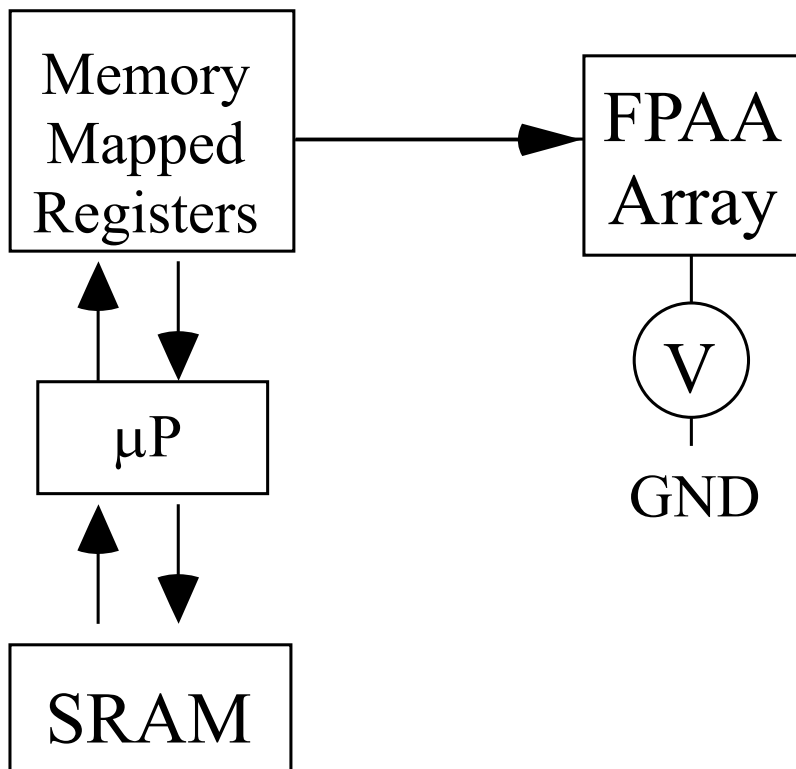
Block description: A nine transistor OTA block with input FG devices, which is one analog element blocks. Ibias controls the bias current. Vfg\_n and Vfg\_p define input FG pFET's floated node voltage, respectively.



Block name: fgswitch  
Number of inputs: 1  
Number of outputs: 1  
Parameter list: fgswitch\_fgswc\_ibias  
Block description: An FG switch. fgswitch\_fgswc\_ibias controls the bias current.



Block name: gpio\_in  
Number of inputs: 0  
Number of outputs: 1  
Parameter list: GPIO IN Variable name, sample rate  
Block description: Digital In blocks interfacing with the  $\mu$ P through memory mapped registers.



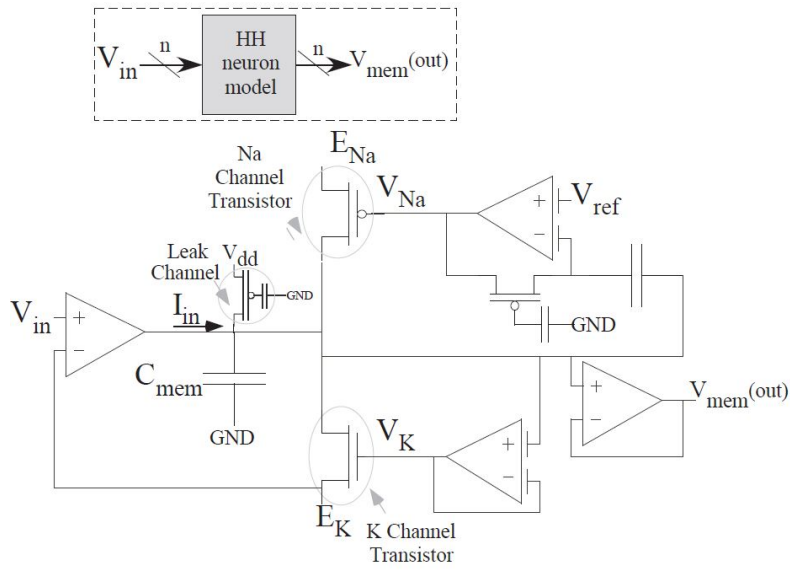
Block name: hhn

Number of inputs: 4

Number of outputs: 1

Parameter list: hhn\_fgswc\_ibias, hhn\_fgota1\_ibias, hhn\_fgota1\_pbias, hhn\_fgota1\_nbias, hhn\_fgota0\_ibias, hhn\_fgota0\_pbias, hhn\_fgota0\_nbias, hhn\_ota0\_ibias, hhn\_ota1\_ibias, hhn\_cap0

Block description: a Hodgkin Huxley neuron circuit.



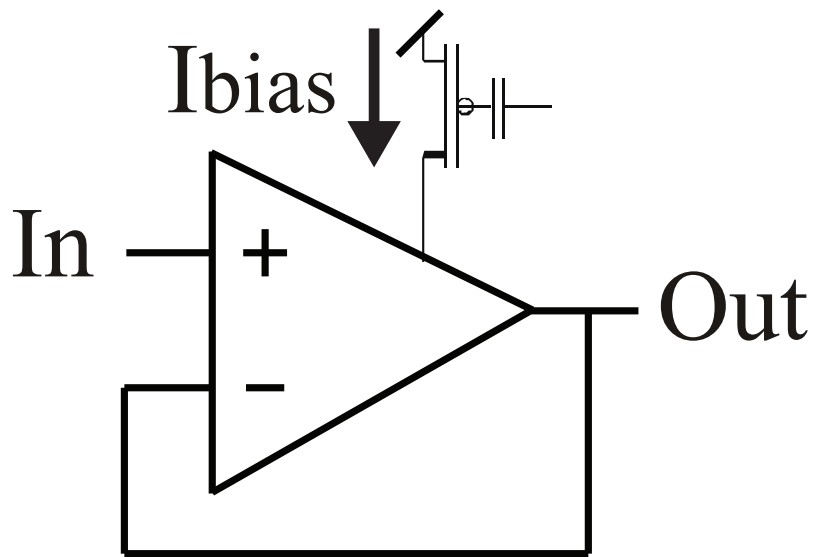
Block name: lpfota

Number of inputs: 1

Number of outputs: 1

Parameter list: Cutoff\_freq

Block description: A low pass filter block using an OTA. The default value of cutoff frequency is set to 21.7 Hz.



Block name: meas\_volt

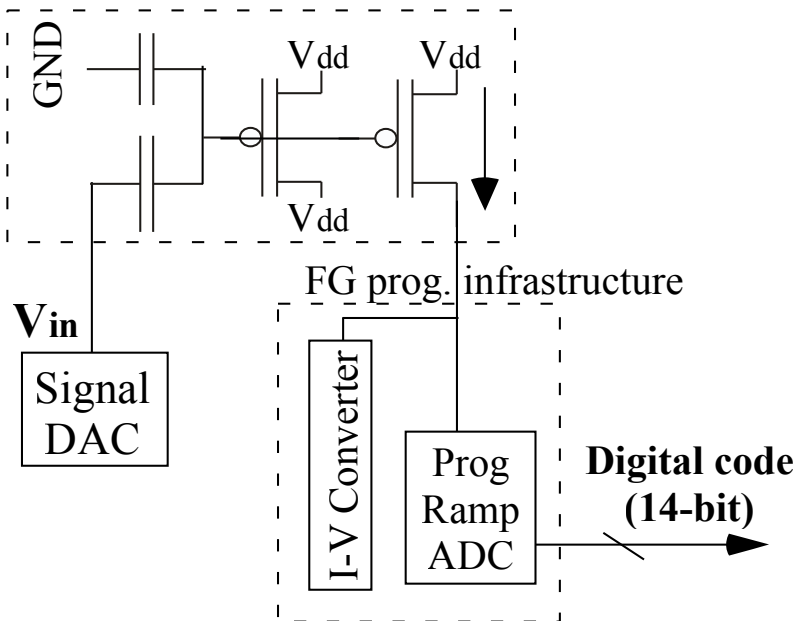
Number of inputs: 1

Number of outputs: 0

Parameter list: Variable name, sample rate

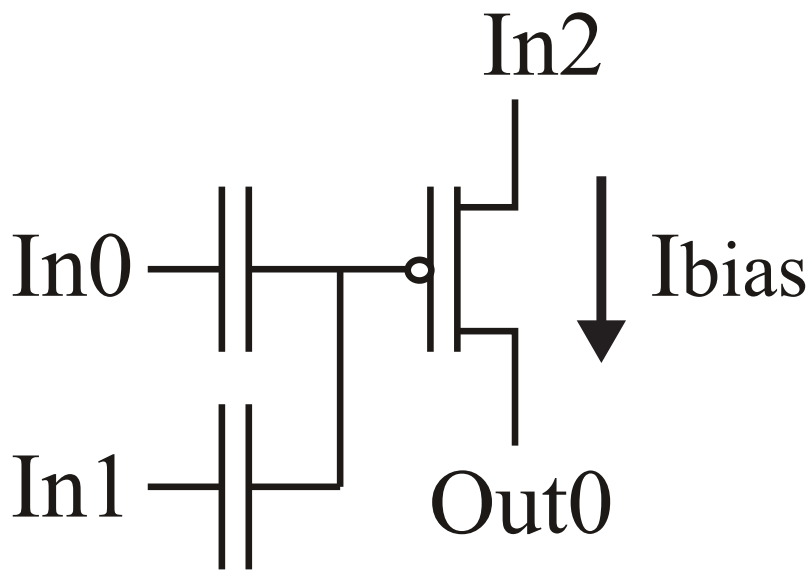
Block description: An ADC block using a Multiple-Input Translinear Element (MITE) device in a CAB couples , which is measured by a pFET diode I-V converter and a 14-bit ramp ADC in the program infrastructure.

## MITE in CAB

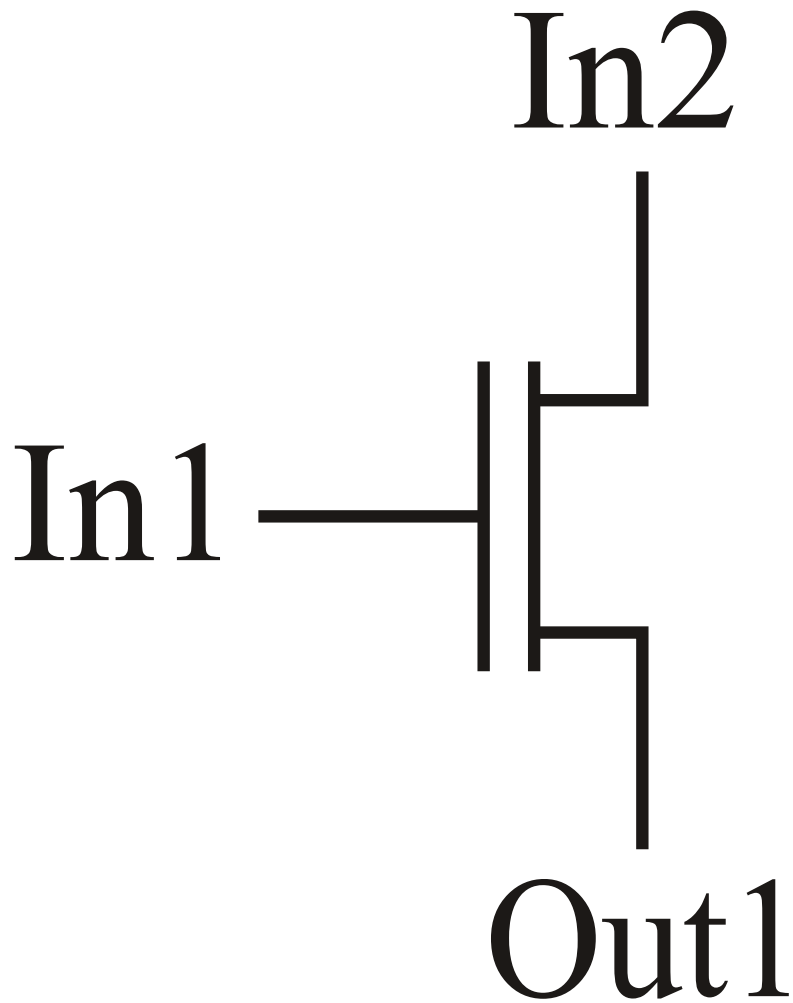




Block name: mite\_FG  
Number of inputs: 3  
Number of outputs: 1  
Parameter list: MITE\_current  
Block description: A MITE (Multiple-Input Translinear Element) block.  
MITE\_current controls the bias current.



Block name: nfet  
Number of inputs: 2  
Number of outputs: 1  
Parameter list: No.  
Block description: n-type MOSFET.



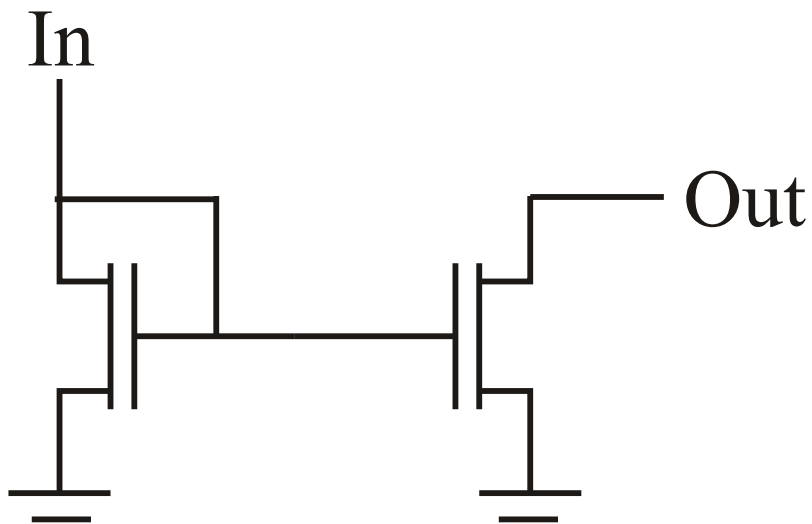
Block name: nmirror

Number of inputs: 1

Number of outputs: 1

Parameter list: none

Block description: An nmirror circuit element in CAB.



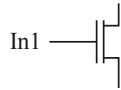
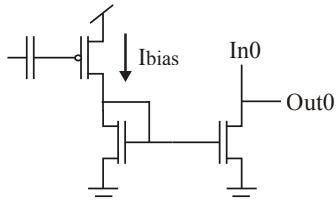
Block name: nmirror\_w\_bias

Number of inputs: 2

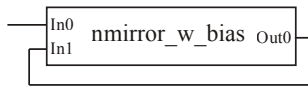
Number of outputs: 1

Parameter list: nmirror\_w\_bias\_ibias

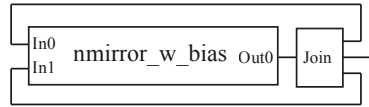
Block description: An nmirror circuit with a FG bias current. Ibias is nmirror\_w\_bias\_ibias, which has a default value of 50 nA.



When input is in use:



When output is in use:



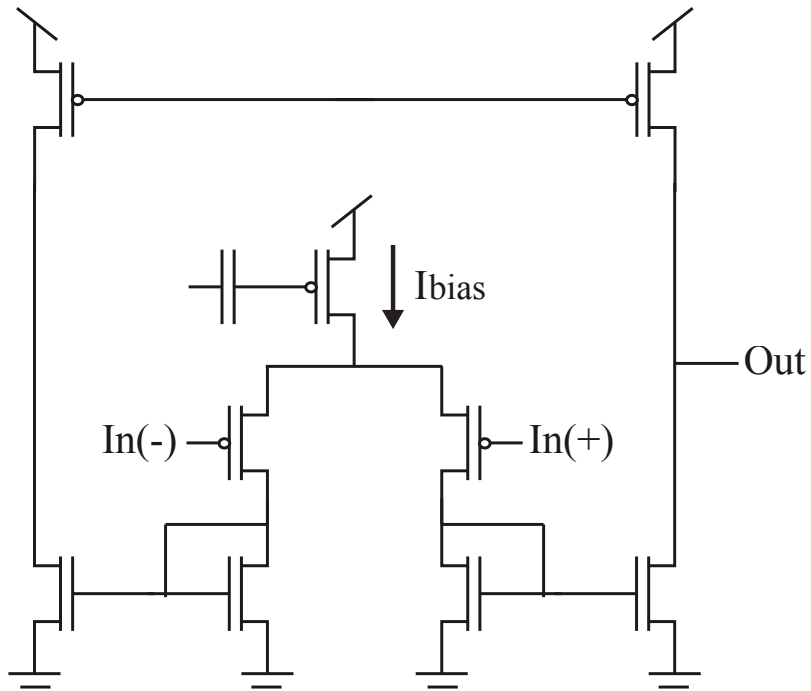
Block name: ota

Number of inputs: 2

Number of outputs: 1

Parameter list: ibias

Block description: A nine transistor OTA block, which is one analog element blocks. Ibias controls the bias current.



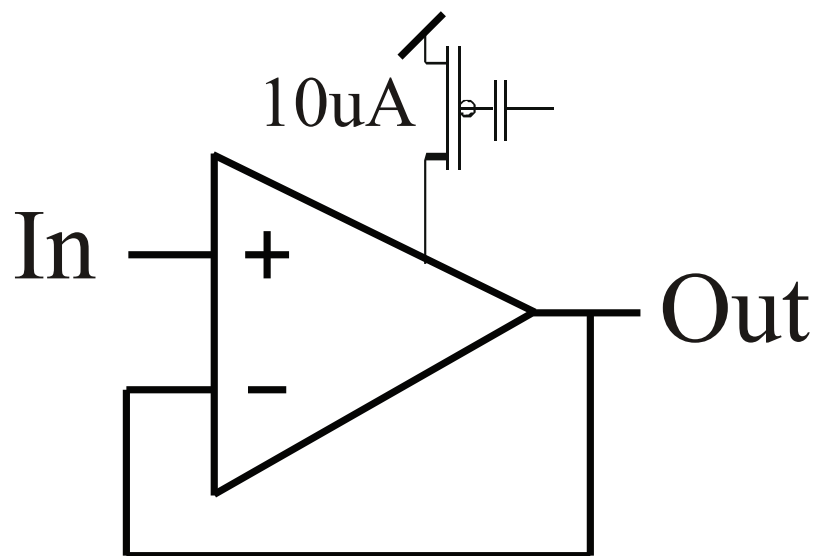
Block name: ota\_buf

Number of inputs: 1

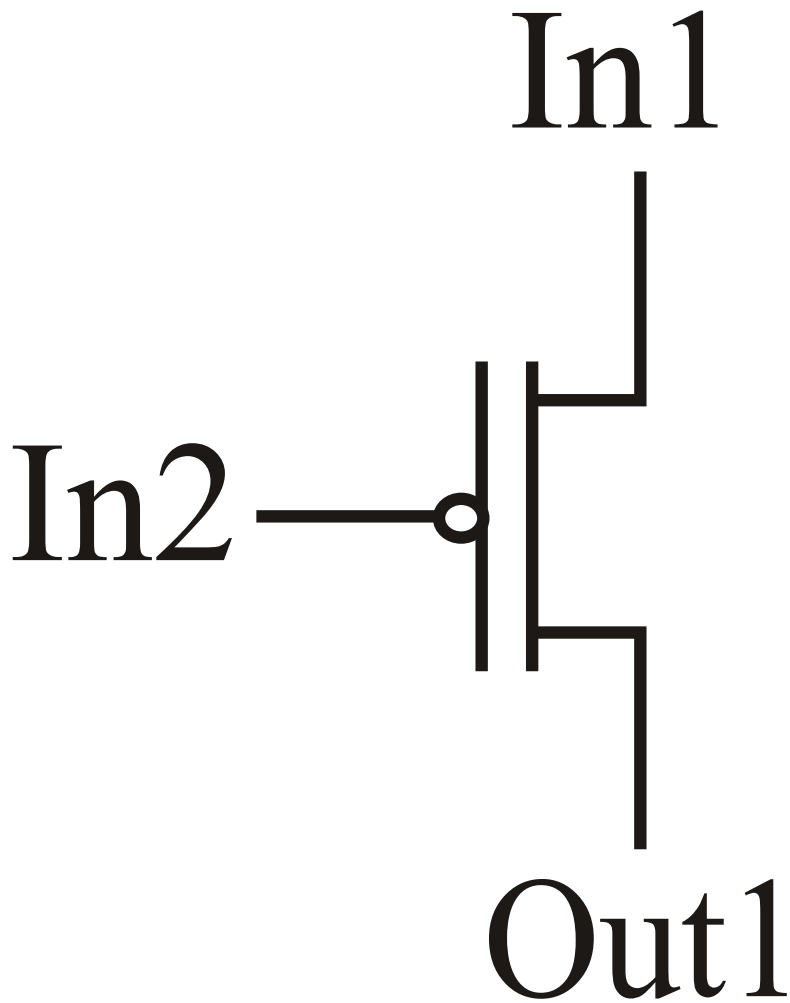
Number of outputs: 1

Parameter list: none

Block description: An analog buffer using an OTA. The bias current is set to  $10\mu\text{A}$ .



Block name: pfet  
Number of inputs: 2  
Number of outputs: 1  
Parameter list: no  
Block description: p-type MOSFET.



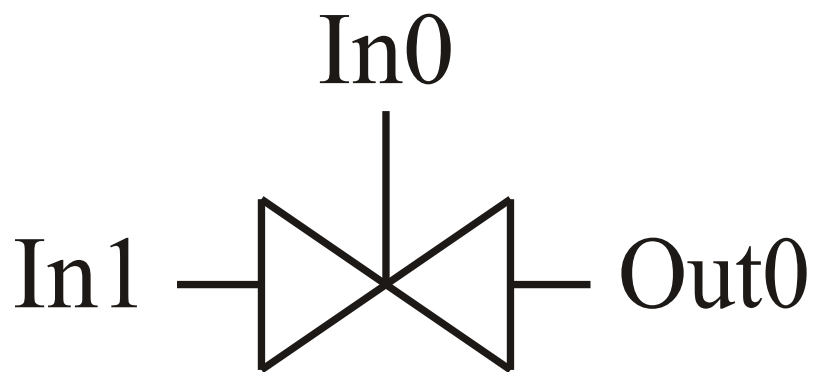
Block name: tgate

Number of inputs: 2

Number of outputs: 1

Parameter list: none

Block description: A T-gate element in CAB.





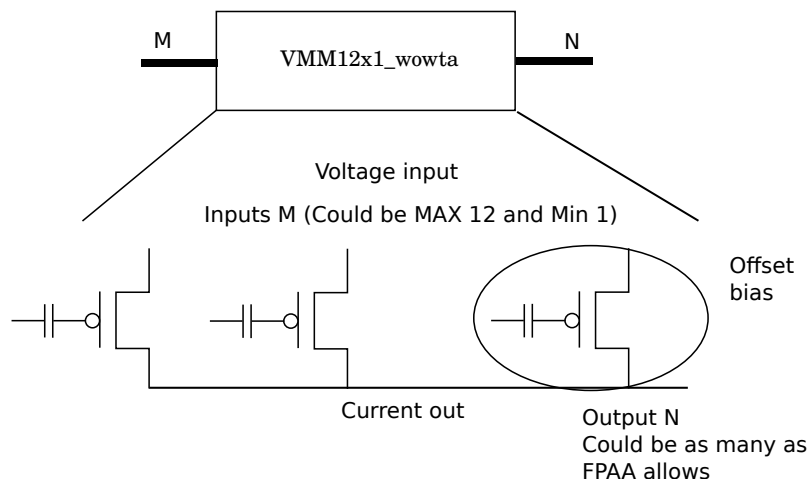
Block name: vmm12×1\_wowta

Number of inputs: 12

Number of outputs: 1

Parameter list: Input\_Dimensions, Weight\_Matrix, Offset\_bias

Block description: This is a Vector Matrix Multiplier circuit built using Floating Gate (FG) pFET transistors. There are 12 input FG pFET transistors and an offset FG transistor. Input\_Dimensions has row and column depending on inputs for your VMM one can have minimum of 1 input to maximum of 12 inputs. Output columns can be as many as allowed by FPAA. Each VMM block will sit in a different CAB. The inputs and outputs are vectorized.



Block name: wta\_new

Number of inputs: 3

Number of outputs: 1

Parameter list: number of blocks, wta\_new\_buf\_bias, wta\_new\_wta\_bias

Block description: A vectorized version of WTA circuit. Classic work on winner take all circuit (<https://papers.nips.cc/paper/151-winner-take-all-networks-of-on-complexity.pdf>) please read it before attempting to compile. This WTA has a FG pFET load (wta\_new\_wta\_bias) at the output. Its output is voltage and input is current (usually used with VMM12x1\_wowta). The output is buffered using ota in a follower configuration (wta\_new\_buf\_bias). The first input and the output are vectorized where as the second and third input are common.

