Hodgkin–Huxley Neuron and FPAA Dynamics

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***Abstract*—We present the experimental silicon results on the dynamics of a Hodgkin–Huxley neuron implemented on a reconfigurable platform. The circuit has been inspired by the similarity between biology and silicon, by modeling ion channels and their time constants. Another significant motivation behind this paper is to make the system available to circuit designers as well as users in the neuroscience community. The open-source tool infrastructure and a remote system ease the accessibility of our system to a number of users. We demonstrate the reproducibility of the results by replicating the dynamics across different boards along with responses from different inputs and with different parameters. The reconfigurability enables one to make use of a single primary design to obtain a variety of results. The measurements are taken from the system compiled on a field programmable analog array fabricated on a 350-nm process.**

***Index Terms*—Floating gates, field programmable analog array (FPAA), ion channels, neurons.**

I. Hodgkin–Huxley Neuron on a Reconfigurable Platform

THE pathway of neuromorphic computing [1] offers us a number of opportunities to build our applications and circuits and systems efficiently especially due to the analogy between biology and silicon. Our work aims to present the hardware results on the dynamics from a Hodgkin-Huxley (HH) neuron adapted from our original model [2] and implemented on a System on Chip (SoC) large-scale Field Programmable Analog Arrays (FPAA) fabricated on a 350 nm CMOS process [3].

Hodgkin and Huxley won the Nobel prize for their work [4] on eliciting a response from the nerve fiber of a squid axon. The action potential is generated as a result of a set of voltage-gated ion channels. This exponential distribution of carriers and their mechanisms of drift and diffusion of ions through a bi-lipid biological membrane are similar to the movement of charge through a transistor channel. Fig. 1 illustrates how our approach is inspired by this movement of charge through the biological membrane and further, in the reproducibility of the action potentials and accessibility to a wide set of users either remotely or through a local board.

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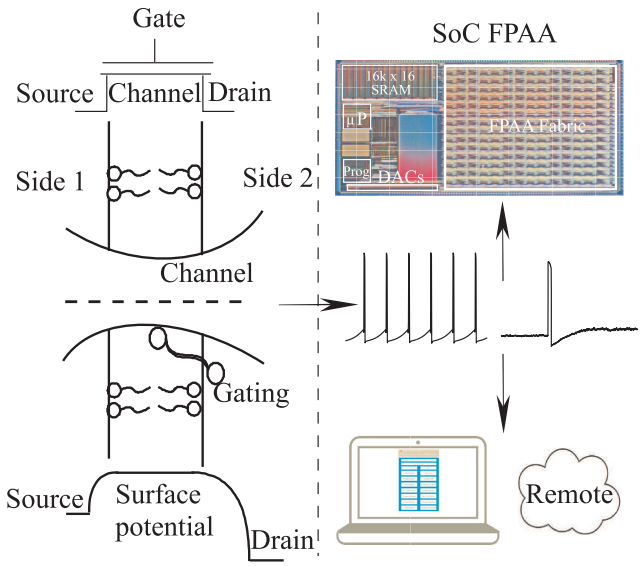

Fig. 1. High level idea behind the implementation of the Hodgkin–Huxley neuron on the FPAA. The similarity of a biological channel with a bi-lipid cell membrane to a MOSFET, shown on the left hand side, is one of the primary motivations behind the ion-channel based implementation. The band diagram has the surface potential which is analogous to the biological nernst potential of the ions. The hardware implementation of the HH neuron model on SoC FPAA, inspired by this concept, offers multiple opportunities. The reconfigurability helps to replicate a variety of action potentials through our open toolset and thereby offering greater insights to a few concepts in neuroscience through experimental results from the hardware.

This work reproduces the spiking behavior and shows the non-linearity of dynamics of HH neuron by modeling voltages, ion channels and time constants. We show a model which is not only inspired by the physical similarity between ion channels and semiconductors but one which also helps to clarify a few concepts on ion-channels and neurons, as shown in Fig. 1. Rather than just simulating and understanding from the equations, anyone can use and reproduce similar results using our open-source tool infrastructure and remote system [5] [6]. One can study and analyze the system behavior by observing the effect of tuning the ion channel parameters with ease due to a reconfigurable chip which helps the user to get a better insight into the causality behind the dynamics. Hence, we demonstrate a system from the perspective of the user in this paper.

A software simulation is done by modeling a set of equations which has more than twenty parameters [4] to tune to obtain the right behaviour. However, in our system we mainly have three bias parameters to tune the time constants for spiking, while the other parameters like E_{Na} and E_K, the supplies to the circuit are constant and global, thereby reducing the whole parameter set to obtain a spiking behaviour. Also, the bio-

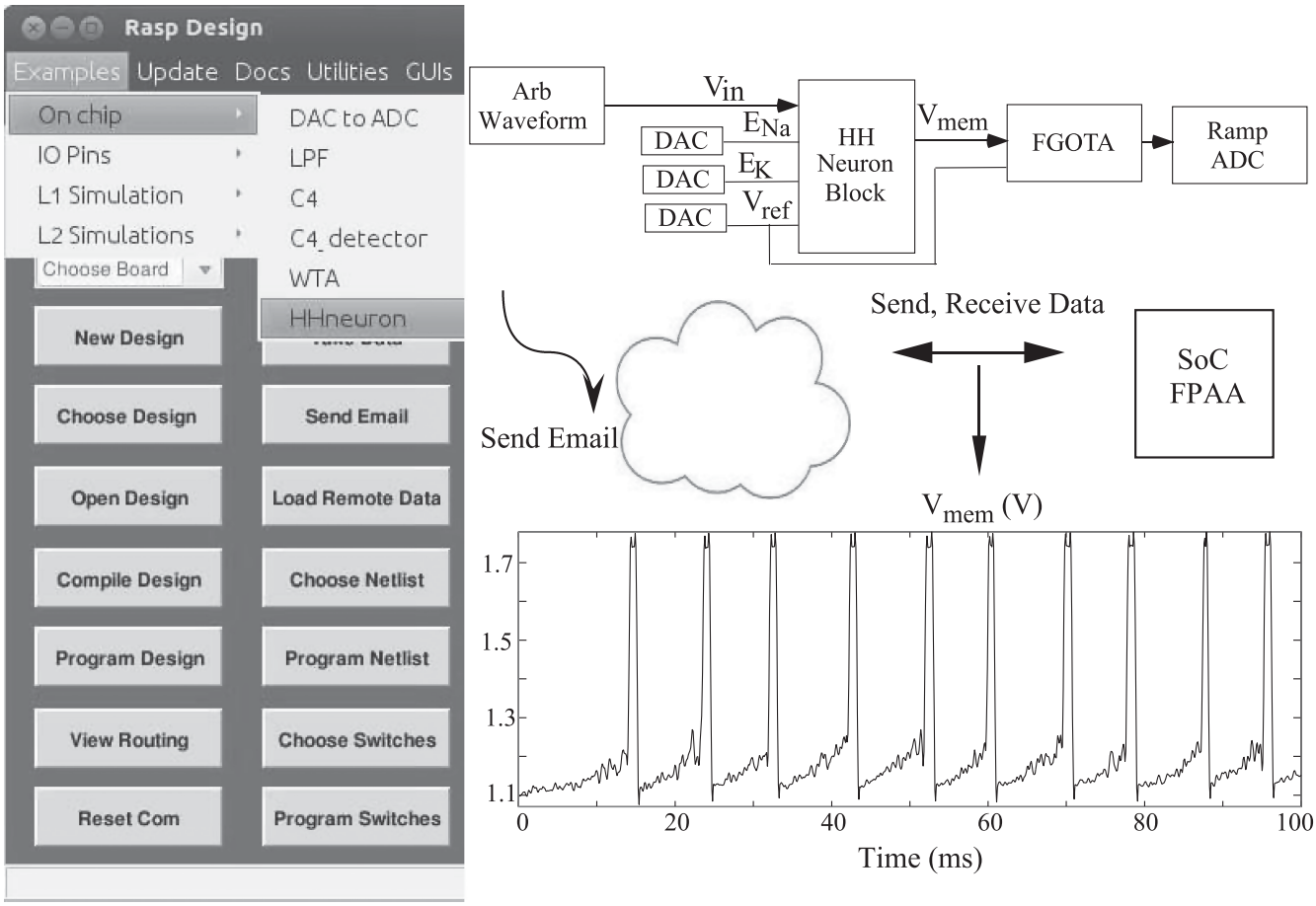

Fig. 2. Graphical user interface from which the HH neuron design can be viewed from the examples drop-down, in the open-source tool infrastructure is shown. The FGOTA and the ramp ADC constitute the measurements setup, to amplify the membrane voltage signal and observe the spiking behavior from the neuron clearly. The example can be compiled and data can be measured by sending the email and remotely receiving the result from the FPAA to observe various dynamics. One such set of behavior is zoomed out for the clarity of the reader and shown for the membrane voltage output from the neuron.

physical behaviour is emulated in hardware since we are modeling the ion channels without just curve fitting and translating the mathematical equations to hardware. Unlike an ASIC, the reconfigurable nature allows us to obtain a multitude of dynamics for the HH neuron and we are able to use the same chip to scale up as well as implement the functionality of neuron models as well. The low cost and flexibility as well the non-requirement of waiting for the chip to come after fabrication every time helps us in rapid prototyping, while the remote system enables the user to obtain the relevant dynamics from the neuron as it is available in the examples in the tools as shown in Fig. 2. It can be replicated by others in the community too with the inner details having been abstracted away for the ease of the user, while at the same time, offering the flexibility of access to an advanced user too.

This paper elaborates on the modeling of the HH neuron and implementation of the circuit and the varying spiking dynamics observed through the experimental measurements obtained from the FPAA. Section II introduces the translation of our original model to the FPAA with all its constraints and opportunities. We first observe the action potentials in Section III. Section IV describes the similarity between a biological channel and transistor channel. We discuss the criticality to get the correct biasing points in Section V and further discuss the physics behind the ion channels in Section VI. Section VII gives a deeper insight into different spiking dynamics across chips while Section VIII concludes the discussion.

II. Implementation on the FPAA

Reconfigurability and programmability [7] aid in achieving a number of objectives, which are advantageous in our work to observe a multitude of dynamics using a minimum number of elements. The FPAA SoC [3] consists of Computational Logic Blocks (CLBs) and Computational Analog blocks (CABs) which are primarily used here to model the behavior integrated with a processor and other peripherals. The transistor channel models are modified from the circuit [2] utilizing the current FPAA resources using nFETs, pFETs, Operational transconductance amplifiers (OTAs) and Floating-Gate (FG) OTAs such that the circuit is integrated in one CAB, thereby occupying less than 1 percent of the IC. The current chips fabricated in a 350 nm CMOS process on which the measurements have been taken consist of 98 CABs.

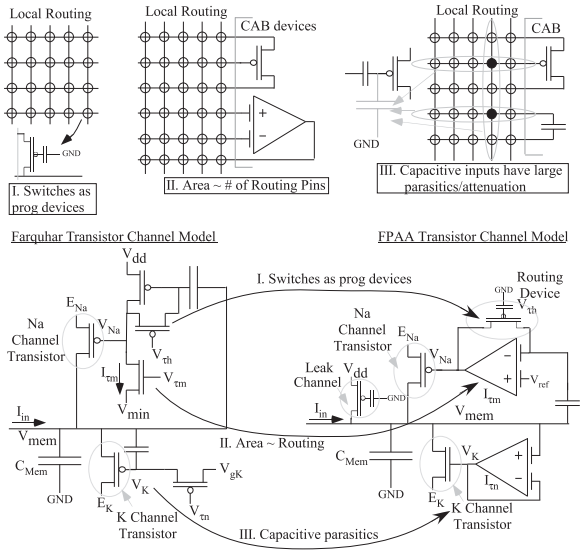

Fig. 3. Translation from the original structure to the one on the FPAA constrained in one CAB. The switches in the routing as depicted are not deadweight but those FG-pFETs are used as programmable switch elements for computation. With the current structure on FPAA, a transistor or an OTA corresponds to a 3 terminal device, thereby an extra area is not a concern since it is decided by the number of routing pins. Keeping this in mind, the Na^+ and K^+ channel are converted on our FPAA as shown.

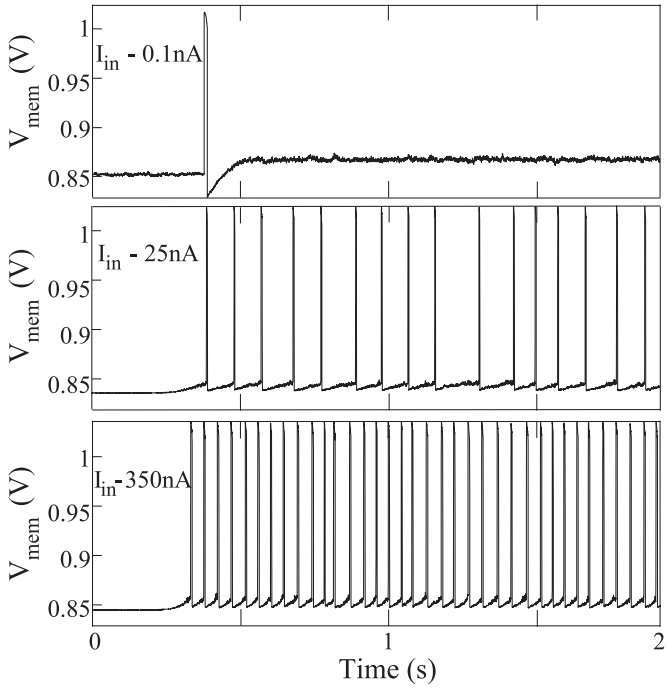

Fig. 4. Different spiking rates and change in the inter-spike interval for a set of conditions and parameters, over a longer period of time. The effective input current is varied, thereby changing the total current contributed at the membrane voltage node. The behavior of V_{mem} changes from one spike to multiple spikes with different rates.

Hodgkin-Huxley performed voltage clamp experiments, where a step voltage was given and the current measurements were taken from the ion channel. This data helped to derive the types of channels responsible for the dynamics and equate and formulate a model. From their data [4], it is seen that the spike is observed due to the interaction between primarily the sodium, Na^+ and potassium, K^+ channel. Their nernst potentials, given by E_{Na} and E_K are translated to voltages here, which are in terms of U_T, the thermal voltages, and serve as supplies to the neuron circuit. The gating dynamics to produce V_{Na} and V_K for the respective channels are built from the FPAA resources, where a pFET and nFET model the Na^+ and K^+ channel respectively, operated in the sub-threshold regime.

The Na^+ channel is responsible for the rising and falling phase of the action potential due to its activating and inactivating mechanism. The step response of the Na^+ channel from the original data [4] shows that it has the characteristics of a band-pass filter. Its time constants are defined to be τ_m and τ_h. While, the K^+ channel is responsible for returning the depolarized state of the neuron to its resting potential and its time constant is defined to be τ_n.

Our classical circuit [2] had a Na^+ and K^+ channel as a band pass and high pass filter respectively. The K gating, with respect to how much it turned on was quantitatively described by the 'n' activation factor while the 'm' activation and 'h' inactivation factors determined the Na gating time constants. However with the FPAA, due to the significant capacitance in the routing, the FPAA gain from V_K to V_{mem} is reduced, whereas the original structure [2] needs a higher gain especially around higher frequencies. This inspired us to modify the design, for the K^+ channel to be a low-pass filter, whose output to the K gating nFET is represented by V_K. An FGOTA in a follower configuration is used for this purpose since the FGs help to set the DC offsets, while tuning the bias current at the right place would produce the desired τ_n.

The Na^+ channel's output to the Na gating pFET is represented by V_{Na}. The Na channel, a band-pass filter can be considered to be a modified Capacitively Coupled Current Conveyer, C^4 filter [3]. An FG-pFET is used in the feedback to set the τ_h constant. No extra device is required for this purpose, since the feedback is a part of the local routing without occupying an extra area.

Fig. 3 demonstrates the concept behind the above implementation on the FPAA. The role of the local routing, as shown through the input and output lines to the CAB devices is focused on in Fig. 3. The switches in the routing, the FG-pFETs are used as programmable switch elements for computation [7]. The routing tracks dominate the area and one transistor is similar in area to one OTA, both being three terminal devices, inspiring to transform the design of the channel gating dynamics modeled by the transistors to OTAs. Hence, a primarily transistor based Na^+ channel converts to an FGOTA and an FG-pFET switch on the routing based device on the FPAA. Due to the routing parasitic capacitive inputs contributing to a large attenuation, the high-pass K^+ channel translates to a low-pass structure with the desired gain on our device.

III. Action Potential

Fig. 4 shows the spiking behavior on V_{mem} in response to a step input current. The effective input current to the cell is used as a primary parameter to study this behavior [8]. We can see

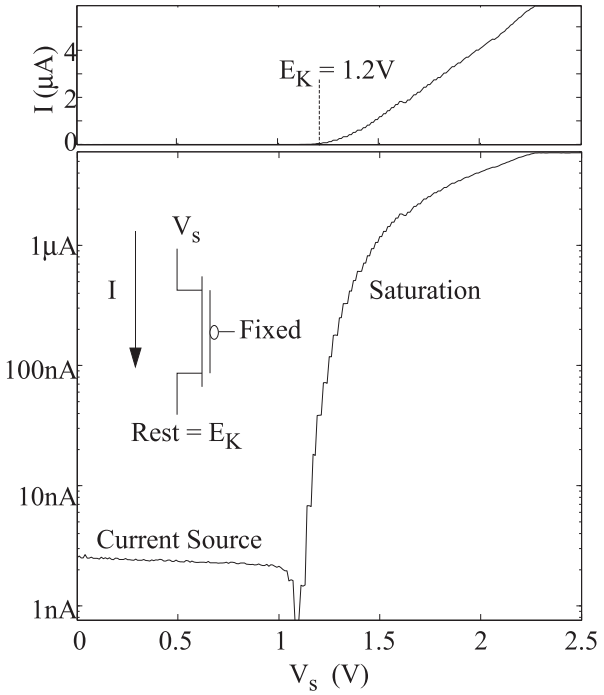

Fig. 5. PFET is modeled as a prototype for a biological channel. Current as a function of the source voltage is shown in absolute as well as log scale. The gating potential is fixed at 0.1 V, while E_K is biased to 1.2 V, through which we can identify the dual behavior of the terminal as a source and drain.

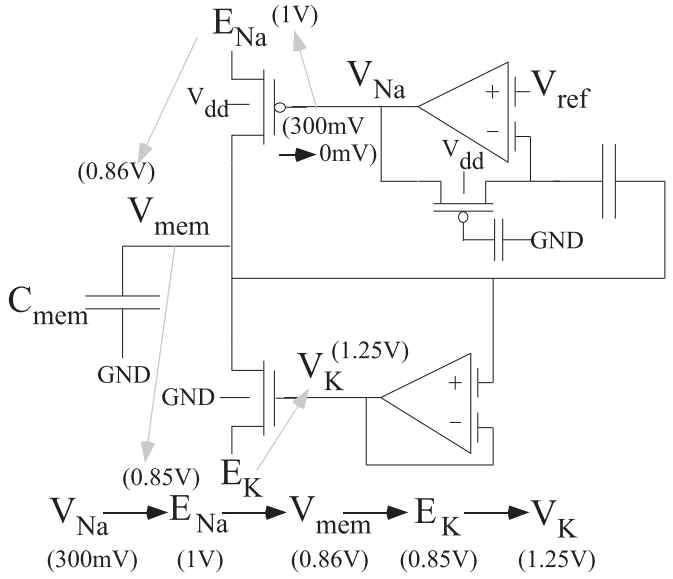

Fig. 6. Bias levels are important for the circuit since they determine the dynamics of the action potential, such that it is between E_K and E_{Na}. Further, the FGOTAs' bias currents help to set the time constants of the K^+ low pass filter and the Na^+ band pass behavior. The arrows indicate the sequence followed to arrive at the various DC levels, starting from V_{Na}.

that the inter spike interval (ISI) decreases and the number of spikes in a specific period of time increases as the input current increases across the plots [9]. A phasic spiking is observed [10] initially for a lower current, where a single spike is observed and V_{mem} rests at its resting voltage. Continuous spiking patterns are observed as the current changes. The average firing rate is consistent but the thermal noise contributed by the transistors in the model as well as from the measurement and instrumentation circuitry causes changes to the ISIs in the spiking pattern over time.

IV. Passive Channel

A pFET is modeled as the prototype for a passive ion channel, which selectively allows ions to cross the membrane. The flow of ions due to the difference in the concentration in the intracellular and extracellular space [11] and the channel formation is similar to the energy band diagram as observed with a silicon channel model. A single transistor modeled as a biological passive channel aids us to decide the regions of operation of the circuit elements, thereby initiating the process to figure out the parameters to bias the system. The I-V relationship [12] shown in Fig. 5 where we measure the pFET as a passive channel helps us to take a systematic approach.

Fixing the gating potential of the pFET and the drain voltage at E_K, the current flowing through the transistor is observed as the source voltage is swept. It can be seen from the current though the pFET vs Source voltage plot in Fig. 5 that the terminal behaves as a source and a drain node when it acts as a current source and when the transistor is in saturation respectively. There is a constant current when the sweeping voltage is less than E_K, while it exhibits a source behavior as the source voltage crosses the resting potential of E_K. This can be observed in an activating excitatory synapse when the FG-pFET's source is at E_{Ca} which is $4U_T$ [11] while its drain is at the membrane voltage at a resting potential of $-2.5U_T$ and for a peak at the gate. The concept of passive channel is relevant in the case of modeling of dendrites too [13] where the saturation region is exploited.

V. Biasing the Neuron

The complementary relationship between the voltage and current from a pFET modeled as a biological channel, plays a significant role in determining the bias points for the various nodes, giving an insight into the design. The current measurements' results from a step voltage input through the voltage clamp experiments helped to determine the gate voltage needed to produce the desired response from the ion channels, which in turn, is the starting point of the biasing of the neuron. Fig. 6 shows the concept behind the sequence in figuring out the biases required to obtain action potentials from the neuron.

The gain from the Na^+ gating channel output, to the membrane voltage is known to be around 8. Thus, the DC of V_{Na} can be fixed to be around 250-300 mV, thereby setting the source and drain DC voltages for the feedback FG-pFET and programming a large current for the feedback element. For the Na gating channel pFET to be in saturation, knowing V_{Na} and the current through the pFET in saturation in the order of nAs, we can set E_{Na} to be at 1V. This sets E_K since the difference between E_K and E_{Na} is around 150 mV. From the Nernst potential [11], we know E_K is $-3U_T$, while E_{Na} is $2U_T$. The resting potential for membrane voltage is 10 mV above E_K. From E_K and the

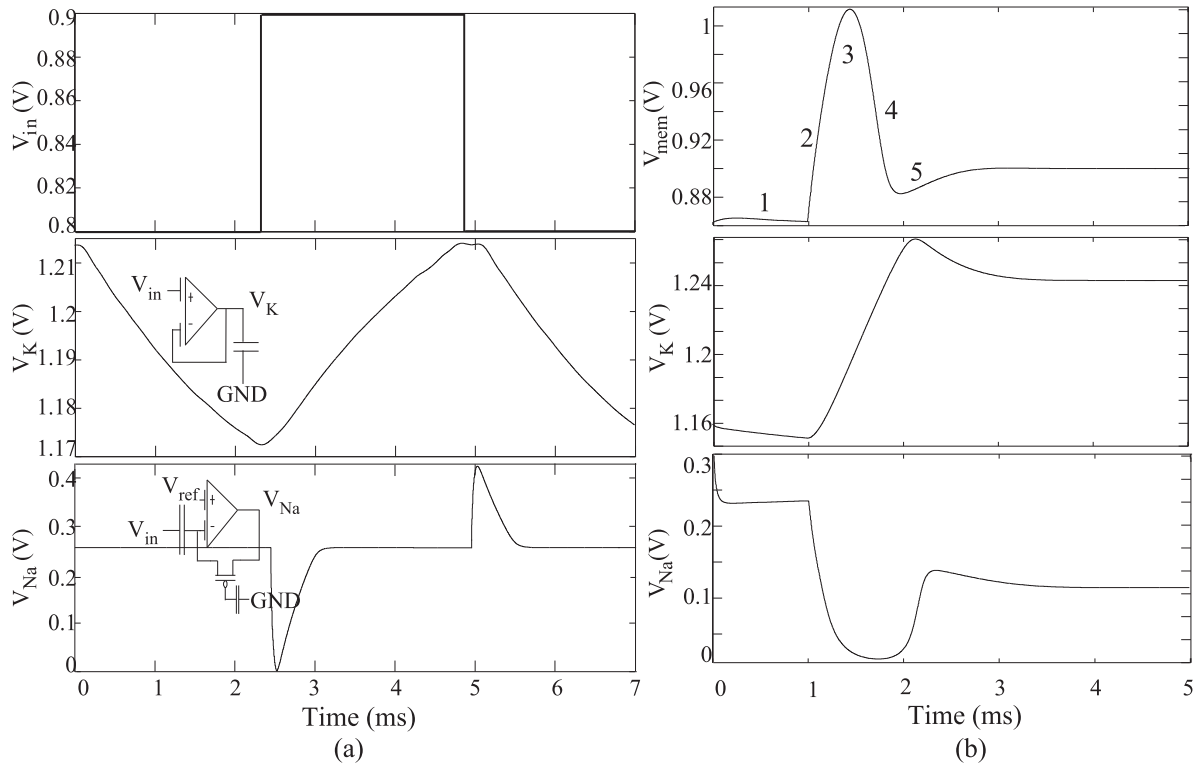

Fig. 7. (a) K^+ and Na^+ gating circuit and the experimental results for the step response of the channels are shown. A step input of 100 mV is applied. The transient response of the K^+ and Na^+ channel depicts the low-pass and bandpass filter behavior respectively. The low pass effect is responsible for bringing the action potential back to the resting potential. A DC level of 1.2 V is achieved by tuning the offset currents in the FGOTA and the time constant can be tuned by I_{τ_n}, the current to which the FGOTA is biased. The DC level of the Na^+ channel is observed at around 300mV. The feedback time constant is controlled by the FG-pFET switch in the routing. (b) Device level simulation results for an action potential to a step input of 100 mV are shown. V_{mem}, V_K and V_{Na} are observed on one plot in response to a step input for a set of biases.

current through the K gating nFET, we can determine V_K to have a DC of around 1.25 V. From these DC biases' points, we can determine how to tune the FG OTAs and the conductances to generate a spike. The biasing on the Na^+ is critical in terms of getting the DC values, time constants and the gain right, since that sets the rest of the biasing and time constants. A gain of -8 or -12 dB between V_{mem} and V_{Na} is required for it to spike, so that one does not see just an oscillatory response. The corners of the bandpass filter are not quite wide and their frequencies are tuned such that there is a factor of two to four between the two bands. It is important to make sure that the feed forward time constant due to the forward FGOTA, τ_m is faster than the feedback time constant, τ_h, caused by the output to the middle capacitively coupled node. The DC level affects the corner frequency of the amplifier, since it is giving the DC point of the FG-pFET device that is creating the feedback. Considering the channel transistors to be in saturation with the Na^+ channel pFET's current being 1 percent of the K^+ channel nFET, the resting potential of V_{mem} sits at E_K. A leak channel that represents the ion channels for chloride and other ions [4] , modeled by an FG switch in the routing is added to pull up the V_{mem} to $U_T/2 + E_K$, as the V_{mem} is at the transition point between the linear and non-linear conductance regions. The time constants are set such that τ_n is slower than τ_m biologically similar to the fact that K^+ channels respond slower than the Na^+ channels.

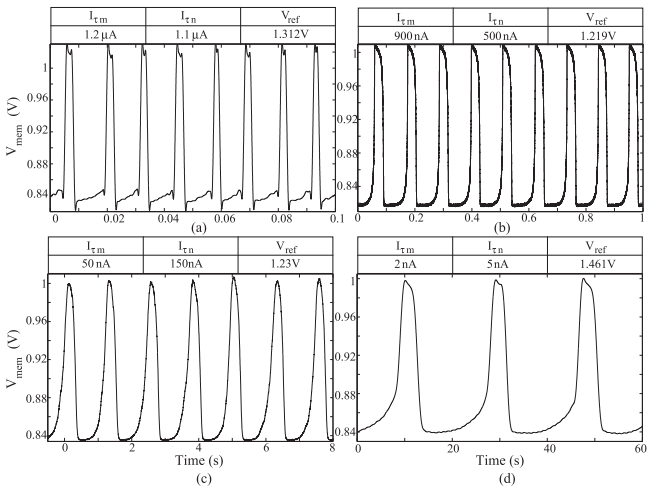

Fig. 8. The experimental measurements' data from the FPAA for an action potential to a step input of 100 mV, exhibiting different spiking frequencies. The biases are controlled such that different rates can be obtained, scaling the I_{τ_m}, I_{τ_n} and V_{ref} accordingly depending on the rate desired. As observed from the time scale, the spiking frequencies reduce with the progression of the plot from (a) to (d).

VI. Physics of Sodium and Potassium Channel

Fig. 7 illustrates the Na^+ and K^+ channel behavior clearly. The interaction of the currents from the Na^+ and K^+ produce

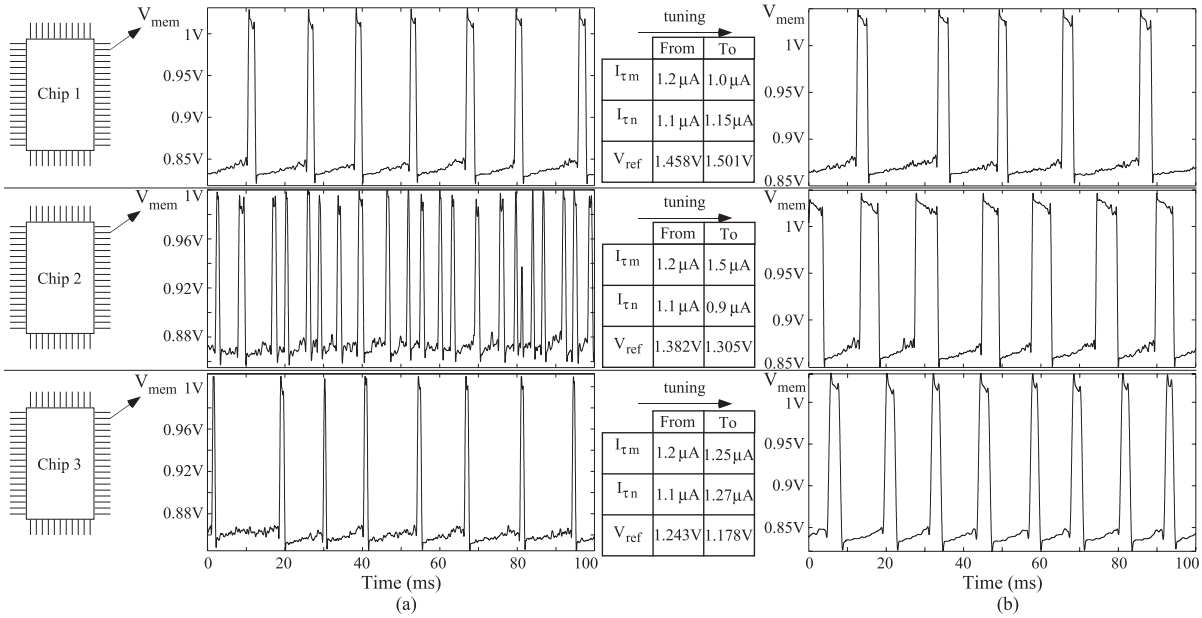

Fig. 9. Experimental measurements' data from the FPAA for an action potential to a step input of 100 mV, from different boards. (a) Results before tuning for mismatch. (b) Measurements after tuning. The biases are controlled such that the DC biases match along with the different frequencies and rates from the different chips. The threshold voltage mismatches are compensated and adjusting I_{τ_m}, I_{τ_n} and V_{ref} aids in adjusting the respective time constants.

the action potential. A step input current is injected into the node through an OTA or an FG-pFET which models a synapse. The capacitance from the line acts as the membrane capacitance, C_{mem}. Fig. 7(a) shows the responses of the Na^+ and K^+ channel individually extending on the concept of the voltage clamp experiment, where the ionic currents were observed [4] after selectively blocking the respective ion channels. Activating one channel at a time in the system, the bias parameters were calculated through simulation [12] and from the experimental results on hardware. They were figured out such that we get a bandpass response for the Na^+ channel while the K^+ channel gives a low pass response. The transient responses to a step input in the Fig. 7(a) give insights into the separation of the time constants τ_m, τ_h and τ_n of the ion channels. From the calculations shown in Fig. 6, we get similar DC points by adjusting the offsets through the FGOTAs.

Fig. 7(b) shows a single spike and the different regions of the action potential are labeled in the figure. The membrane voltage, initially starts at its resting voltage, about 10 mV above E_K at 1. The region 2 of depolarisation where the Na^+ ions flow in is represented here when the Na^+ gets activated and the positive feedback through the FG-pFET kicks in and as V_{Na} drops, V_{mem} rises to E_{Na}. At 3, the K^+ channel starts to affect the response and the feedback time constant, τ_h starts recovering. The Na^+ channel sees the input to it decreasing, causing V_{Na} to rise and settle to its DC of 300mV and τ_h pulls V_{mem} to its equilibrium at 4. At 5, the K^+ and Na^+ shut off, and we see the rise in V_{mem} as the node charges through C_{mem} and the refractory period is a factor of the input current integrating through the capacitor at the node. This spiking behavior observed is biologically similar to the ion channel behavior with the Na^+ and K^+ channel conductances changing with time due to the opening and closing of the respective ion channels and causing the depolarisation and hyperpolarisation in the membrane voltage.

Observing the results from the transitions of V_K and V_{Na} with respect to V_{mem}, we can further understand the close coupling between the non-linear dynamics of the ion channels which contributes to give rise to an action potential in Fig. 6(b) through circuit level simulations [12]. As the voltage on V_{mem} starts rising from its resting voltage to its peak, there is a fall in V_{Na}, with V_K peaking as expected, with the rise and fall governed by the time constants. The rise during the refractory period is controlled by C_{mem}.

VII. Looking into Different Spiking Dynamics

We explore different dynamics in this section, analyzing the effect of modifying time constants to achieve different firing rates. The tuning for mismatch is also studied to obtain similar dynamics across chips [14] along with subjecting the system to other signals like a ramp input and noise.

A. Effect of Modifying Time Constants

Fig. 8 shows a multiplication in the frequency of the spikes as the plots progress from (d) to (a). This adaptation in the spiking frequency is due to the change in time constants τ_m, τ_n and τ_h which is changed by tuning the bias currents I_{τ_m} and I_{τ_n} and V_{ref}. As they change, the time taken by the Na^+ and K^+ channel to respond to changes in V_{mem} varies, leading to a higher frequency in spiking.

I_{τ_m} and V_{ref} change the corners of the bandpass filter responsible for the Na^+ channel while I_{τ_n} adjusts the corner of the K^+ channel. We show how we can run our circuit at different time scales in Fig. 8. Our tools allow one to use a single Xcos

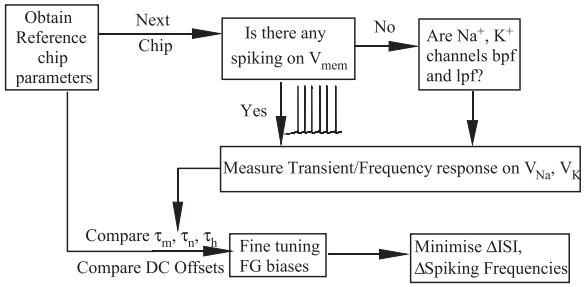

Fig. 10. Tuning algorithm to minimise the variation between different chips to get similar spiking responses across boards is shown by analysing V_{Na}, V_K and then fine tuning the FG biases on the CAB elements of the neuron model.

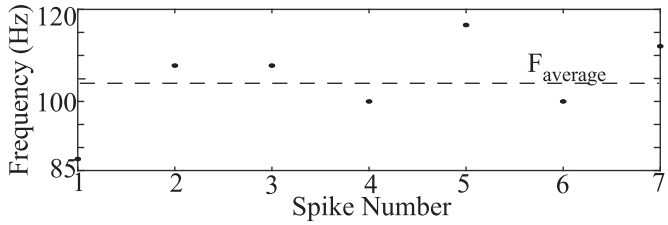

Fig. 11. Spiking frequency for a chip represented as filled circles is plotted as time progresses. It is defined as the reciprocal of ISI here. It is not a constant due to the thermal noise of the transistors in the system. The average value across time is calculated, marked as a dotted line, to compute the spiking frequency of each chip, which is used to quantitatively correlate the behavior between the chips.

design and a fine-tuning of the parameters enables running at a slower, faster or at the real time speed.

B. Across Chips Calibrating for Mismatch

Mismatch in the responses between different chips or among different neurons has been exploited to use them beneficially in some applications [15]–[18]. The intra-neuron mismatch due to the variation from CAB to CAB is lesser than chip-to-chip one as expected, since the die to die variations are higher than on die variation [19]. A classic neuromorphic problem is studied here to identify if this spiking behavior is reproducible and experimental measurements were taken across three different chips. We try to minimize this mismatch since we wish to efficiently use as many neurons as possible for computation, without using extra resources to correct for the added variation [20]. The results with the same identical set of parameters are shown in Fig. 9(a). The threshold voltage mismatch caused due to the indirect FG programming infrastructure can either be compensated by using the systematic automated mismatch map approach [21] in our system or other techniques as shown in [22], with translation of parameters in a network [23]. [24], [25] have explored different optimization algorithms to arrive at the parameter space set for the tuning the neuron model [26]. The parameters are tuned here at the neuron level by looking at the varying time constants specific to this circuit since our platform allows one to shift biases.

Fig. 10 shows the tuning methodology for mismatch minimization between the chips. We first start with obtaining the spiking response from a reference board by programming the biases and time constants of each of the channels as elaborated in Section V. Once the reference parameters are obtained, these are used for compiling down the design to the respective chips. An Xcos block for debugging has been created in the library of blocks with the pins instrumented out to measure V_{Na} as well as V_K in addition to V_{mem}. With the reference parameters, a check is done to observe if there is any spiking activity or not. If there are no spikes, we do a sanity check if the Na^+ and K^+ channel behave as band-pass and low-pass filters respectively.

After observing the spiking behaviour on V_{mem}, we calculate the variation in the ISIs or spiking frequency to minimize its difference from the parameter chip. A sample average spiking frequency is shown in Fig. 11. The transient or the frequency response from V_{Na} and V_K helps us to calculate the respective time constants τ_m, τ_h and τ_n. The FG biases on I_{τ_m}, V_{ref} and I_{τ_n} are then fine-tuned. To get equivalent spiking amplitudes between the chips, E_{Na} and E_K which are the supplies given through DACs on the respective chips are calibrated as well as the DC offsets are equalised through fine tuning of the FG biases on the FG OTAs of the Na^+ and K^+ channel.

Fig. 9 shows how the rates and frequencies are thus matched across the chips thereby giving an identical behavior among all the three chips. This proves our hypothesis that the dynamics are repeatable and reproducible among the different boards too, due to the programmability offered by the FG devices in the FPAA. We have defined different metrics like variations in ISI, spiking frequencies to correlate the performance across chips in Fig. 12.

C. Effects of Ramp and Noise Inputs

Subjecting the circuit to different ramp and noisy inputs, we see different dynamics as seen in Fig. 13. When a ramp signal is applied at the input, there is an initial delay in the spiking which is proportional to the time for which the ramp is active before it settles to a steady value. Fig. 13(b) also shows after the first four spikes, the inter-spike interval changes due to the delay and then we observe a continuous spiking.

A random noise generated input is given to the system, to explore the effect of noise [27]–[29] since it is an inherent property of a biological system [30]. The resulting V_{mem} spikes even with a noisy signal. The system is edge-triggered rather than level triggered since an action potential is observed even at an input level lower than the 'threshold' value. In these cases, V_{mem} is primarily influenced by changes on V_{Na} since a positive feedback loop is created between V_{Na} and V_{mem}. The bandpass filter for the Na^+ channel gating destabilizes the circuit since the loop gain is higher than one. The 'h' variable is significant in the dynamics, in the downward transition where the feedback is out of band. The positive feedback is again analogous to that caused due to the increase in g_{Na} with more influx of the Na^+ ions.

VIII. Summary and Discussion of the Neuron Structure

FPAA offers reconfigurabilty and programmability, which enables rapid prototyping in hardware. It is useful for scaling

CORRELATION MEASURES ACROSS CHIPS

Metrics	Before Tuning			After Tuning		
Chip Number	Chip 1	Chip 2	Chip 3	Chip 1	Chip 2	Chip 3
ISI (ms)	12.14	4.07	12.45	15.71	10.08	9.61
Spiking Frequency	82.37	245.7	80.32	63.65	99.2	104.1

Fig. 12. Table shows metrics like ISI and spiking frequency, to demonstrate numbers to quantitatively compare the behaviors before and after tuning for mismatch.

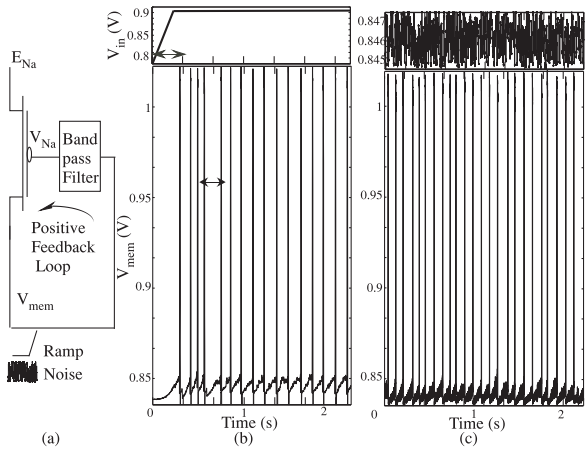

Fig. 13. Response of the membrane voltage to a different set of inputs over a longer period of time. (a) Positive feedback loop from V_{Na} to V_{mem} destabilizes the system thereby affecting the overall dynamics of the system. The 'h' variable plays a significant role here. (b) Initial delay in V_{mem} is seen corresponding to the application of the ramp input and it continues spiking. (c) With a baseline of 0.84 V and considering a "threshold" of 0.85 V, a Gaussian noisy input generated through a random noise generator, shows that it continues spiking with higher noise levels as soon as it sees a rise in the input signal.

up and building large-scale networks and systems for real time applications unlike just simulations in software which do not give real time responses and may have a reduced speed. The parallel execution nature and the fact that each neuron occupies only one CAB element on the SOC makes it a useful platform. The circuit also consumes a power of 0.79 μW due to the devices being operated in subthreshold regime. When one thinks of expanding to build larger networks for real-time applications, the neurons and synapses built from CABs and routing elements are used for computation.

Through this paper, we attempt to bridge the gap between users in the hardware and computational community [31] especially by providing reusable neuron blocks [32] on a mixed-signal platform. One just needs to pull out the design Xcos structure from our openly available tool infrastructure, compile and get the results back from silicon through a remote system. Moreover, a simulation engine in the toolset also enables users to model and simulate the system and compare their results from the FPAA SoC, hence letting the users to compute and understand while looking at the hardware results.

A fundamental implementation of silicon neuron circuit [33] was shown building from the classic HH equations. There have been other approaches [26], [34]–[36] that have been adapted from this classic implementation, translating from the equations to hardware while we also see a voltage-dependent ion channel based modeling [37]. A comprehensive set of different circuit models and solutions to build neurons on silicon has been discussed in [38].

Comparing our implementation to one in a digital setting, as has been shown in FPGAs [39]–[42], we can turn to a reduced neuron model, computationally a digital concept [43] where the number of state variables is reduced to mostly two. This is due to the ease with which a two state variable can be studied for its non-linear dynamics and one can observe the phase plane behavior [9] to observe different bifurcations depending on the chosen parameter.

In the circuit described in this work, the four state variables can be brought down to two, by tuning the Na^+ channel, where τ_m moves to 0, τ_h tends to infinity, thereby making the Na channel just an amplifier with a finite gain. The concept of multiply-accumulates (MAC) [44], a standard operation which adds a product of two numbers to an accumulator, especially used in digital computing to compare the performance of digital signal processors, helps to throw light on the efficiency of the neuron models. The Integrate and Fire neuron [45] can be built from this, with the same number of devices, though with lower number of parameters, with 1-4 MACs optimized for a digital implementation, while the models like Izhikevich [10] and FitzHughNagumo model involve 30-60 MAC per sample as they are a two state variable system. However, they may not accurately represent the behavior of neurons like the HHneuron model which emulates the ion channel dynamics. While the HHneuron model may involve a larger number of Ordinary Differential Equations (ODEs), with numbers in the range of 1000 MAC per computational iteration for a digital implementation, it can be implemented in our analog formulation with a few devices and parameters unlike the full parameter set used in the HH equations, thereby reducing redundancy and the bias parameters are directly relatable to observable time constants in the dynamics.

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