Implementation of Synapses with Hodgkin Huxley Neurons on the FPAA

Aishwarya Natarajan, Jennifer Hasler
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, Georgia
E-mail: anatarajan35@gatech.edu, jennifer.hasler@ece.gatech.edu

***Abstract*—The neuronal responses through excitatory and inhibitory synapses are implemented on a reconfigurable and programmable platform. The synaptic cleft between the pre synaptic and post synaptic neuron has been depicted as a ramp generator while the post synaptic potentials are observed from the transistor channel neuron model which emulates the ion channels in biological neurons. The synaptic strengths are tuned by modulating the charge on the floating gate devices on the hardware demonstrated through particular voltage levels and time constants. The models have been designed and built in such a way that the tools associated with the chip make it possible to build up and compile a bigger network of neurons and synapses. The experimental measurements are taken from the circuits compiled on a Field Programmable Analog Array fabricated on a 350nm process.**

***Index Terms*—FPAA, Neurons, Floating gates, Excitatory, Inhibitory, Synapses, PSP**

I. Macromodeling a neuron with synapses on a reconfigurable platform

The foundation of building bio-inspired systems for real time applications is the design of efficient neuronal and synaptic blocks. Synapses enable the neurons to communicate with each other and allow one to implement algorithms to exploit the action potentials from neuronal cells. The Field programmable Analog Array (FPAA) [1] System on Chip (SoC), a reconfigurable mixed signal hardware is utilized in this paper to show such bio-inspired circuits for energy efficient computing [2]. Tunability and programmability are achieved through the floating gate (FG) elements on the device. One could obtain different responses based on external inputs or other interconnections on the hardware itself. Furthermore, the open source Xcos/Scilab based tool framework [3] allows one to optimize the circuits, along with a higher level of compilation as well for more flexibility.

This paper takes advantage of the similarity between neuroscience and silicon to model synapses and neurons on the hardware. This block can be further expanded to build neural networks directly on the hardware and the analog signal processing offers high energy efficiency [4] and operates on low power as well, due to the fact that the analog elements are operating in the subthreshold regime.

Figure 1 illustrates the use of different blocks to build a variety of networks based on biological neuronal cells on the SoC FPAA. The neurons are Hodgkin Huxley (HH) based models emulating the ion channels. The synaptic cleft connecting the

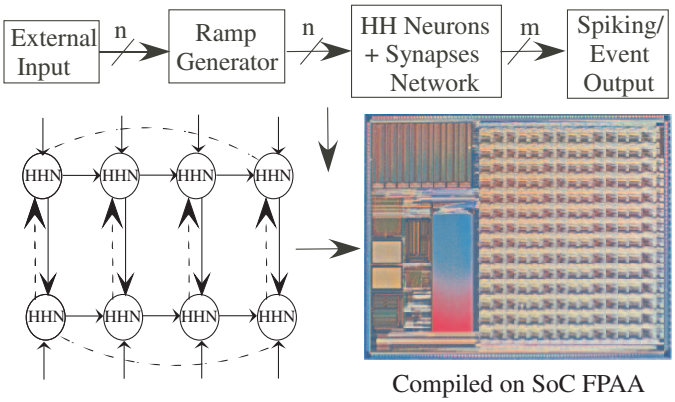

Fig. 1. A network of neurons with external inputs and projecting excitatory and inhibitory synapses between them is shown here. These are translated to a set of macroblocks based on biological neuronal cells. The system can be compiled on the SoC FPAA to obtain experimental data. The ramp generator processes the external inputs that feed the synapses and the HH neurons' network is configured in the desired topology. Each macromodel of the HH neuron, integrated with synapses, is built in a single Computational Analog block (CAB). These level=1 macroblocks are vectorized thereby allowing higher levels of compilation and enabling larger networks to be built on the SOC FPAA.

pre synaptic and post synaptic neuron is modeled to produce a triangle like response either from an external input or from another neuron. This ramp waveform is fed to a FG device in the routing that emulates the synapse and then exhibits the post synaptic response. The neuron projects to either excitatory or inhibitory synapses depending on the type of neurotransmitter a neuronal cell projects at its individual synapse. The responses of the blocks are controlled through the FG devices to generate an excitatory or inhibitory synapse and the synaptic strength is varied by modulating the charge on the floating gate.

The HH neuron along with the synaptic clefts and synapses is macromodeled and abstracted in the library blocks to be compiled onto the FPAA hardware. They are level=1 vectorized blocks with voltage input and voltage output [5]. The toolset enables one to build multiple neurons with synapses connecting between them by instantiating the library blocks [6]. This aids to build multiple configurations using the same single chip, rather than building custom chips for each configuration or application. The versatile place and route used in the tools allows one to position the blocks according to the required topology on the chip.

The experimental results obtained from the synaptic responses due to the neurotransmitters as well as the action

978-1-7281-0397-6/19/$31.00 ©2019 IEEE

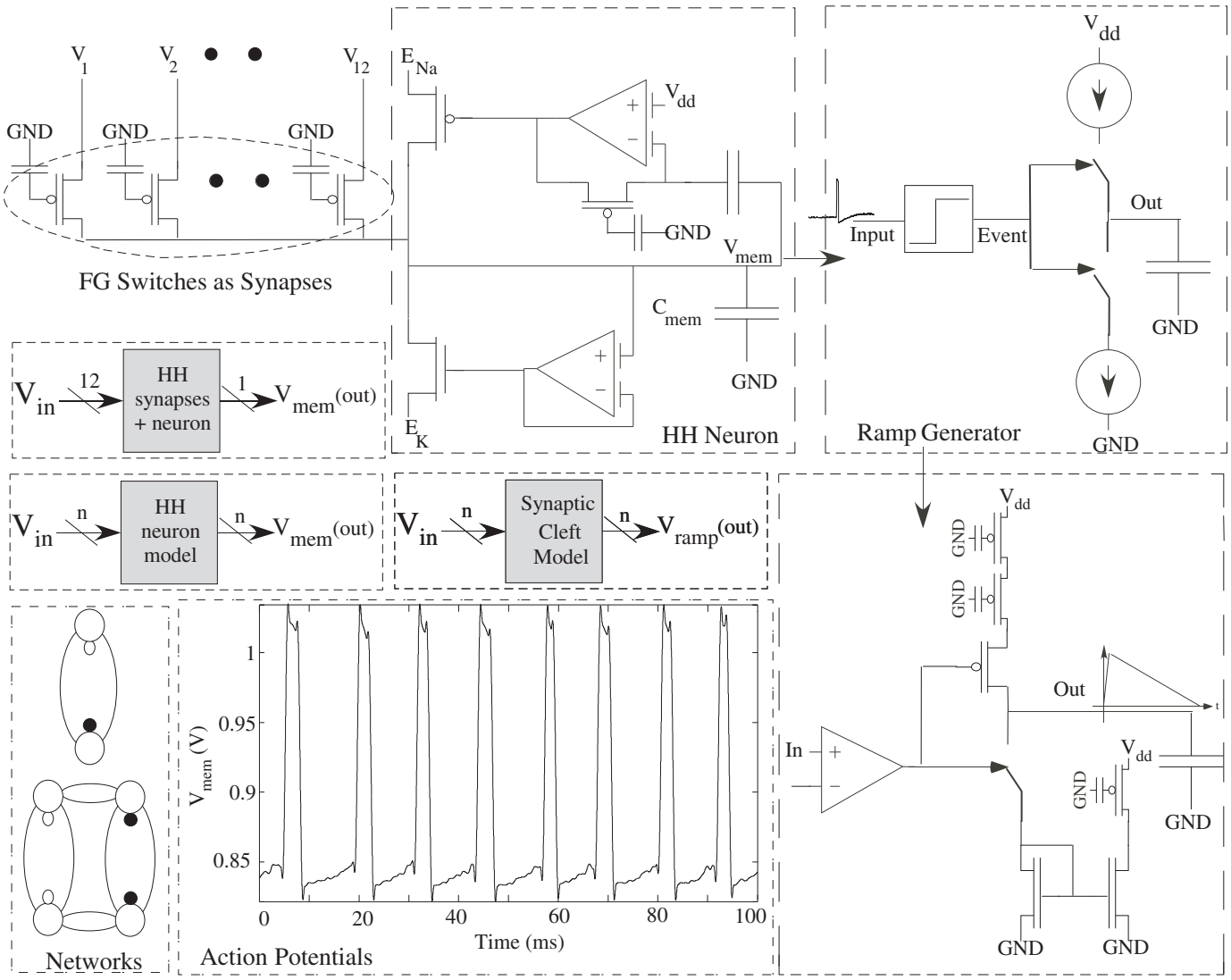

Fig. 2. The design of the Xcos blocks, namely HH neuron block with the synapses and the synaptic cleft model, constrained to one CAB, is shown here. The synapses are through the FG pFET input currents, utilizing the routing FG switches. The ramp generator models the pre synaptic cleft response to create the triangles for the inputs to the synapses. The neuron projects to either excitatory or inhibitory synapses whose strengths and biases are controlled through the FG devices, to generate an event output or an action potential from the neuron. The FG elements are programmed with subthreshold currents. In case of transistor channel based HH neuron, the gating dynamics determined by the Na^+ band-pass circuit and the K^+ low-pass configuration are implemented through FG OTAs. The ramp generator makes use of the switches in the local routing, pFET, T-gate switches and a current mirror. The OTA detects the spike, generating an event, while the FG devices in the pull-up and pull-down design control the rise and fall time of the triangle. All the blocks are vectorized, implying multiple neurons can be implemented such that each neuron goes to each of the CABs and different size networks can be created. The experimental measurements of membrane voltage from the HH neuron model for an action potential are shown here too.

potentials from the ion channel based model of HH neuron are close to the behavior observed from biological neurons and synapses. Section II gives an overview of the circuit on the FPAA, while Section III and IV describe the action potentials produced from the neuron and the synaptic cleft as a ramp generator. Section V addresses the excitatory and inhibitory synapses with how to approach the tuning of the parameters while Section VI concludes the discussion by elaborating on building networks.

II. Design and Overview of the Block Constrained to one CAB

Figure 2 illustrates the different Xcos macroblocks to build any arbitrary sized network on the chip. The fabric array on the FPAA SoC comprises Computational Logic Blocks (CLBs) and Computational Analog blocks (CABs) which are interfaced with other peripherals including SRAM, MSP 430 processor to perform programming of the FG elements [7] as well as reconfiguring the interconnections. Each CAB is configured as one neuron along with the synaptic cleft that generates the ramp waveform connecting into the synapse that projects onto the post synaptic neuron. The FG local routing fabric, consisting of FG pFET switches models the synapses and is used for computation.

The experimental measurements are taken from the FPAA fabricated on 350nm process, that has 98 CABs. A CAB consists of nFETs, pFETs, transmission gates, Operational transconductance amplifiers (OTAs), FGOTAs and capacitor

banks. Using these available resources in one CAB , the design is figured out in such a way that it replicates the biological neuronal response and minimizing area overhead. Once the neuron is designed, the remaining available elements are optimally partitioned to design the circuits required for modeling the synaptic behavior.

III. Action potentials from the HH Neuron model

The transistor channel neuron model [8] inspired by Hodgkin and Huxley's work eliciting responses from a squid axon [9] is based on the ion channels in a neuronal cell. E_{Na} and E_K represent the biological supplies to the neuron which are equivalent to the nernst ionic potentials, while C_{mem} denotes the membrane capacitance. The depolarisation and hyperpolarisation in the membrane potential, V_{mem} happen due to the opening and closing of Na^+ and K^+ ion channels and the resulting interaction between them. Their conductances are modeled through a set of FG OTAs, nFETs and pFETs. They are represented as band-pass and low-pass filter on the hardware respectively. The non-linear dynamics arising out of their interaction gives rise to a continuous spiking response to an input fed through a FG pFET in the routing as shown in Fig. 2. The spiking frequency is varied by controlling the time constants of the Na^+ and K^+ channels.

IV. Synaptic Cleft modeling

Figure 2 shows the flow of signals from the input events between the pre synaptic and post synaptic neurons through the synaptic gap, equivalent to the movement of ions in the ion channels. A current starved inverter based structure to modulate the gate of the FG elements was shown in [10] while [11] presented integrate and fire neurons with current mode integrator based synapses and conductance based synapses in [12] and [13] shows current sink based synaptic inputs.

The ramp generator can be used to process the digital input and also to mimic the synaptic cleft. The action potential from the pre synaptic neuron is fed to the ramp generator. Once the neuron spikes, it is converted to an event through an OTA that behaves as a comparator with a threshold level. Depending on if one desires a ramp up or down first, the input is fed to the corresponding terminal of OTA. As the spike is rising, the t-gate switch closes and the current mirror in the pull-down draws the current, with the rising time constant being controlled by the FG pFET. The pull-up then activates as the event falls whose time constant is much slower than the rising time, tuned by the cascode FG pFET structure in the routing. Since the post synaptic potential (PSP) of biological neurons decays slowly [14], [15], the FG pFETs are biased such that it discharges slower than the rate at which it charges. This ramp is then fed to the source of the synapse element due to the exponential relation between the output current and source of a FG pFET. If the external inputs are digital events, these triangle ramp generators can be used as well for input processing.

A current source as close to an ideal one as possible is required especially so that the ramp generator produces minimum curvature in the triangle fed to the synapse, be it

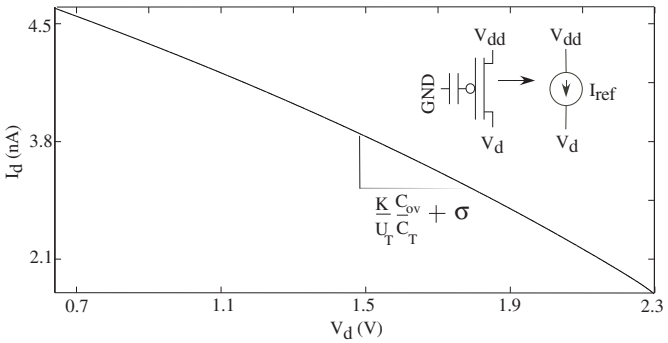

Fig. 3. The current from a FG pFET in the routing is measured as a function of the drain voltage and the I_d - V_d curve is shown in log scale. The capacitive coupling can be seen in the slope and a range of currents is obtained as the input voltage is swept. The source voltage is fixed at a V_{dd} of 2.5 V and the FG pFET is biased such that it is in saturation. From the slope, the value of effective σ is calculated thereby giving the estimate of the early voltage which shows that the overlap capacitance in the routing is significant, which may cause a curvature in the response of the ramp generator. Hence, a cascode pFET structure is used to get a more accurate current source.

inhibitory or excitatory. Hence, a through characterization of the FG pFET is performed. The drain voltage is swept to measure the drain current. The FG device is biased in the subthreshold region and the current in the saturation region is observed when the source to drain voltage is greater than 100mV, since we require it to behave as a current source. The source voltage is fixed at 2.5V. Due to early effect [16], which is a factor of the significant overlap gate to drain capacitance in the routing, the channel current depends on the drain voltage. To minimize this deviation from an ideal current source, a cascode structure is used in the pull-up design of the ramp generator which reduces the effective σ, thereby increasing the early voltage, making it a better current source.

V. Post synaptic responses through Excitatory and inhibitory Synapse

As the neurotransmitters are released into the synaptic cleft from the pre synaptic neuron, it attaches to the receptors of the post synaptic neuron causing the ion channels to open, resulting in flow of ions in the postsynaptic neuronal cell. This causes a change in the membrane potential [15] and an excitatory or inhibitory response is observed based on the type of ions that flow into the cell. An excitatory synapse causes deploarisation in the post synaptic V_{mem} while the inhibitory synapse reduces the V_{mem}.

Figure 4 shows the experimental compiled results of the triangle created from the ramp generator as well as the PSPs. The synapse is modeled by the FG pFET in the routing inspired by the single transistor learning synapse [17] while the change in membrane potential is amplified through a FG OTA with a high gain and buffered out through an OTA connected in a source follower configuration, with all the instrumentation being performed on chip.

In case of an excitatory synapse shown in Fig. 4a, the source of the FG pFET is modulated. The pFET is modeled as a biological passive channel, with its drain connected to E_K, while the EPSP measured from its source has a fast rising time and then decays down slowly.

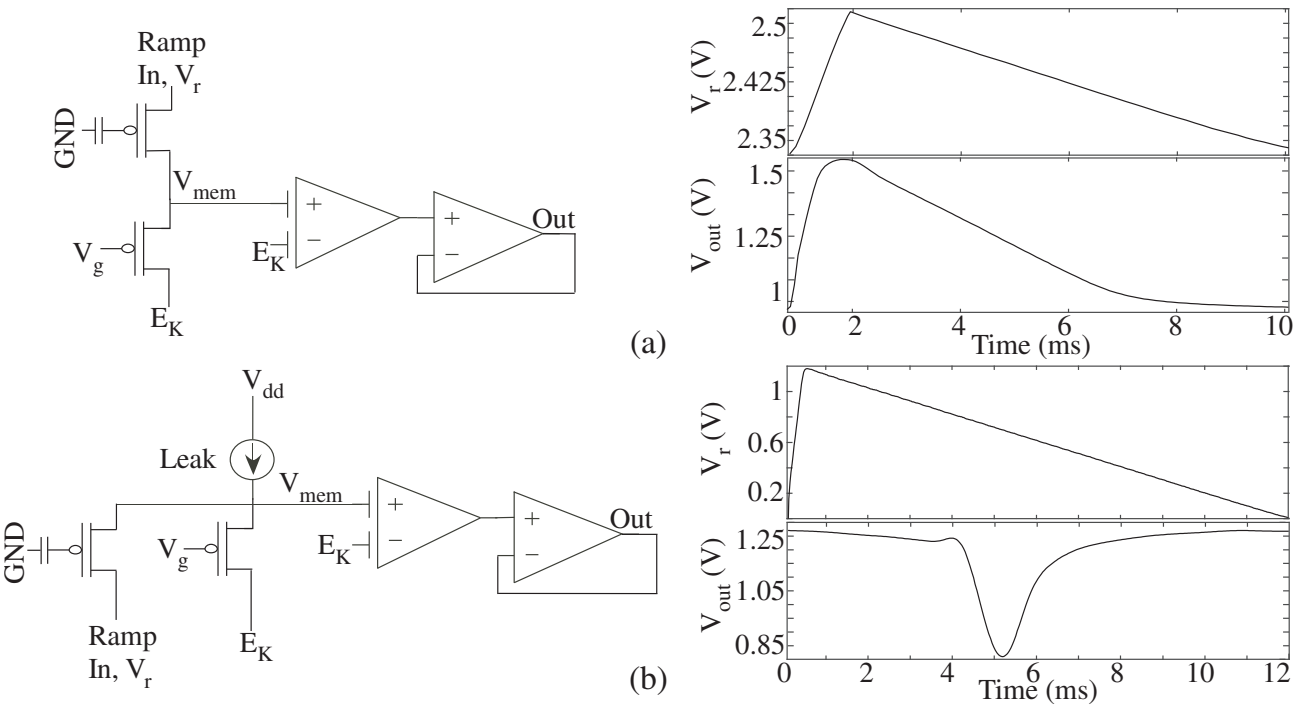

Fig. 4. The experimental measurements data from the FPAA for an excitatory and inhibitory synapse and the corresponding test setups are shown. The rise and fall times are controlled through the bias currents of the pFET and the current mirror in the ramp generator circuit. The change in membrane potential is gained up through the FG OTA and then buffered out to measure PSP. (a) The ramp input is fed to the source of the FG pFET for an excitatory synapse. The EPSP measured from the synapse with a passive channel rises up and decays slowly. (b) The ramp input is fed to the drain of the FG pFET for an inhibitory synapse. The inhibitory synapse is slower than the excitatory one and the IPSP, measured from the synapse with the passive membrane biased with a leak channel to draw the current, drops to E_K and then settles back at a resting potential.

The drain of the FG pFET is modulated for an inhibitory synapse in Fig. 4b. Hence, the ramp from the ramp generator is fed to the drain of the FG pFET and also connected to a leak channel biased by a current source that enables the FG source to draw the current and we observe an inhibitory PSP (IPSP) that drops to E_K and then rises back and settles to a resting potential. The inhibitory synapse is designed to be slower than the excitatory one, matching the biological synapses [15].

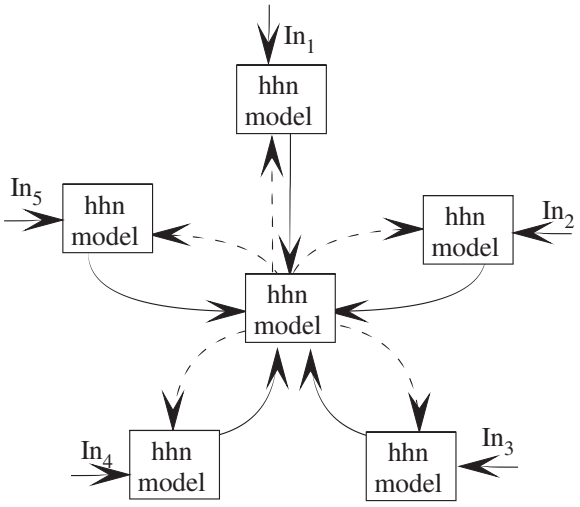

Fig. 5. A configuration of a ring Winner Take All network structure is shown. The interneuron has an inhibitory synapse associated with it represented by the dotted lines while the outer neurons are excitatory ones shown through the projections of the solid lines. Each HH neuron is configured in one CAB while the synapses are the FG pFETs in the routing.

VI. Building Networks

We have presented the macromodeled block of HH neuron model integrated with excitatory or inhibitory synapses and synaptic clefts or ramp generators, analogous to biology and demonstrated results from a reconfigurable hardware, the FPAA fabricated on 350nm process. Through the open source tool infrastructure, one could consider creating networks building upon these blocks including central pattern generators [18], [19], Winner take all (WTA) [10], [11], [20], [21] etc further used for different applications [22]–[24].

An example of one such spiking network, the WTA is shown in Fig. 5. The outer ring consists of five neurons with excitatory synapses projecting to an interneuron that feeds back an inhibitory connection to the other neurons. As the excitatory synapse activates the interneuron, the inhibitory synapse that it projects starts to inhibit the excitatory elements. The synapses are programmed through the FG elements such that the desired excitatory cell wins after the inhibition provided by the interneuron. The intra CAB variation is less [25] leading to reduced mismatch among the cells which can either be utilized [26], [27] or minimized [28] through the FG devices themselves without using extra resources for the compensation, thereby producing the desired behavior according to the corresponding application.

References

[1] S. George, S. Kim, S. Shah, J. Hasler, M. Collins, F. Adil, R. Wunderlich, S. Nease, and S. Ramakrishnan, “A programmable and configurable

mixed-mode FPAA soc," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 6, pp. 2253–2261, June 2016.

[2] C. Mead, *Analog VLSI and Neural Systems*. Addison-Wesley Longman Publishing Co., Inc., 1989.

[3] M. Collins, J. Hasler, and S. George, "An open-source tool set enabling analog-digital-software co-design," *Journal of Low Power Electronics and Applications*, vol. 6, no. 1, p. 3, 2016.

[4] J. Hasler and H. B. Marr, "Finding a roadmap to achieve large neuromorphic hardware systems," *Frontiers in Neuroscience*, vol. 7, no. 118, 2013.

[5] A. Natarajan and J. Hasler, "Modeling, simulation and implementation of circuit elements in an open-source tool set on the FPAA," *Analog Integrated Circuits and Signal Processing*, vol. 91, no. 1, pp. 119–130, 2017.

[6] J. Hasler, A. Natarajan, and S. Kim, "Enabling energy-efficient physical computing through analog abstraction and ip reuse," *Journal of Low Power Electronics and Applications*, vol. 8, no. 4, p. 47, 2018.

[7] S. Kim, J. Hasler, and S. George, "Integrated floating-gate programming environment for system-level ics," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. PP, no. 99, pp. 1–9, 2016.

[8] A. Natarajan and J. Hasler, "Hodgkin–huxley neuron and fpaa dynamics," *IEEE transactions on biomedical circuits and systems*, vol. 12, no. 4, pp. 918–926, 2018.

[9] A. L. Hodgkin and A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *The Journal of Physiology*, vol. 117, no. 4, pp. 500–544, 1952.

[10] S. Brink, S. Nease, P. Hasler, S. Ramakrishnan, R. Wunderlich, A. Basu, and B. Degnan, "A learning-enabled neuron array ic based upon transistor channel models of biological phenomena," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 1, pp. 71–81, Feb 2013.

[11] G. Indiveri, E. Chicca, and R. Douglas, "A vlsi array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity," *IEEE Transactions on Neural Networks*, vol. 17, no. 1, pp. 211–221, Jan 2006.

[12] T. Yu, T. J. Sejnowski, and G. Cauwenberghs, "Biophysical neural spiking, bursting, and excitability dynamics in reconfigurable analog vlsi," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 5, pp. 420–429, Oct 2011.

[13] J. Schemmel, A. Grubl, K. Meier, and E. Mueller, "Implementing synaptic plasticity in a vlsi spiking neural network model," in *The 2006 IEEE International Joint Conference on Neural Network Proceedings*, July 2006, pp. 1–6.

[14] C. Koch, *Biophysics of Computation: Information Processing in Single Neurons (Computational Neuroscience Series)*. New York, NY, USA: Oxford University Press, Inc., 2004.

[15] D. Purves, G. Augustine, and D. Fitzpatrick, *Neuroscience. 2nd edition. ; 2001.* Sunderland (MA): Sinauer Associates, 2001.

[16] T. A. Fjeldly and M. Shur, "Threshold voltage modeling and the subthreshold regime of operation of short-channel mosfets," *IEEE Transactions on Electron Devices*, vol. 40, no. 1, pp. 137–145, Jan 1993.

[17] P. Hasler, C. Diorio, B. A. Minch, and C. Mead, "Single transistor learning synapses," in *Proceedings of the 7th International Conference on Neural Information Processing Systems*, ser. NIPS'94. Cambridge, MA, USA: MIT Press, 1994, pp. 817–824. [Online]. Available: http://dl.acm.org/citation.cfm?id=2998687.2998789

[18] M. Ambroise, T. Levi, S. Joucla, B. Yvert, and S. Saighi, "Real-time biomimetic central pattern generators in an fpga for hybrid experiments," *Frontiers in Neuroscience*, vol. 7, p. 215, 2013. [Online]. Available: https://www.frontiersin.org/article/10.3389/fnins.2013.00215

[19] T. Levi, F. Khoyratee, S. Saghi, and Y. Ikeuchi, "Digital implementation of hodgkin—huxley neuron model for neurological diseases studies," *Artif. Life Robot.*, vol. 23, no. 1, pp. 10–14, Mar. 2018. [Online]. Available: https://doi.org/10.1007/s10015-017-0397-7

[20] A. Basu, S. Ramakrishnan, C. Petre, S. Koziol, S. Brink, and P. E. Hasler, "Neural dynamics in reconfigurable silicon," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 5, pp. 311–319, Oct 2010.

[21] M. Oster, R. Douglas, and S.-C. Liu, "Computation with spikes in a winner-take-all network," *Neural computation*, vol. 21, no. 9, pp. 2437–2465, 2009.

[22] S. Koziol, S. Brink, and J. Hasler, "A neuromorphic approach to path planning using a reconfigurable neuron array ic," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 12, pp. 2724–2737, Dec 2014.

[23] S. Sheik, M. Coath, G. Indiveri, S. Denham, T. Wennekers, and E. Chicca, "Emergent auditory feature tuning in a real-time neuromorphic VLSI system," *Frontiers in Neuroscience*, vol. 6, no. 17, 2012.

[24] S. Renaud, J. Tomas, N. Lewis, Y. Bornat, A. Daouzli, M. Rudolph, A. Destexhe, and S. Saighi, "Pax: A mixed hardware/software simulation platform for spiking neural networks," *Neural Networks*, vol. 23, no. 7, pp. 905 – 916, 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0893608010000638

[25] A. Natarajan and J. Hasler, "Dynamics of hodgkin huxley neuron across chips implemented on a reconfigurable platform," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–5.

[26] O. Richter, R. F. Reinhart, S. Nease, J. Steil, and E. Chicca, "Device mismatch in a neuromorphic system implements random features for regression," in *2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct 2015, pp. 1–4.

[27] E. Neftci, E. Chicca, G. Indiveri, and R. Douglas, "A systematic method for configuring vlsi networks of spiking neurons," *Neural Computation*, vol. 23, no. 10, pp. 2457–2497, 2011.

[28] S. Kim, S. Shah, and J. Hasler, "Calibration of floating-gate SoC FPAA system," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2017.