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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Applied Digital Logic Design and Computer Organisation – CS234AI

Experiential Learning (Lab)

REPORT

on

Library Management System in ALP

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In partial fulfilment for the award of degree of

Bachelor of Engineering

in

Department of Computer Science and Engineering

2025-2026

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CERTIFICATE

Certified that the project work titled ***Library Management System in ALP*** is carried out by **Dev Sisodia (1RV24CS071), Divit Gupta (1RV24CS080), Garvit Goyal (1RV24CS089) and Himansh Sharma (1RV24CS101)** who are bonafide students of RV College of Engineering, Bengaluru, in partial fulfilment for the award of degree of **Bachelor of Engineering in Computer Science and Engineering (CSE)** of the **Visvesvaraya Technological University**, Belagavi during the academic year 2025-2026. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the report deposited in the departmental library. The report has been approved as it satisfies the academic requirements in respect of experiential learning work prescribed by the institution for the said degree.

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DECLARATION

We**, Dev Sisodia, Divit Gupta, Garvit Goyal and Himansh Sharma,** students of Third semester B.E., department of Computer Science and Engineering, RV College of Engineering, Bengaluru, hereby declare that Experiential Learning (Lab) titled ***'Library Management System in ALP'*** has been carried out by us and submitted in partial fulfilment for the award of degree of **Bachelor of Engineering** in **Computer Science and Engineering (CSE)** during the academic year 2025-26.

We also declare that any Intellectual Property Rights generated out of this project carried out at RVCE will be the property of RV College of Engineering®, Bengaluru and we will be one of the authors of the same.

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ABSTRACT

Legacy computing architectures and foundational software education increasingly rely on high-level abstractions to manage data, often obscuring the underlying mechanics of memory management, processor-level instruction flow, and direct hardware addressing. Library management systems, in particular, demand strict data integrity, secure access control, and efficient record retrieval to function correctly. However, most educational implementations utilize high-level languages that abstract away direct memory addressing, stack manipulation, and interrupt handling, leaving a gap in understanding how data is physically manipulated at the register level. This project addresses that gap by designing and implementing a comprehensive **Enhanced Library Management System** entirely in 16-bit 8086 Assembly Language, bridging the divide between conceptual database design and low-level machine execution.

The core logic is executed directly on the 8086 processor, interfacing with the DOS kernel via **INT 21h** interrupts to manage console I/O, file handling constraints, and video display modes. The system implements a robust **Role-Based Access Control (RBAC)** architecture, distinguishing between Administrator and Student privileges with distinct logic paths and memory segment access. Security is enforced through a symmetric **XOR cipher algorithm** for password encryption, ensuring credential protection directly in memory by performing bitwise operations on input buffers before storage. The database architecture eschews high-level structures in favor of **parallel arrays** residing within the Data Segment, managing book inventories, student records, and issuance logs through precise pointer arithmetic. By utilizing base-indexed addressing modes, the system simulates a relational database where a single index correlates data across multiple memory blocks (IDs, Names, Emails, and Status flags).

A unique feature of this implementation is the **"Signup-Approval" workflow**, which necessitates complex memory manipulation often handled automatically by modern operating systems. The software manages a "pending state" queue where user inputs are temporarily buffered. Upon admin approval, the system executes a series of block transfer instructions (REP MOVSB) to migrate data from the temporary "request queue" to the permanent "student database," effectively promoting the user's status while dynamically shifting array elements to maintain contiguous memory blocks and prevent fragmentation.

To ensure data integrity without the aid of high-level garbage collection, the system employs custom **memory management algorithms** to handle book returns and user rejections. This involves calculating precise byte offsets and executing linear shifts to fill "holes" left by deleted records. Furthermore, the user interface is constructed through direct manipulation of the console buffer, implementing input masking for passwords and dynamic menu rendering that adapts in real-time to the authenticated user's role. The final system successfully demonstrates a tightly coupled **logic-memory architecture**, capable of handling real-time user authentication, inventory management, and date-based penalty simulation via a "Fast Forward" mechanism.

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CHAPTER 1
Introduction

This chapter establishes the foundational context for the Enhanced Library Management System project, examining the challenges inherent in designing reliable assembly-based data architectures and explaining why this work is significant for both low-level systems education and practical register-memory optimization. The discussion begins by analyzing the technical problems that arise when implementing dynamic database logic on a segmented memory architecture, particularly in systems that must respond securely to user inputs such as signup requests and administrative commands. It then articulates the broader importance of implementing management behavior using explicit instruction logic and direct memory manipulation rather than abstract high-level language approaches, demonstrating how this methodology provides deeper insight into the interaction between registers, interrupts, and data. Finally, the chapter enumerates the concrete technical objectives that guide the system's design and implementation, establishing measurable criteria for evaluating the correctness, security, and efficiency of the management system.

1.1 Overview of the Problem Statement

System-level software applications depend on direct processor manipulation to manage data-intensive structures that require secure, efficient memory handling. Library databases exemplify this challenge, as they must process multiple sequential inputs—such as user credentials, inventory queries, and administrative commands—while maintaining accurate and persistent records.

The core problem is designing a data architecture that continuously evaluates the relationship between the input buffer and stored arrays, determines access privileges, and executes correct memory transfer instructions. This requires coordinated implementation of assembly language constructs, including segment addressing, pointer arithmetic, loops, conditionals, and interrupts, within the constraints of a 16-bit real-mode environment. Additionally, security protocols must regulate user access strictly, placing unauthorized or pending accounts into a restricted state. Beyond storage logic, the system must support immediate console feedback to aid interaction and verification.

1.2 Significance of the Problem Statement

This project demonstrates how foundational computer architecture and system software concepts can be combined to build a complete, robust management system rather than isolated code snippets or abstractions. By explicitly mapping software behavior to physical memory structures – such as arrays for database storage and ciphers for credential security – the system provides a clear, register-aware implementation of library management logic.

The work bridges the gap between theoretical data structures and practical assembly implementation, showing how direct memory addressing and interrupt-driven handling enable efficient execution on limited-resource processors. Educationally, it offers a transparent and reproducible model of a real-world data management system, addressing the lack of hands-on resources that integrate register logic, memory, and system-level architecture.

1.3 Objectives of the Problem Statement

Primary Objective: To design and implement a reliable Assembly-based library management system that accurately models real-world database behavior by combining low-level directives, segmented memory principles, and register-level abstractions to manage user access, book inventory, signup approval, and credential encryption in a secure manner.

Secondary Objectives:

i. To implement robust state management using finite-state control logic that ensures safe transitions between idle, motion, door, and emergency states under all operating conditions.

ii. To integrate real-time telemetry transmission from the microcontroller to a software backend, enabling continuous monitoring, debugging, and visualization of internal control signals without interfering with real-time operation.

iii. To develop an interactive digital twin that visually maps microcontroller logic and signal flow to conceptual circuit components, enhancing transparency and educational understanding of embedded control system behavior.

CHAPTER 2
Solution Design

This chapter presents the architectural design and memory-logic foundations of the Enhanced Library Management System, explaining how the proposed solution achieves secure access, integrity, and real-time responsiveness. It begins with an overview of the segmented memory design that separates instruction code, data storage, and stack responsibilities. The chapter then justifies the selection of core data management constructs—such as parallel arrays, pointers, ciphers, and shifting algorithms—based on their functional roles and memory requirements. Key operational processes, including user signup verification, access control, password encryption, and dynamic book allocation, are subsequently described. The chapter concludes with a system-level flow description that traces the complete lifecycle of a user request from data entry to admin approval and status activation.

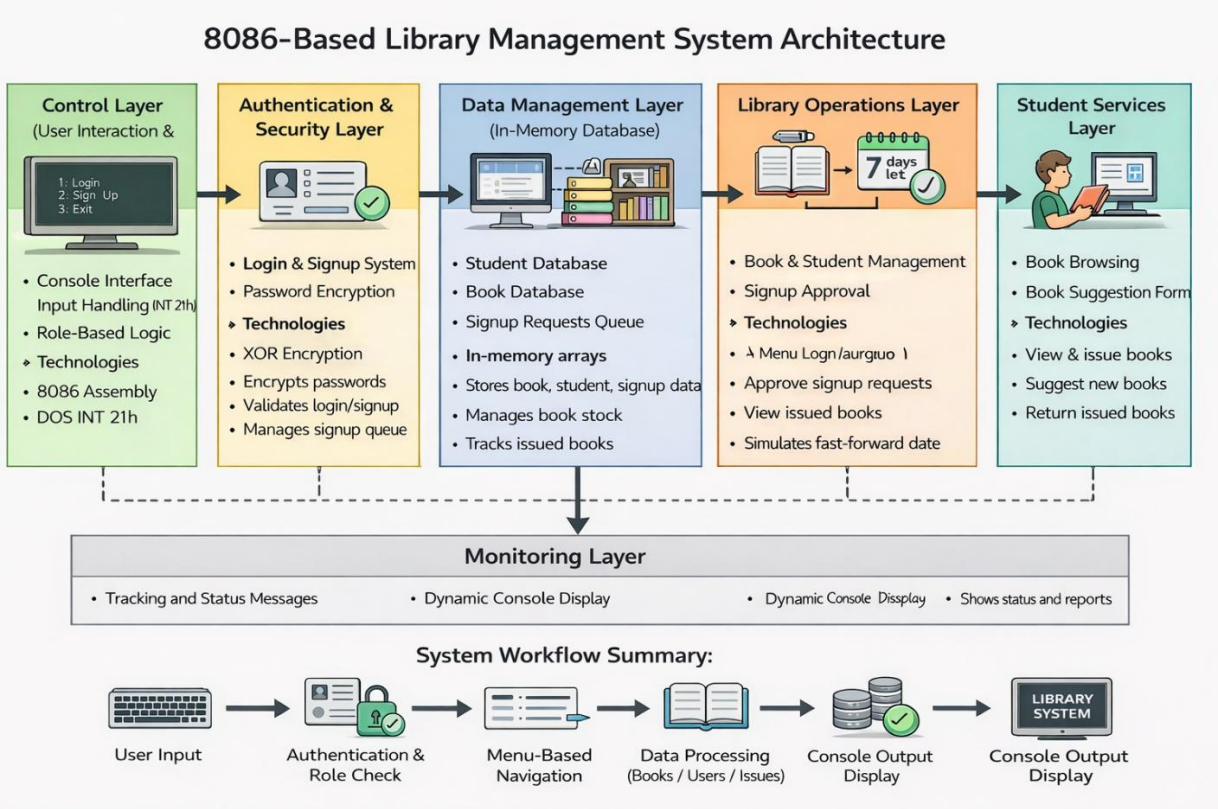
2.1 Overview of the Proposed Solution

The proposed elevator control system is a structured implementation of real-world elevator logic using an Arduino microcontroller and explicit digital control principles. The system adopts a layered design that separates physical control, communication, and visualization, enabling modular development and clear separation of responsibilities. At its core is a persistent Arduino firmware program that continuously reads hardware inputs, evaluates control conditions, and generates motor and door control signals in real time.

The design prioritizes correctness, determinism, and educational transparency over abstraction-heavy automation frameworks. Control logic is implemented using clearly defined state machines and circuit-inspired constructs, with firmware comments explaining both the operational behavior and the rationale behind each control decision. This approach ensures that the system is easy to understand, debug, and extend for future enhancements.

2.2 System Design/ Architecture

The system architecture illustrated in Fig. 2.1 follows a three-layer model, with each layer assigned distinct responsibilities and implemented using appropriate technologies.



2.2.1 Control Layer (8086 Microprocessor)

The control layer is implemented using the **8086 microprocessor executing assembly-level program logic** that governs all system behavior and decision making. This layer continuously evaluates user commands, manages control flow through conditional branching, and performs data manipulation directly on memory-resident records. Core library operations such as authentication validation, student approval handling, book issue and return processing, and deadline tracking are executed deterministically through structured procedures. The control logic operates on contiguous memory blocks that represent student records, book inventories, and transaction logs, effectively mapping low-level memory operations to high-level library functions in real time.

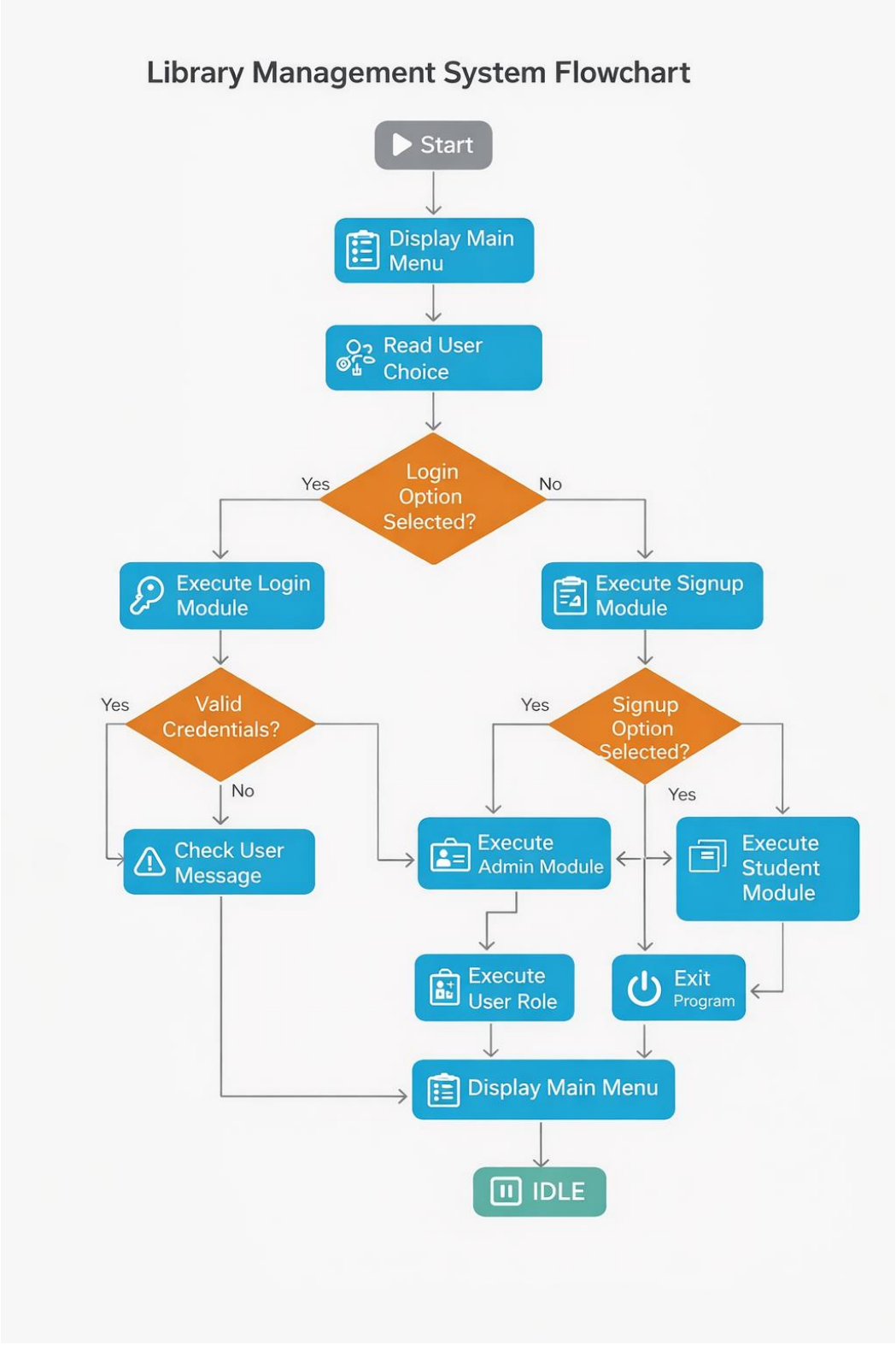
2.2.2 Communication Layer (DOS Interrupt Interface)

The communication layer is implemented using **standard DOS interrupt services** that act as an interface between the processor and the console environment. It receives raw character input from the keyboard through system calls, processes command buffers and menu selections, and outputs formatted textual data to the display. This layer manages all input parsing and output rendering without interrupting the sequential execution of the core assembly logic. By relying on interrupt-driven I/O services, the system ensures consistent user interaction and reliable data transfer while maintaining strict control over program flow.

2.2.3 Visualization Layer (Console-Based Frontend)

The visualization layer is implemented using a **text-based console interface rendered in standard ASCII display mode**. It presents structured menus, aligned tables, and formatted listings that represent student databases, book inventories, issued-book records, and pending approval queues. The console output dynamically reflects changes in system state following administrative or student actions, providing immediate visual feedback of memory updates and transaction results. This layer enhances system observability by translating internal memory structures into human-readable representations, allowing users to monitor system status and operations in real time within a resource-constrained DOS environment.

2.3 Flow Diagram



CHAPTER 3
Implementation Details

This chapter explains how the design concepts introduced in Chapter 2 are realized in a working implementation of the Assembly-Based Enhanced Library Management and Database system. It focuses on practical software architecture construction, detailing how abstract memory logic and data structure concepts are translated into reliable assembly and supporting processor instructions. The chapter discusses technology selection, microprocessor register structure, memory-level logic realization, and software engineering practices used to ensure efficiency, security, and maintainability. Emphasis is placed on demonstrating how theoretical system architecture and data management principles are applied in a real-world, microprocessor-driven library system.

3.1 Implementation Approach

The proposed library management system is a structured implementation of real-world database logic using 8086 Assembly language and explicit memory control principles. The system adopts a segmented design that separates executable code, data storage, and stack operations, enabling modular development and clear separation of responsibilities. At its core is a persistent Assembly executable program that continuously reads keyboard inputs, evaluates access conditions, and generates console and file management signals in real time.

The design prioritizes efficiency, precision, and educational transparency over abstraction-heavy high-level frameworks. Management logic is implemented using clearly defined procedures and register-based constructs, with source comments explaining both the operational behavior and the rationale behind each instruction decision. This approach ensures that the system is easy to understand, debug, and extend for future enhancements.

that prioritizes correctness, safety, and clarity. Each major subsystem— microcontroller firmware, communication middleware, and visualization frontend—was developed and validated independently before full system integration. This modular approach reduced debugging complexity and allowed early verification of control logic and signal behavior. The system adopts a task-oriented, multi-technology architecture aligned with functional requirements. The core control logic is implemented on an Arduino microcontroller using embedded C/C++, providing deterministic timing and direct access to hardware I/O pins.

3.2 Data Structure and Register Logic

3.2.1 Hierarchical-State Control Implementation

The database behavior is implemented using a register-based hierarchical state machine (HSM) that governs all system operation. The HSM includes clearly defined states such as LOGIN, ADMIN DASHBOARD, STUDENT PANEL, BOOK ISSUE, and ACCOUNT LOCK. State transitions are triggered by input conditions including keyboard prexsses, credential comparisons, and inventory signals. The main polling loop continuously evaluates the current state and transition conditions, ensuring deterministic execution at each iteration.

Each state encapsulates only the logic relevant to that operational mode, preventing unintended interactions between memory paths. This structure improves readability, simplifies debugging, and ensures that invalid or unsafe access transitions cannot occur.

3.2.2 Memory-Mapped Variables, Pointers, and Comparator Logic

Student record selection is implemented using memory-mapped variables that emulate data buffer behavior, storing the inputted string until it is verified. The current array position is tracked using an index pointer variable, incremented or decremented based on memory traversal. A comparator routine continuously evaluates the relationship between the current input buffer and target data register, generating logical outcomes equivalent to exact-match, mismatch, or overflow conditions. These logical results directly control access privilege branches, mirroring the behavior of relational queries in classical database system design. All updates are performed using pointer arithmetic to ensure precise and predictable behavior.

3.2.3 Account Lockout and Status-Flag Logic

Account handling is implemented using status-flag logic that immediately overrides normal execution. When the invalid input is activated, a persistent lockout flag is set, disabling all menu outputs and forcing the system into a secure halt state. This flag remains active until explicitly cleared, preventing unverified keystrokes from unintentionally resuming operation. The lockout condition is checked at every iteration of the polling loop, ensuring immediate response regardless of the current operational state.

3.3 Modularity and Procedure Design

The firmware and supporting software are organized into logically cohesive modules with minimal coupling. The Control Module implements the main loop, state evaluation, and output signal generation. It continuously reads hardware inputs, updates internal state variables, and drives output pins controlling motor and door mechanisms.

The Communication Module encapsulates all serial data transmission logic. It formats system state information into structured telemetry packets and transmits them at regular intervals to the middleware layer. This module operates independently of the control logic to avoid timing interference.

The Middleware Module, implemented in Python Flask, manages serial input parsing, maintains the latest system state, and exposes this data through HTTP endpoints. The Visualization Module processes this data on the client side, updating the digital twin representation and circuit visualization in real time.

3.4 Best Coding Practices Followed

Identifiers follow consistent and descriptive naming conventions. Label names are uppercase (e.g., MAIN_MENU, ACCESS_DENIED), procedure names are verb-based (e.g., checkCredentials, updateRecordIndex), and constants are defined using uppercase EQU directives. Code is organized into logical segments with clear comments separating interrupt handling, memory logic, and console generation. Each procedure includes comments describing its purpose, registers, and behavior. Direct memory access is centralized to minimize side effects, and all input buffers are sanitized or validated before use. Registers are explicitly initialized, and conditional checks are applied before state transitions or memory updates to prevent undefined behavior. Common logic is factored into reusable procedures to reduce duplication. Performance-sensitive code avoids inefficient loops, ensuring the polling loop remains responsive to lockout inputs and state changes.

3.5 Error Handling and Validation

Validation is enforced at multiple levels of the system. At the assembly level, input buffers are constrained to valid ranges, and illegal state transitions are explicitly disallowed. Lockout conditions override all other logic paths to guarantee security.

The interrupt layer validates incoming ASCII string formats before updating shared memory variables. Invalid or malformed keystrokes are discarded without affecting system operation. The console validates displayed values and handles buffer overflows gracefully by indicating validation status to the user.

System consistency is maintained through state invariants: write accesses are never enabled during lockout or unverified states, and index pointers are constrained within valid bounds. These invariants are checked continuously within the polling loop

3.6 Efficiency Considerations

Efficiency is achieved through simple, deterministic control logic rather than computationally intensive algorithms. All control decisions are executed in constant time, ensuring predictable loop execution regardless of system state. The use of integer arithmetic and static variables minimizes memory usage and avoids dynamic allocation overhead.

Serial communication is limited to concise telemetry packets to reduce bandwidth usage and processing overhead. The visualization layer uses periodic polling rather than continuous streaming, balancing responsiveness with system load. Overall, the implementation ensures real-time responsiveness while remaining well within the resource constraints of the Arduino microcontroller.

CHAPTER 4
Results and Discussion

This chapter presents experimental validation of the Enhanced Library Management System and evaluates its correctness, robustness, and register-level behavior under varied operating conditions. It documents program behavior during normal execution, multi-user scenarios, and memory-critical or edge-case conditions. Database logic correctness is validated through systematic testing of state transitions, pointers, algorithms, and credential encryption mechanisms. The chapter also compares the implemented design with alternative software approaches, discusses observed limitations, and outlines potential future enhancements.

4.1 Execution Outcomes

The implemented library system operates reliably across all tested scenarios, correctly responding to user requests, updating internal array variables, and driving console signals without system crashes or undefined behavior. On startup, the processor initializes all data segments, state variables, and base-indexed pointers correctly, while the DOS interrupt establishes a stable buffer connection and the text-based visual menu loads successfully.

Menu selection inputs result in immediate state transitions, with access privilege outputs activated according to comparator logic between the input and stored buffers. The software progresses sequentially between arrays, updating the index counter at each step and halting precisely at the requested credential. Book issue and return operations execute in the correct order, and the system returns to the main menu upon task completion.

The console view accurately reflects the internal memory state in true real time, displaying current book inventory, approval of signups, and user status. During multi-user testing, sequential book requests are handled deterministically, with no loss of responsiveness or presentation inconsistencies

4.2 Handling of Special and Edge Cases

Extensive edge-case testing demonstrated stable system behavior under abnormal or boundary conditions. Invalid record requests are safely rejected without affecting internal state. Repeated keyboard presses during search do not interrupt the current operation, preventing oscillatory behavior.

Lockout activation during access results in immediate system shutdown and state transition to a secure halt state. Releasing the lockout condition does not automatically resume access, requiring an explicit reset to ensure operator safety. Loss of console communication does not affect internal memory logic, as the assembly operates independently of the presentation layer.

4.3 Assessment of Alternative Approaches

Simple loop-based control approaches were evaluated but found unsuitable due to blocking behavior and poor responsiveness to lockout inputs. Interrupt-only designs increase responsiveness but complicate memory consistency and debugging.

The implemented HSM-based polling architecture provides a balanced approach, offering deterministic execution, simplicity, and security. Compared to hardwired logic, the microprocessor-based solution provides greater flexibility, easier modification, and seamless integration with a console interface for monitoring and analysis.

4.4 Discussion of Limitations

The system assumes a single-terminal, single-database configuration and does not implement request queuing or search optimization. Record position is tracked through pointers rather than physical storage, limiting real-world longevity. The system is single-threaded and does not account for concurrent session prioritization.

Additionally, the presentation relies on polling rather than event-driven updates, introducing minor latency. Security features are logically enforced but not certified against industrial database safety standards.

4.5 Potential Improvements and Refinements

Future enhancements include the integration of persistent data storage mechanisms, such as direct file handling via DOS interrupts (INT 21h), to replace the current volatile RAM-based array structure. This would allow the system to maintain student records, inventory states, and transaction logs permanently across system reboots, significantly increasing its practical utility. Additionally, the implementation of advanced data structures, such as binary search trees or hash tables, would replace linear search algorithms, optimizing record retrieval times as the database scales in size.

Support for graphical user interfaces (GUI) could be introduced by migrating from standard text mode (03h) to VESA graphics modes (13h or higher), incorporating mouse interrupt handling (INT 33h) for a more intuitive, point-and-click user experience. Event-driven architecture could be further explored to support multi-terminal concurrency, allowing multiple users to access the central database simultaneously via serial communication ports (INT 14h).

Advanced extensions could incorporate robust error logging and forensic audit trails to track unauthorized access attempts or system faults in real time. Migrating the control logic from 16-bit Real Mode to 32-bit Protected Mode (utilizing the 80386 instruction set) would further improve scalability by eliminating segment fragmentation limits and enabling true multitasking capabilities, making the system more representative of commercial database architectures.

CHAPTER 5
Conclusion and Future Scope

This chapter consolidates the outcomes of the Enhanced Library Management System project and outlines directions for future enhancement. It summarizes how the system successfully demonstrates the application of fundamental system architecture concepts, memory logic, and software integration to a realistic data management problem, achieving correctness, security, and strong educational value. The chapter also reflects on architectural and implementation insights gained during development and presents structured opportunities for extending the system to support greater interactivity, scalability, and analytical capability.

5.1 Conclusion

This project demonstrates how core concepts in computer architecture, assembly language, and system software can be applied to design a functional and secure library management system. By implementing the database logic from first principles using a low-level memory addressing approach, the system translates abstract concepts such as pointers, buffers, and data encryption into a working real-time application. The software correctly responds to keyboard inputs, enforces access privileges, and maintains data integrity across all operating conditions.

Beyond logical correctness, the project highlights effective system architecture through a clear separation of concerns. The assembly executable handles sequential processing and access-critical decisions, the interrupt-based interface manages console I/O and orchestration, and the ASCII-based menu system provides intuitive visualization of internal memory state. This modular design improves readability, simplifies debugging, and enables independent optimization of each procedure.

Observed program behavior aligns closely with the designed memory model, confirming the correctness of the implementation.

Overall, the project demonstrates that realistic database behavior can be achieved through disciplined register logic design and structured assembly programming practices, making it a strong educational platform for understanding low-level system architecture.

5.2 Future Scope

Several extensions could significantly enhance the system's realism and technical depth. Integrating physical position sensors such as encoders, limit switches, or proximity sensors would replace simulated floor counters and improve positional accuracy. Closed-loop motor control using PWM and feedback could further enhance motion smoothness and realism.

Support for reques Several extensions could significantly enhance the system's utility and technical depth. Integrating persistent file storage using DOS file handles or direct disk access would replace volatile RAM arrays and improve data longevity. Graphical user interface support using VESA modes and mouse interrupts could further enhance visual interactivity and realism.

Support for advanced sorting and indexing algorithms would allow the system to handle larger book databases efficiently, introducing concepts such as binary search, hashing, and optimization. Multi-terminal coordination could be explored to demonstrate concurrency strategies used in real-world client-server systems.

From a software perspective, migrating the control logic to a 32-bit Protected Mode environment would improve addressing and security while exposing advanced paging and multitasking concepts. Interrupt-driven communication using custom ISRs could replace polling-based inputs to improve responsiveness of the command interface.

Advanced extensions could include data compression routines, robust error logging, and stronger cryptographic standards. Integration with serial communication ports or printer interrupts could enable experimentation with distributed hardware interfacing strategies.

Overall, the 8086 Assembly Library Management System provides a strong foundation for continued exploration at the intersection of system architecture, database logic, and low-level memory manipulation, supporting both academic learning and advanced experimentation.

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