Experiment No. 8 **FLIP-FLOPS**

To investigate the operation of various flip-flops, SR, JK, D and T using gates and flip-flop ICs.

A Flip-Flop is a Bistable-Multivibrator, which is capable of storing one bit of information. It has two outputs, one for normal value and one for the complement value. The input to the flip-flop can be fed in a number of ways and this fact give rise to different types of flip-flop. There are two characteristics shared by all flip-flops,

1. If input to the flip-flop causes it to go to '1' state, it will remain there until some signal causes it to go to '0' state and vice-versa, i.e., a FF has two stable states.

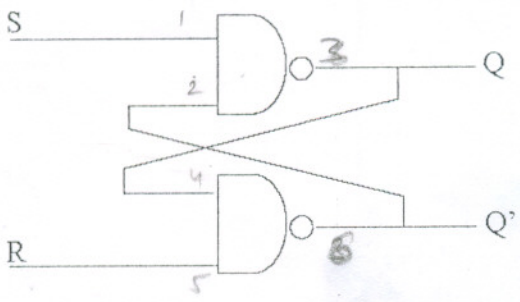
2. The flip-flop has two output signals, one of which is the complement of the other.

In this experiment you will construct, test and investigate the operation of various flip-flop circuits; RS, D, JK, and T flip-flops.

Activity-1. SR Latch

The SR Latch is a basic flip-flop made with two cross-coupled NAND gates. It has two inputs S(SET) and R(RESET), and it has two outputs Q and Q'.

Circuit Diagram:



Observations: Truth-Table

Inputs	Outputs	Comments
S R	Q_{t+1} Q'_{t+1}	
0 0		
0 1		
1 0		
1 1		

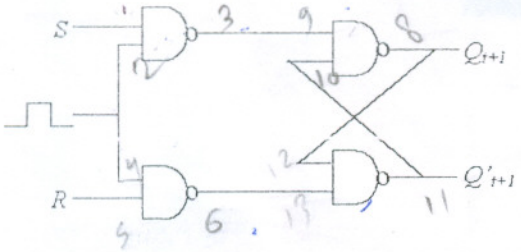
Procedure:

Step.1. Construct the basic FF circuit and connect the two input switches and the two outputs to the indicator lamps.

*Step.*2. Set the two switches to LOGIC-1, then momentarily turn each switch separately to the LOGIC-0 position and back to the 1.

*Step.*3. Obtain the Truth-Table of the circuit.

Activity-2. Clocked RS Flip-Flop



Observations: Truth-Table

Inputs			Outputs		Comments
CLK	S	R	Q_{t+1}	Q'_{t+1}	
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Procedure:

Step.1. Construct a clocked RS flip-flop with four NAND gates.

Step.2. Connect the S and R inputs to the two switches and the clock input to a pulsar.

Step.3. Obtain the 'truth-Table' of the circuit.

Activity 3. Implementation of Positive Edge-Triggered D Flip-Flops Using 7474 IC

IC 7474 consists of two D-Positive Edge-triggered FFs with preset and clear. Its PIN assignment is shown in Fig. Below.

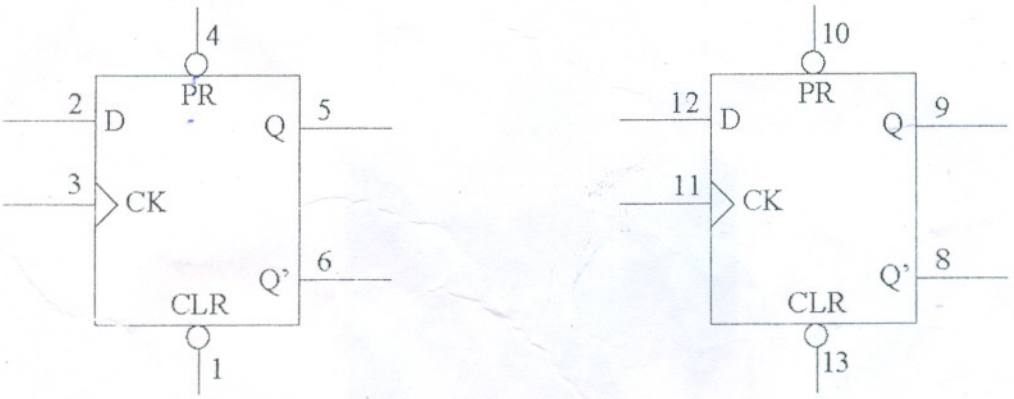


Fig. Logic Symbol, Vcc(14),GND(7)

Observations: Function Table

Inputs				Outputs	
Preset	Clear	Clock	D	Q	Q'
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	↑	0	0	1
1	1	↑	1	1	0
1	1	0	X	No Change	No Change

The Function Table specifies the preset and clear operations and the clock operation. The clock is shown with an upward arrow to indicate that it is a positive edge-triggered FF.

Investigate the operation of one of the FF and verify its function table.

Activity-4. Implementation of Clocked JK Flip-Flops Using IC 7476

IC type 7476 consists of two JK Master-Slave FFs with Preset and Clear. The pin assignment for each FF is shown in the Fig. Below.

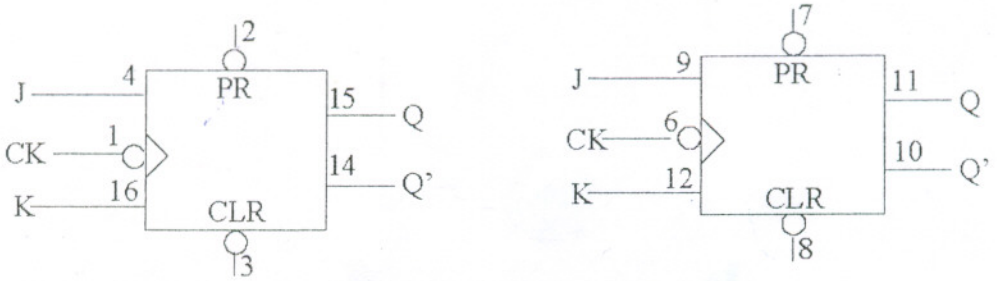


Fig. Logic Symbol, Vcc(5), GND(13)

Observations: Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	⊓	0	0	No Change	No Change
1	1	⊓	0	1	0	1
1	1	⊓	1	0	1	0
1	1	⊓	1	1	Toggle	Toggle

From the Function-Table, the first three entries in the table specify the operation of the asynchronous preset and the clear inputs. These inputs behaves like a NAND SR Latch and are independent of the clock or J and K inputs. The last four entries in the function table specify the clock operation with both the preset and clear inputs maintained at the Logic '1'. The clock value is shown as a 'Single Pulse'.

Operations:

Follow the following steps to verify the operation of the IC 7476,

Step.1. The positive transition of the pulse changes the Master FF, and the negative transition changes the Slave FF as well as the output of the circuit.

Step.2. With J = K = 0, the output does not change.

Step.3. With J = K =1, the FF Toggles (or complements).