ADDERS and SUBTRACTORS

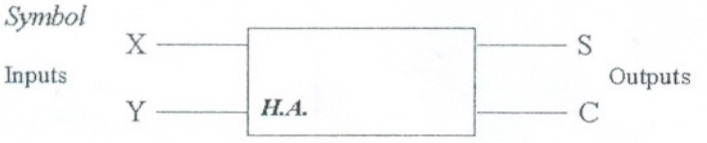
Experiment No. 03

***Aim**: To Implement Adders and Subtractor circuits.*

In this experiment you will construct and test various adders and subtractors circuits.

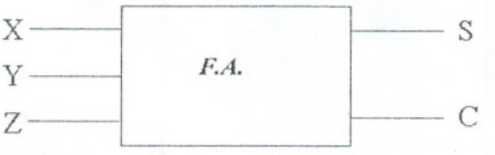
Half Adders: A half adder performs the arithmetic addition of two binary digits. It has two inputs (Augend & Addend) and two outputs (Sum & Carry). The two inputs are the two 1-bit numbers X and Y, and the two outputs are the sum(S) and carry (C).

Logic Symbol



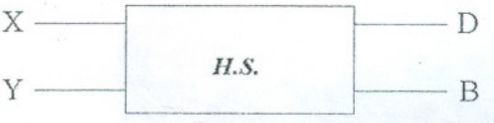
Full-Adders: A full-adder is a combinational circuit that performs the arithmetic sum of three input bits namely Augend-bit(X), addend-bit(Y), and carry-bit from the lower significant position(Z).

Logic Symbol



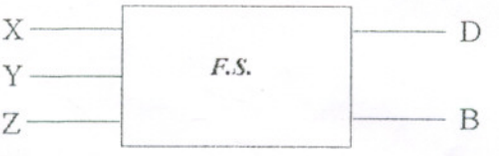
Half-Subtractor: The half-subtractor is and combinational circuit which is used to perform the subtraction operation of two bits. It has two inputs, X(minuend) and Y(subtrahend) and two outputs D(difference) and B(borrow).

Logic symbol



Full-Subtractor: And full subtractor is and combinational circuit that performs the subtraction operation of three bits, namely, X(minuend), Y(subtrahend), and Z(borrow from the previous stage) and produces two outputs D(difference) and B(borrow).

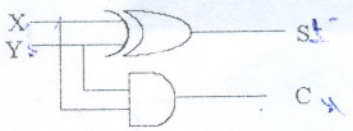
Logic Symbol



Activity.1. Half-Adder

Design, construct and test a half-adder circuit using one XOR gate and one AND gate, only.

Design



Observations

Truth-Table

Inputs		*Outputs*	
X	*Y*	*S*	*C*
0	0		
0	1		
1	0		
1	1		

Write: The switching expressions for Sum (S) = ...

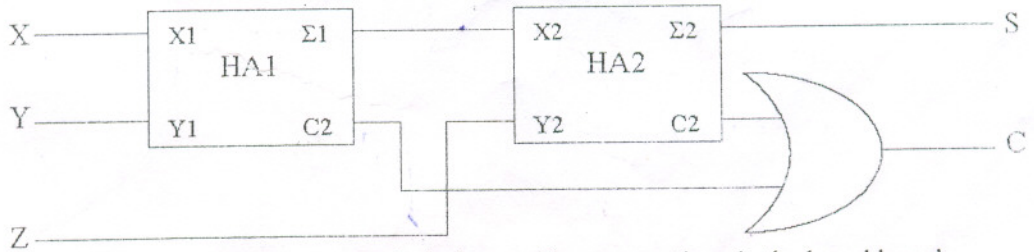
and for Carry(C) = ...

Exercise-1. Design, construct and test and half-adder circuit using five NAND gates, only and verify the truth-table, you made above.

Activity.2. Full-Adder

Design, construct and test a full-adder circuit using two half-adders and one OR gate only.

Design



Get the gate level circuitry you made, before making connections in the bread-board.

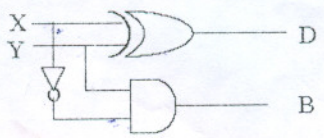
Observations
Truth-Table:

Inputs			*Outputs*	
X	*Y*	*Z*	*S*	*C*
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Write: The switching expressions for Sum (S) = ...
and for Carry(C) = ...

Activity.3. Half-Subtractor
Design, construct and test and half-subtractor circuit using one XOR gate, one AND gate, and one NOT gate only.

Design



Observations
Truth-Table

Inputs		*Outputs*	
X	*Y*	*D*	*B*
0	0		
0	1		
1	0		
1	1		

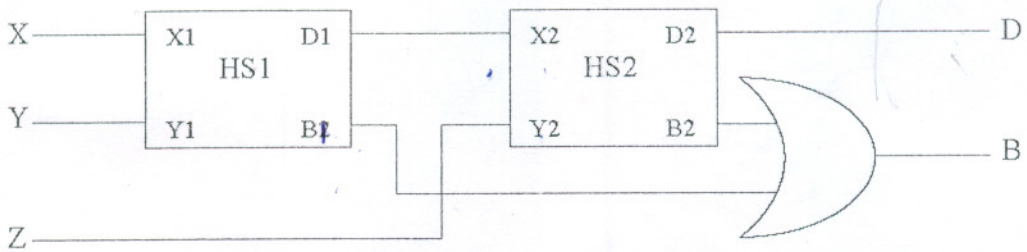
Write: The switching expressions for Difference(D) = ...
and for Borrow (B) = ...

Exercise-2. Design, construct and test and half-subtractor circuit using five NAND gates, only and verify the truth-table, you made above.

Activity.4. Full-Subtractor

Design, construct and test a full-adder circuit using two half-adders and one OR gate only.

Design



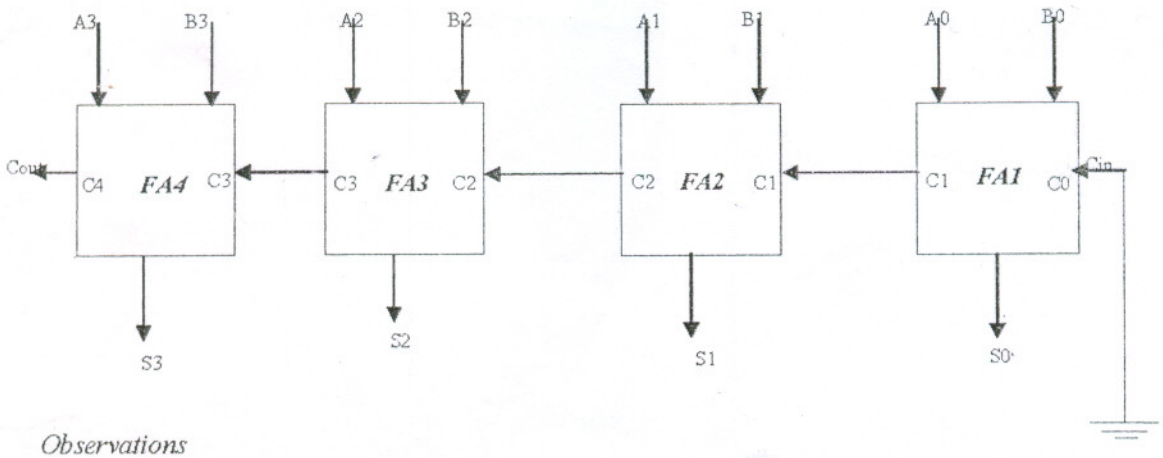
Get the gate level circuitry you made, before making connections in the bread-board.

Observations
Truth-Table:

Inputs			*Outputs*	
X	*Y*	*Z*	*D*	*B*
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Write: The switching expressions for Difference(D) = ...
and for Borrow (B) = ...

Activity.5. 4-bit Parallel-Adder
IC type 7493 is and '4-Bit Binary Parallel Adder'. Its internal construction is shown below:



Observations
Truth-Table

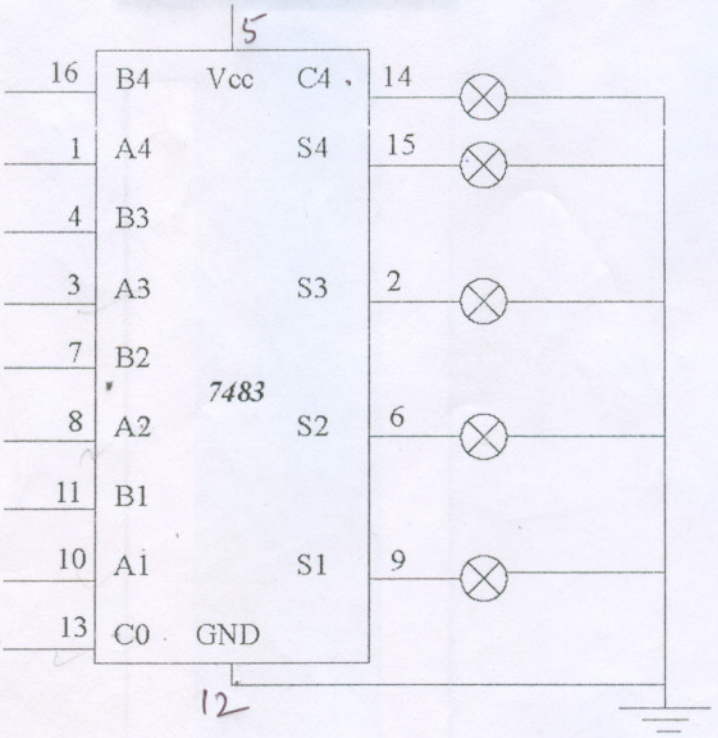
Inputs								*Outputs*				
A4	*A3*	*A2*	*A1*	*B4*	*B3*	*B2*	*B1*	*C4*	*S4*	*S3*	*S2*	*S1*

The two four-bit binary numbers are A1, A2, A3, A4, and B1, B2, B3, B4. The four-bit sum is obtained from S1, S2, S3, S4. Here, C0 is the input carry and C4 is the output carry.

Procedure:
Step.1. Connect the power supply and ground terminals of 4-bit binary adder IC 7483.

Step.2. Connect the four 'A' inputs to a fixed binary number 1101 and the B input and the input carry to the final toggle switches.
Step.3. Apply five outputs to indicator lamps/LEDs.
Step.4. Perform the experiment and records the results.

Pin-out Diagram



Observations

Table.1. When A(A4A3A2A1) = 1001 and C0=0

Inputs				*Outputs*				
B4	*B3*	*B2*	*B1*	*C4*	*S4*	*S3*	*S2*	*S1*
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Table.2. When A(A4A3A2A1) = 1001 and C0=1

Inputs				Outputs				
B4	*B3*	*B2*	*B1*	*C4*	*S4*	*S3*	*S2*	*S1*
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Write the outputs:

1. When A=1010 and B=1110.
   For C0=0, S=..... & For C0=1, S=.....
2. When A=1100 and B=1010
   For C0=0, S=..... & For C0=1, S=.....
3. When A=1011 and B=1111.
   For C0=0, S=..... & For C0=1, S=.....
4. When A=0011 and B=1100.
   For C0=0, S=..... & For C0=1, S=.....

Activity.6. Adder-Subtractor

The subtraction of two binary numbers can be done by taking the 2's complement of the subtrahend and adding it to the minuend. The two's complement can be obtained by taking the 1's complement and adding 1. To perform A-B, we complement the four bits of B, add them to the four bits of A, and add 1 through the input carry.

Procedure:

This is done as the fig. Shown below.

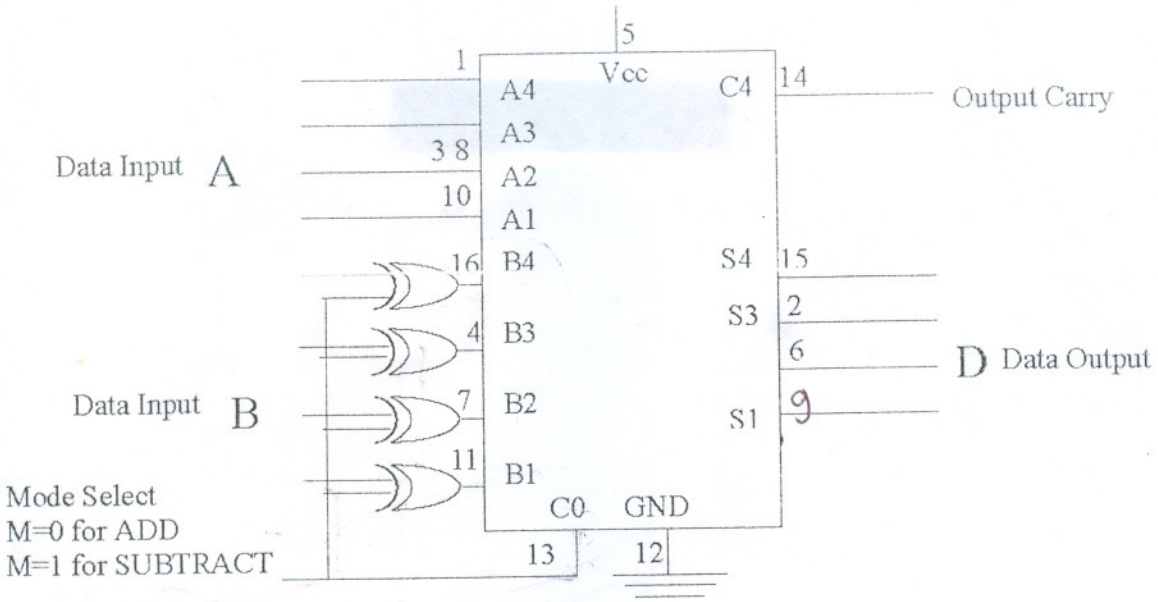
Step.1. When M=1,

The four XOR gates complement the bits of B, since X⊕1=X'. Thus, when M=1, the input carry C0 is equal to 1 and the sum output is A plus 2's complement of B; i.e. the output generated is A-B.

Step.2. When M=0,

The four XOR gates leaves the bits of B unchanged, since X ⊕ 0=X'. Thus, when M=0, the input carry C0 is equal to 0 and the sum output is A plus B; i.e. the output generated is A+B.

Construct the adder-subtractor circuit and test it for proper operation.



Observations

Table.1. When M = 0 and A(A4A3A2A1) = 1001

Inputs				*Outputs*				
B4	*B3*	*B2*	*B1*	*C4*	*S4*	*S3*	*S2*	*S1*
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

By analyzing the truth-table you made above, write:

(i) the name of the operation performed .....

(ii) the output for: 11+5; 15+15; 7+9; 8+15; and 13+4.

Table.2. When M = 1 and A(A4A3A2A1) = 1001

Inputs				*Outputs*				
B4	*B3*	*B2*	*B1*	*C4*	*S4*	*S3*	*S2*	*S1*
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

By analyzing the truth-table you made above, write:

(i) the name of the operation performed .....

(ii) the output for: 11-5; 15-15; 7-9; 8-15; and 13-4.

Inputs								*Outputs*				
A4	*A3*	*A2*	*A1*	*B4*	*B3*	*B2*	*B1*	*C4*	*S4*	*S3*	*S2*	*S1*