Readme

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1 Simulator

1.1 Generation of binaryfile

- Using makefile we can get binaries riscv_sim.a
- To get riscv_sim.a binary file enter the below command in the terminal

  $ make all
- Enter the following command in the terminal for usage of the binary file
  $ ./riscv_sim
- You must keep the input file as "**input.s**".in the same directory as the executable file.

1.2 Files

- **assembler.hh**
  contains all function prototype and global variables used for this application.
- **assembler_implementation.cpp**
  contains definitions of all the functions defined in header file and some initialisation of global variables.
- **main.cpp**
  contains calling of functions of implementation file.
- **cache.cpp**
  contains functions for implementation of cache.
- **Makefile**
  generation of binary files riscv_asm.

1.3 Input and Output

The input is given in "**input.s**" and the output is generated in "input.output" file
In inputfile we give series of instructions and the output is printed in the console itself based on the command.
More details about input format is :

- Cache_sim enable config for loading configuaration file
- load input.s for load input file
- There should be only one instruction in each line
- There should be no blank lines in the input file
- The input starts on the first character in each line
- The input should only contain the risc-v instructions
- The registers can be in x format or u can use aliases.
- there should space between the instruction and register and after each operand there is a comma and after each comma there should be a space.

If any of the above input constraints is failed it outputs the "error program got terminated."