Letters

Low-Power and High-Performance Ternary SRAM Designs With Application to CNTFET Technology

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***Abstract*—This paper presents two efficient ternary SRAM designs appropriate for several transistor-based technologies. The first design is based on the *cycle operator* in ternary logic while the second is a buffer-based design that employs the positive and negative ternary inverters. Both the designs consume low power in comparison to existing standard ternary inverter-based SRAM designs. Further, the read and write delay for the proposed designs are much lower than the corresponding ones for existing designs. Detailed analyses of the proposed circuits are presented. Extensive HSpice simulations (and comparisons) using a Carbon Nanotube Field Effect Transistor library are reported. The proposed designs also have noise margins comparable to existing designs.**

***Index Terms*—Ternary SRAM, low power, low delay, unary operators of multivalued logic, carbon nanotube field effect transistor (CNTFET).**

I. Introduction

IN CONTEMPORARY electronic systems, memory occupies a substantial portion of the system on chip. Low power and high performance SRAM cells are key to portable devices. One approach to low power design of an SRAM is via operation at ultra low voltages. However, this results in sub-threshold conduction and sensitivity to process-voltage-temperature variations [1]. Another approach is by moving beyond binary. Several device technologies support ternary logic.

A ternary SRAM cell stores three-valued data (namely, '0,' '1' and '2'). A simple solution for a ternary SRAM is via a pair of standard ternary inverters in the loop to store the information. CMOS-based ternary sequential circuits have been reported as early as 1976 [2]. A ternary memory circuit in CMOS has also been described [3]. Recently, enhancements to the classical CMOS ternary SRAM memory cell have been reported in [4] by employing various width and length ratios. Alternatives to CMOS such as the Carbon Nanotube Field Effect Transistor (CNTFET) offer interesting features. In particular, the threshold voltage of a CNTFET depends just on the diameter of the CNT [5]. This property has been used to design ternary arithmetic circuits [6]. Ternary SRAM designs in CNTFET technology have also been proposed [7]–[10].

In this paper, we present two efficient SRAM designs (with application to CNTFET technology) taking advantage of unary operators of multivalued logic [11]. The judicious selection of unary operators has a direct consequence on obtaining low-power and high-performance ternary SRAM designs. In particular, our first design is based on the *cycle operators* (shown in Table I). With cycle operators, the feedback loop is closed only when the data written is complete (else the loop remains open). Hence, changes that occur in the input data during write do not get stored in the loop. Existing ternary SRAM designs [7]–[10] are typically based on the standard ternary inverter (STI). A ternary buffer implemented with STIs, in general, has a high probability of switching (in comparison to the cycle operator) from V_{dd} to/from Gnd leading to full swing charge and discharge at the output.

We then present a second low-power SRAM design based on a ternary buffer realized via positive ternary inverter (PTI) and negative ternary inverter (NTI) (see Table II). The buffer stores the data without switching. Both the proposed designs also incur low delay in comparison to existing designs [8], [12]. In particular, the cycle operator-based design offers delay advantage due

TABLE I
CYCLE OPERATORS FOR TERNARY LOGIC

Input	Cycle	
A	A^1	A^2
0	1	2
1	2	0
2	0	1

TABLE II
$\overline{A}$, A_P AND A_N DENOTE STI, PTI AND NTI RESPECTIVELY

Input	Inverters		
A	$\overline{A}$	A_P	A_N
0	2	2	2
1	1	2	0
2	0	0	0

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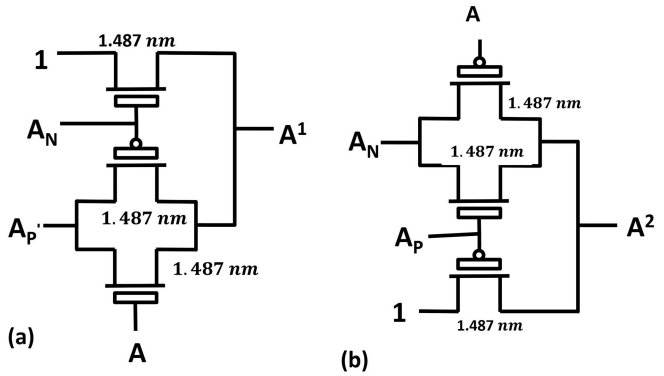

Fig. 1. CNTFET-based circuit for cycle operators (a) A^1 and (b)A^2.

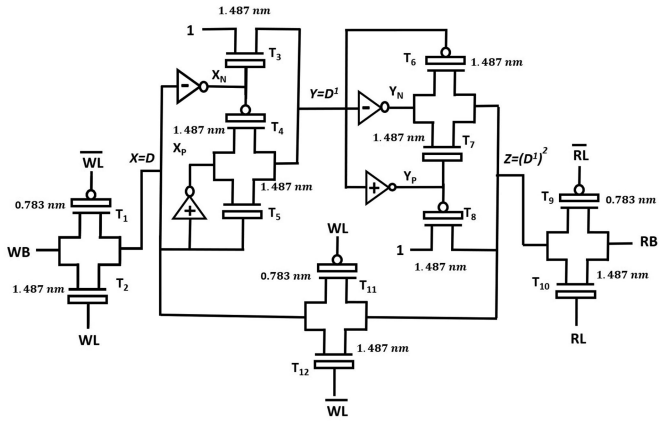

Fig. 2. CNTFET-based circuit for ternary SRAM using cycle operators.

to a pass transistor-based realization while the ternary buffer (using PTI and NTI) is a single stage circuit. Additional details are provided in sections II and III.

Extensive HSpice simulations have also been performed using the CNTFET-model in [13]. *Reading* into the proposed cycle operator-based SRAM takes 14% of the power consumed by [12] (and 18% of the best design in [7]). Further, *reading* into the proposed buffer-based ternary SRAM takes only 19% of the power consumed by [12] (and 24% of the best design in [7]). Write operations also consume lower power with the proposed approaches. Further, the average *read* delay for the two proposed approaches is about 40% of the delay in [8] and 25% of the delay in [12]. The average *write* delay for the first approach is about 30% of the one in [8] and [12] while for the second approach, it is roughly 60% of the delay in [8] and [12]. The write delay of the proposed cycle operator- based SRAM is 19% and buffer-based SRAM is 37% of the recent SRAM design in [10]. Further, the noise margins for the proposed designs are comparable to the existing STI-based designs in [9], [12]. The proposed SRAM designs also have low area overhead in comparison to the designs in [9] and [10]. Additional details are presented in section IV.

II. Proposed Ternary SRAM Design Using the Cycle Operators

As indicated in Table I, there are two cycle operators, A^1 and A^2, for a given ternary input A. The CNTFET realization of these cycle operators is shown in Fig. 1.

The proposed ternary SRAM cell using the cycle operator is shown in Fig. 2. The design stores the ternary digit in the feedback loop formed with two cycle operators and a transmission gate as shown in Fig. 2. The operation of the proposed ternary SRAM circuit is as follows. The writing operations start when WL is high. The data D from the WB line is passed onto the transmission gate pair $T_1 - T_2$ and stored at node X. Then, the first cycle operator circuit composed of transistors $T_3 - T_4 - T_5$ forces the node Y with D^1. Later, the second cycle operator with transistors $T_6 - T_7 - T_8$ results in the output of $(D^1)^2$ at Z. The combination of D^1 followed by D^2 works as a buffer as shown in (1). This cycle operator pair stores the data in the loop when WL is low by switching ON the transmission gate pair $T_{11} - T_{12}$. When WL is low and RL is low, the circuit is in hold mode and stores the data continuously by running the two cycle operator circuits in the loop. Here, the data will be stored in the loop only when WL is low, hence the unwanted changes occurring in the data D when WL is high will not be stored in the loop. The reading operation starts when RL is high. The data stored in the loop is passed into the transmission gate $T_9 - T_{10}$ to the line RB. The design can be altered by using A^2 followed by A^1 in the feedback loop.

TABLE III
Write Delay (ps) of Various Ternary SRAM Cells; Transition $0 \rightarrow 1$ Refers to Writing a '1' When Previous Data is '0'

Write Data	Design [8]	Design [12]	Design [10]	Proposed Cycle operator -based TSRAM	Proposed Buffer -based TSRAM
$0 \rightarrow 1$	113.1	81.55	114.4	15.15	20.01
$1 \rightarrow 2$	5.852	21.28	107.98	11.22	38.45
$2 \rightarrow 1$	95.91	76.36	148.23	13.57	34.95
$1 \rightarrow 0$	7.185	17.29	23.97	12.68	18.62
$0 \rightarrow 2$	20.64	45.17	22.17	15.04	30.47
$2 \rightarrow 0$	10.90	40.36	20.76	14.21	20.35
Avg.	42.26	47.01	72.91	13.65	27.15

$$A = (A^1)^2 = (A^2)^1 \tag{1}$$

Remark 1: A buffer implemented with STI uses two inverters. Hence, ternary logic '0' is inverted to logic '2' by the first inverter and then converted to logic '0' using the second inverter. On the other hand, the cycle operator converts logic '0' to '1' using A^1 and from logic '1' to '0' using A^2. As a result, the probability of switching from 0 to V_{DD} (i.e. logic '2') is more in case of STI. Charging or discharging from 0 to V_{DD} draws more current (than 0 to $\frac{V_{DD}}{2}$ or from $\frac{V_{DD}}{2}$ to V_{DD}). Hence, the cycle operator-based design consumes less power. Additional power savings are obtained by introduction of a transmission gate in the feedback loop to mitigate the possibility of a noise signal storage in the SRAM cell. Numerical data on savings is presented in Table V.

Remark 2: The proposed ternary SRAM cell is implemented in pass transistor logic. This implementation takes less delay for write and read operations compared with an STI-based SRAM design [8], [12], since the latter uses CMOS style of implementation for the STI. Numerical data is presented in Tables III and IV.

TABLE IV
READ DELAY (ps) OF VARIOUS TERNARY SRAM MEMORY CELLS

Read Data	Design [8]	Design [12]	Design [10]	Proposed Cycle operator -based TSRAM	Proposed Buffer -based TSRAM
'0'	127.6	159.40	101.6	35.1	38.5
'1'	39	63.41	177.22	37.5	40.5
'2'	135.3	282.11	179.7	39.5	41.6
Avg.	100.63	168.31	152.84	37.37	40.16

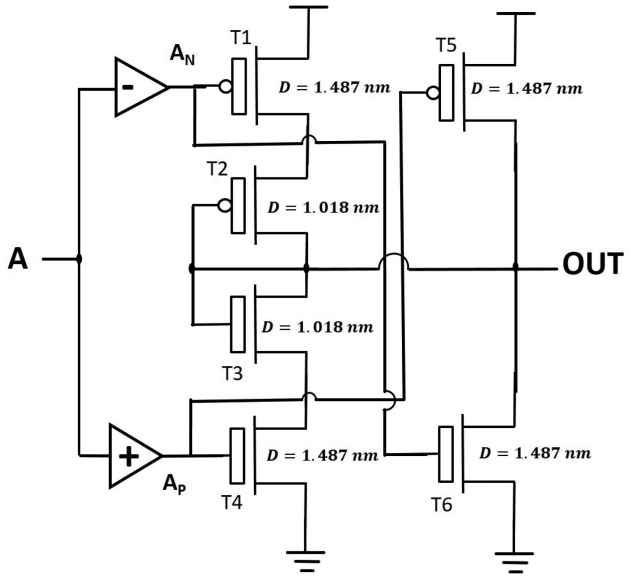

Fig. 3. CNTFET-based circuit for ternary buffer using PTI and NTI.

III. PROPOSED BUFFER-BASED TERNARY SRAM DESIGN

In this section, we present the second design based on the positive ternary inverter (PTI) and the negative ternary inverter (NTI). Fig. 3 depicts the key component of this design, namely the buffer circuit. The circuit operates as follows. When A='0,' the output of the inverters A_P = '2' and A_N = '2'. This results in transistor T6 alone switching ON while all other transistors remain OFF. This results in a path from output to Gnd which corresponds to an output of logic '0'. The operation of the circuit is similar for other inputs.

The next step utilizes the buffer (Fig. 3) to realize the ternary SRAM. This is shown in Fig. 4. The write operation takes place when WL is high. The data D on the WB line is passed to node X through the transmission gate pair $T_1 - T_2$. Then, the buffer forces the output at node Y to be the same as data D. When WL is low, the transmission gate pair $T_9 - T_{10}$ is ON and hence stores the data continuously in the loop. When RL is high, the data from node Y can be read into the line RB through the transmission gate pair $T_{11} - T_{12}$.

Remark 3: The proposed circuit (Fig. 4) stores the data without any switching and hence leads to reduced power consumption during write, read and hold operations. The read and write power of the buffer-based SRAM design are given in Table V.

Remark 4: The proposed buffer-based ternary SRAM has reduced read and write delay in comparison to an STI-based design [8], [12] and this can be attributed to the fact that the buffer in the former is a single stage circuit, while the STI-based buffer is a two stage circuit. Numerical values for the delays are shown in Tables III and IV.

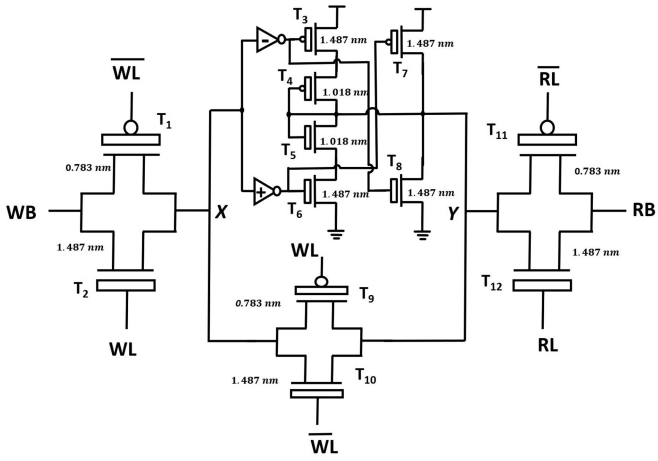

Fig. 4. CNTFET-based circuit for proposed SRAM using ternary buffer.

TABLE V
READ AND WRITE POWER OF VARIOUS TERNARY SRAM CELLS

Logic	3T-STI SRAM [7]	6T-STI SRAM [7]	STI SRAM [12]	STI SRAM [10]	Proposed Cycle Operator SRAM	Proposed Buffer -based SRAM
Write Power(μW)						
'0'	2.58	0.44	0.854	0.648	0.649	0.874
'1'	1.49	1.44	0.752	0.828	0.695	0.434
'2'	2.58	0.44	0.851	0.337	0.701	0.864
Avg.	2.21	0.77	0.819	0.605	0.682	0.724
Read Power(μW)						
'0'	2.47	0.24	0.026	0.153	0.185	0.03
'1'	0.03	1.96	0.621	0.892	0.091	0.091
'2'	2.47	0.24	2.400	0.114	0.165	0.467
Avg.	1.65	0.814	1.016	0.386	0.147	0.196

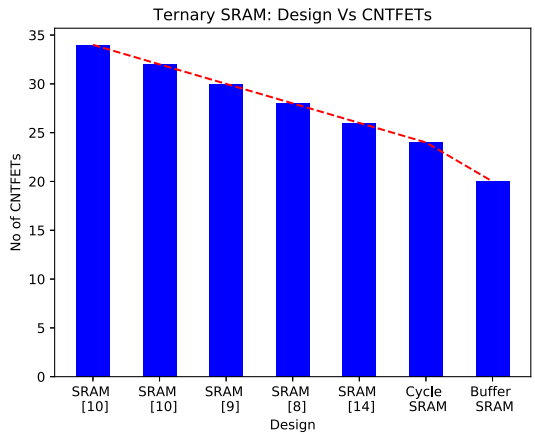

Fig. 5. Comparison of number of CNTFETs required for Various Ternary SRAMs.

The proposed SRAM cells compare favorably with prior designs in terms of area overhead as shown in Fig. 5. In particular, the transistor counts for the proposed designs and two prior designs are given in Remark 5.

Remark 5: The proposed cycle operator-based SRAM takes 24 CNFETs while the buffer-based SRAM takes 20 CNFETs. The SRAM design in [9] takes 30 CNTFETs while the SRAM

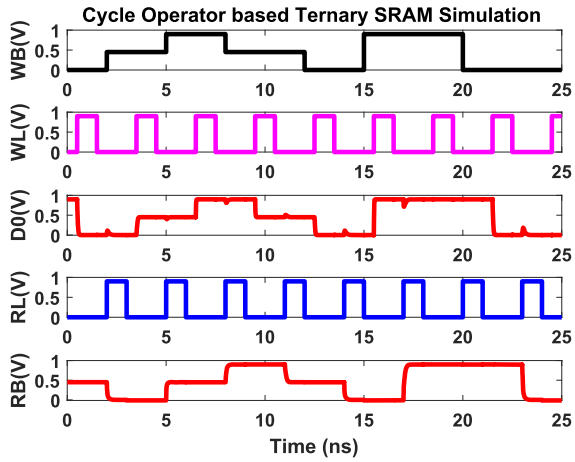

Fig. 6. Cycle Operator-based Ternary SRAM Simulations.

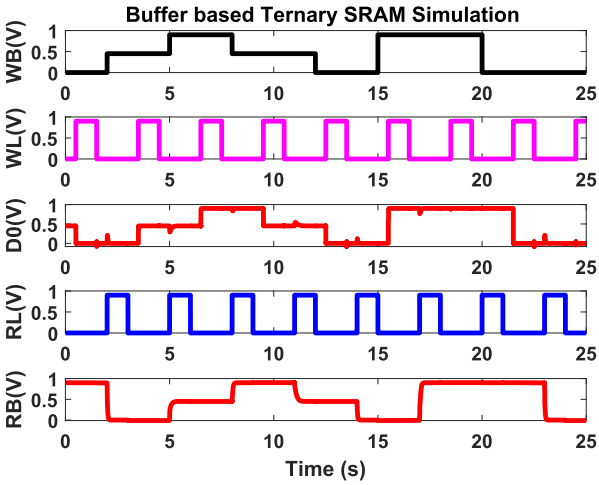

Fig. 7. Buffer-based Ternary SRAM Simulations.

designs in [10] take 32 and 34 CNTFETs respectively. It is worth noting that in STI-based ternary SRAMs, the data is read as $\overline{D}$ and an additional standard ternary inverter is required to get D.

IV. Simulation Results and Comparisons

The proposed ternary SRAM cells have been simulated in Synopsys HSpice using CNTFET-model [13]. This model developed for single-walled CNTFETs is applicable to a wide range of chiralities. The operating voltage for our study is 0.9 V while the channel length is 32 nm. Further, the drive strength is maintained at 1 fF for all the circuits. Figures 6 and 7 show the simulations of the cycle operator-based ternary SRAM and buffer-based ternary SRAM designs respectively.

The write delay and read delay of various SRAM cells are reported in Tables III and IV respectively. The proposed SRAM cells are compared with two existing ternary SRAM cells (with CNTFET realization) reported in [8] and [12]. It can be observed that both the proposed designs have much smaller read and write delay in comparison to [8] and [12].

Table V gives the power required to write and read various ternary logic levels to the proposed memory cells. It can be observed that the power requirements are much less for both

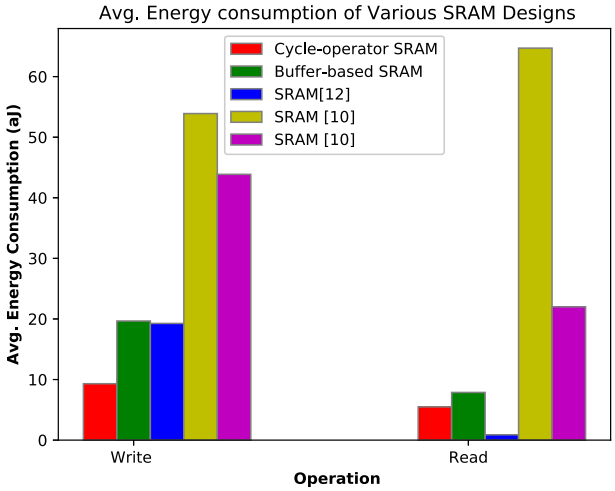

Fig. 8. Average Energy for Various Ternary SRAM designs.

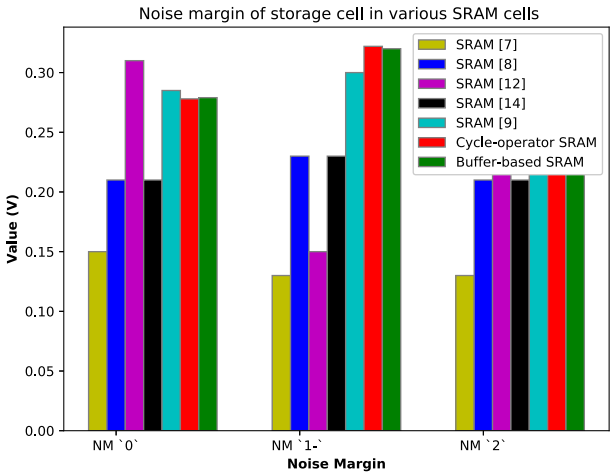

Fig. 9. Static Noise Margin of storage cell in various CNTFET-based ternary SRAM memory cells.

the proposed designs in comparison to [12] and 3T-STI of [7]. The power values are comparable to the 6T-STI design in [7]. Bar charts showing the read and write energy for various ternary SRAM memory cells are presented in Fig. 8. The proposed cycle operator-based SRAM as well as the proposed buffer-based SRAM consume significantly less energy in comparison to the SRAM design in [8]. The energy consumption of the proposed methods is comparable to that of the SRAM design in [12].

The static noise margin for the proposed ternary SRAMs is calculated by considering the storage circuit unit of each SRAM cell. A noise source is considered as the input of the buffer circuits in the feedback loop. Fig. 9 gives the noise margin of the proposed SRAM cells as well as the inverter-based designs in [12], [14] and recent SRAM design [9]. The proposed designs have better noise margin in comparison to the SRAM0 design in [8] (since from Fig. 9, we observe that NM0 - NM1+ = 0.2 for SRAM0 while it is 0.04 for the proposed designs) while it is comparable to the SRAM1 design in [12].

Remark 6 gives the influence of process variations on the performance of the SRAM design.

TABLE VI
RESULTS OF MONTE-CARLO SIMULATIONS (WITH RESPECT TO POWER) CONSIDERING VARIATIONS IN D_{CNT}, L_{ch} AND V_{DD}

Cycle Operator-based SRAM				
Variation	Mean (μW)	Std. Deviation(μW)	Max. Power (μW)	Min. Power (μW)
D_{CNT}	0.863	6.566 m	0.869	0.855
L_{ch}	0.851	0.415 m	0.851	0.849
V_{DD}	0.886	69.5 m	0.988	0.821
Ternary Buffer-based SRAM				
Variation	Mean (μW)	Std. Deviation(μW)	Max. Power (μW)	Min. Power (μW)
D_{CNT}	1.26	0.205 m	1.291	1.245
L_{ch}	1.32	0.337m	1.321	1.321
V_{DD}	1.28	0.1483	1.467	1.128

TABLE VII
RESULTS OF MONTE-CARLO SIMULATIONS (WITH RESPECT TO DELAY) CONSIDERING VARIATIONS IN D_{CNT}, L_{ch} AND V_{DD}

Cycle Operator-based SRAM				
Variation	Mean (ps)	Std. Deviation (ps)	Max. Delay (ps)	Min. Delay (ps)
D_{CNT}	45.1	1.173	47.05	43.65
L_{ch}	69.0	0.848	70.3	68.12
V_{DD}	44.3	6.19	50.8	37.8
Ternary Buffer-based SRAM				
Variation	Mean (ps)	Std. Deviation(ps)	Max. Delay (ps)	Min. Delay (ps)
D_{CNT}	54.35	2.895	57.78	49.4
L_{ch}	80.06	0.843	81.31	78.74
V_{DD}	52.9	18.6	73.3	53.2

Remark 6: Monte-Carlo simulations have been performed in Synopsys HSPICE considering variations in CNT-diameter (D_{CNT}) and channel length (L_{ch}) to estimate the influence of the process variations on the SRAM design. The CNTFET parameter variations in [15] are considered for the Monte-Carlo simulations and a Gaussian distribution is assumed as in [15]. The results from the simulations are given in Tables VI and VII for average power consumption and worst-case delay respectively. It can be observed that variations in channel length (L_{ch}), diameter (D_{CNT}) and power supply (V_{DD}) do not have significant influence on the average power consumption and worst-case delay.

V. CONCLUSION

We have presented two low power and high performance ternary SRAM designs in this paper. One of the designs is based on the cycle operator in ternary logic while the other is a buffer-based design. The proposed ternary SRAM cell can be used as a ternary memory cell without any structural modifications. Further, our designs compare favorably with existing (and recent) designs in terms of area overhead. In addition, Monte-Carlo simulations reveal that the performance of the proposed designs does not degrade with variations in channel length, CNT diameter and operating voltage.

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