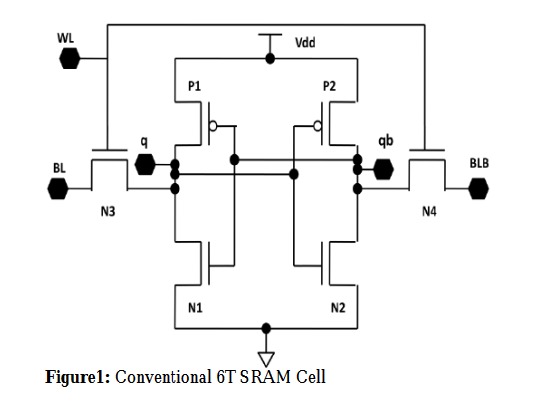
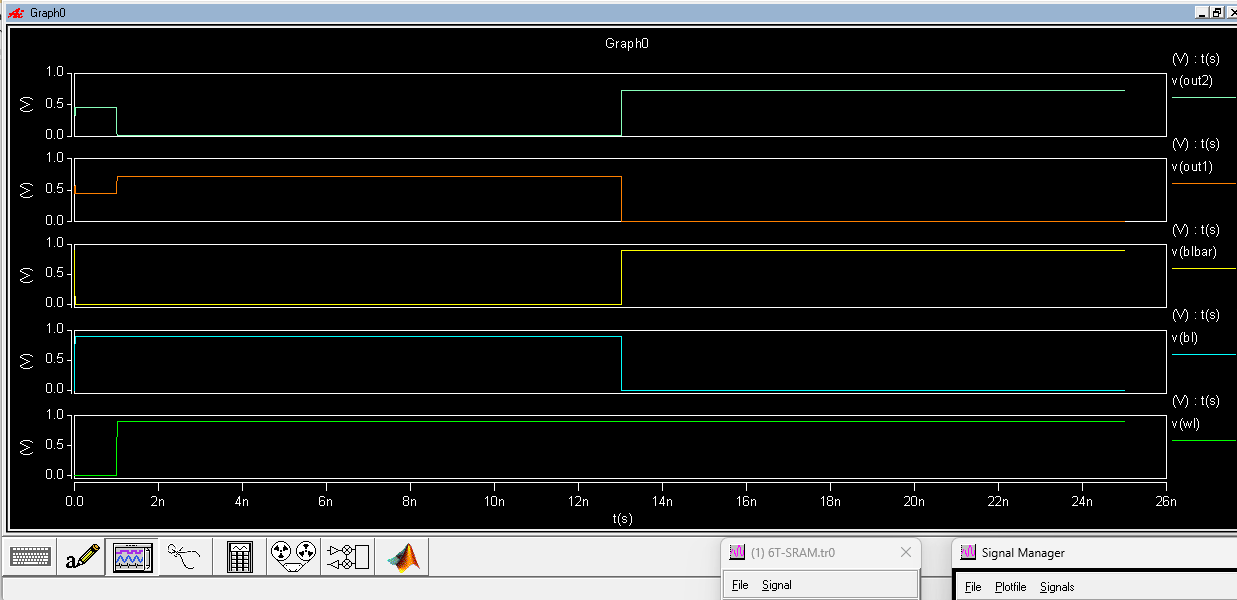
Abstract

Designed SRAM using MOSFET (6T SRAM,8T SRAM), Cycle Operator, Buffer using CNTFET AND GNRFET technology. Generally SRAM is volatile in nature to make it non volatile SRAM designed is using RRAM.

INTRODUCTION:

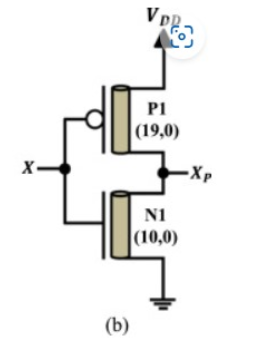
SRAM USING 6T MOSFET:

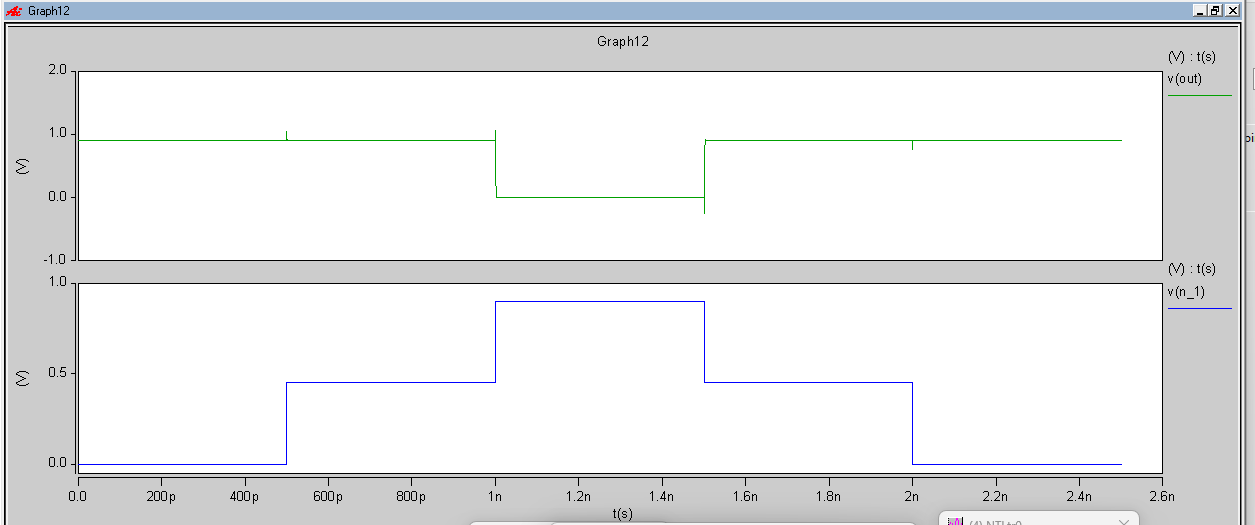


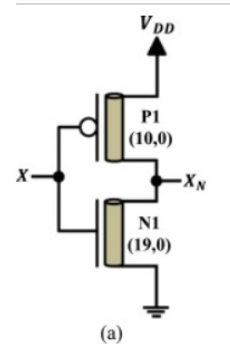


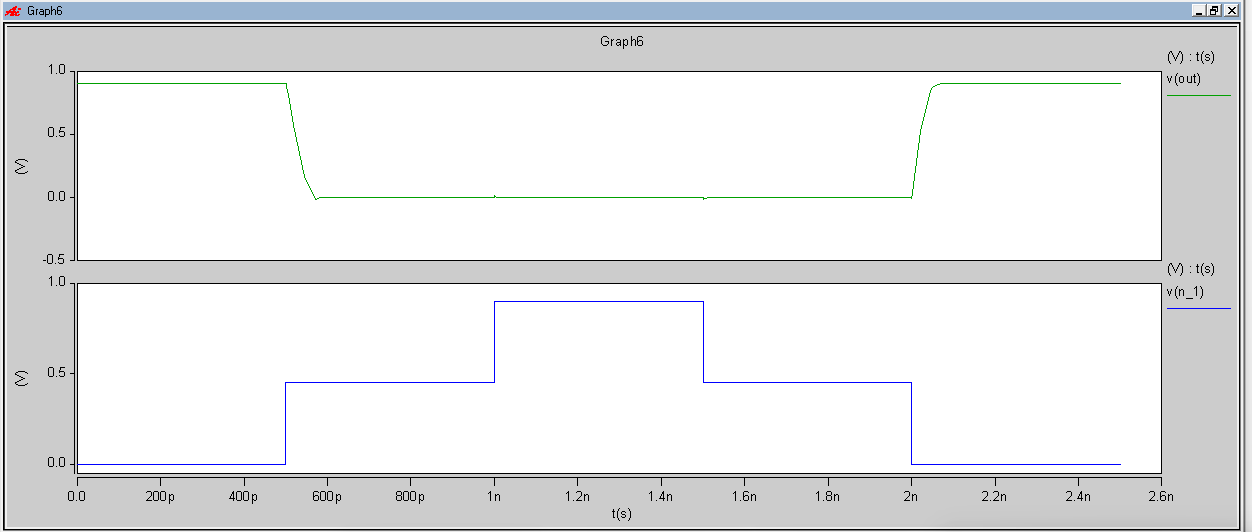
CNTFET:

PTI:

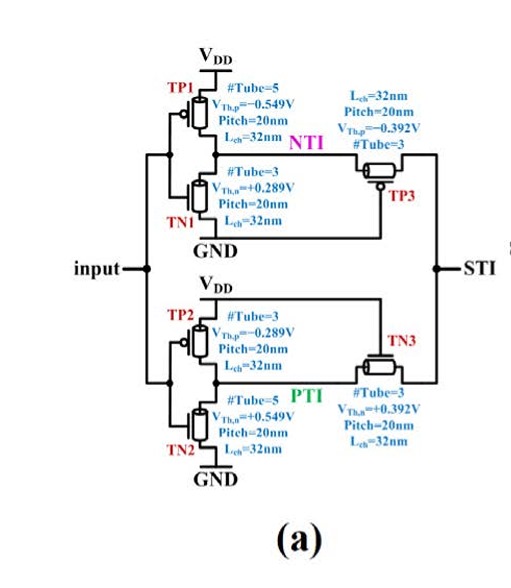


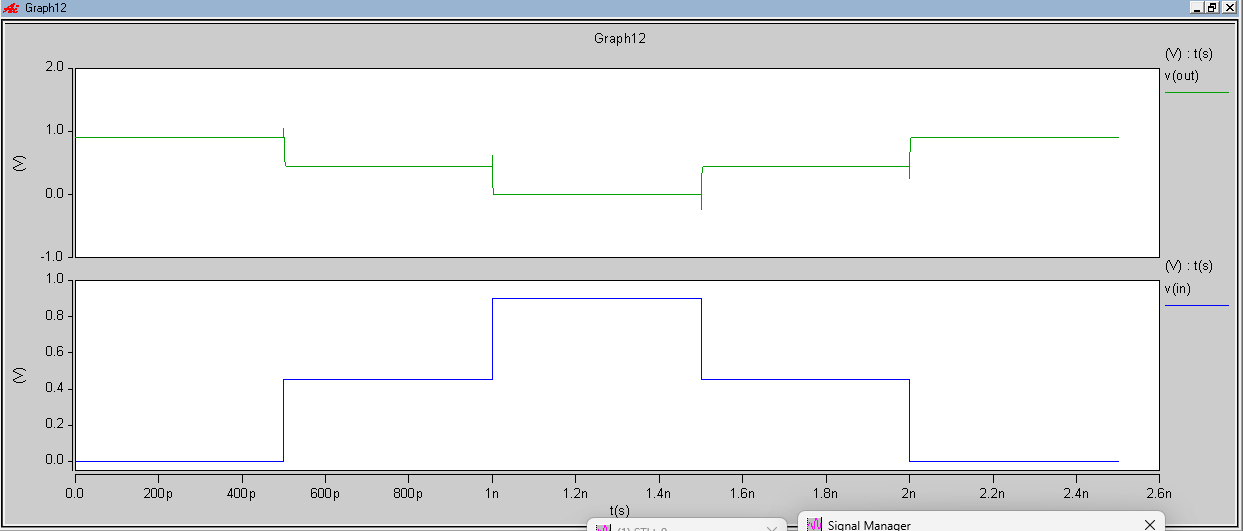
  
NTI:

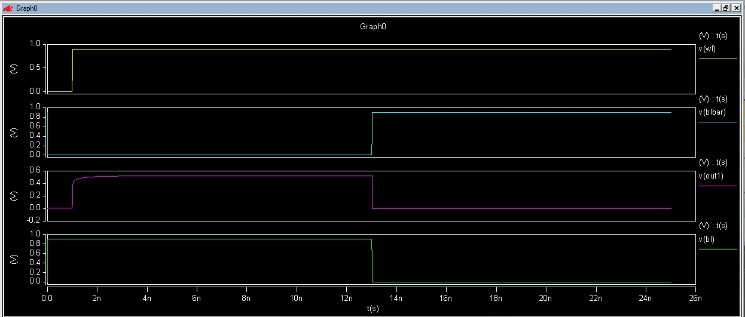




STI:





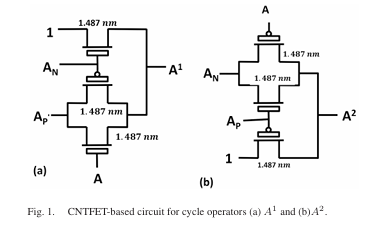
6T SRAM using CNTFET:  


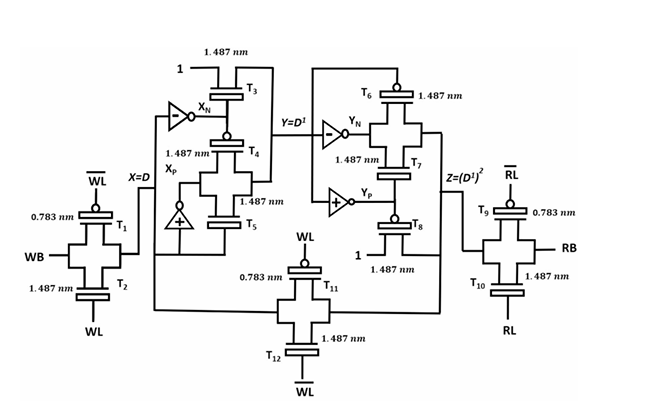
SRAM USING CYCLE OPERATOR:

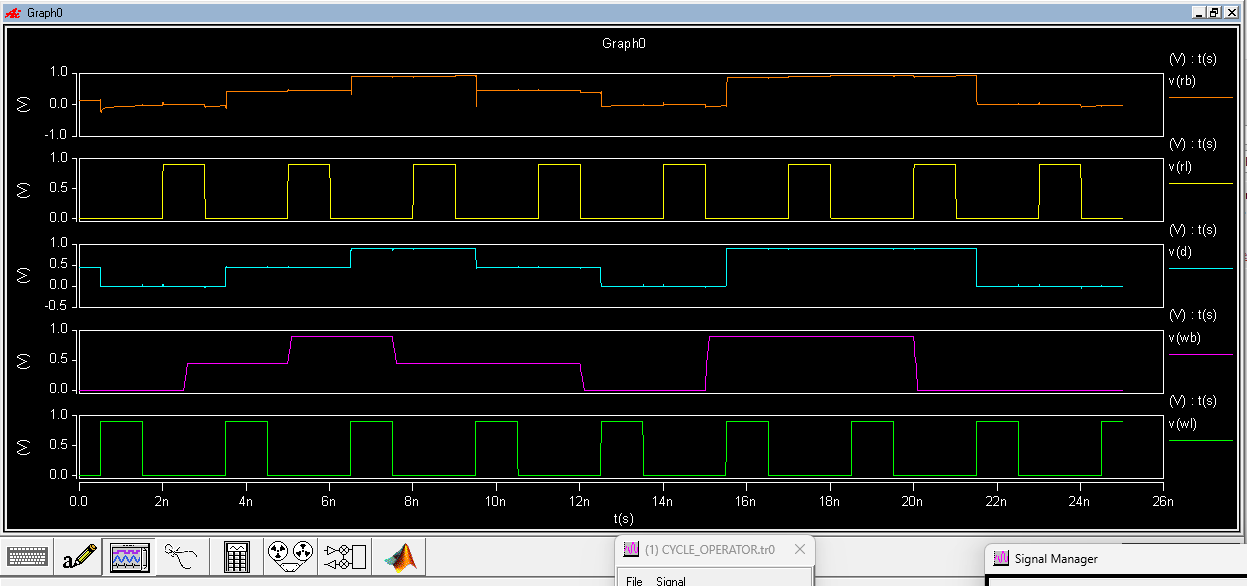
* Cycle operators (A1 and A2) perform transformations within a feedback loop to stabilize the ternary data (0, 1, 2).
* **Design Architecture:**
  + Two cycle operator circuits for data manipulation. Cycle operators (A1 and A2) perform transformations within a feedback loop to stabilize the ternary data (0, 1, 2).
  + Transmission gates for data input/output control.
* **Advantages:**

Prevents the storage of transient or unwanted signals during the write phase.

* **Write and Read Operation:**
  + WL (Write Line) is high, allowing data to pass into the transmission gate.
  + Data is stored using cycle operator feedback.
  + RL (Read Line) is high, allowing stored data to be output without affecting power efficiency







SRAM USING BUFFER

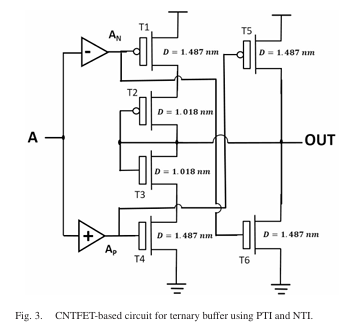
* **Advantages:**

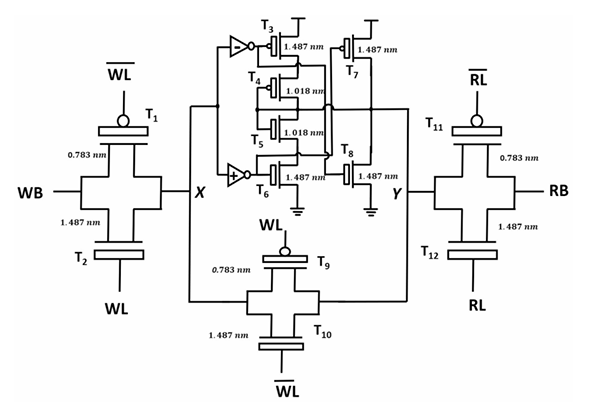
Prevents the storage of transient or unwanted signals during the write phase.

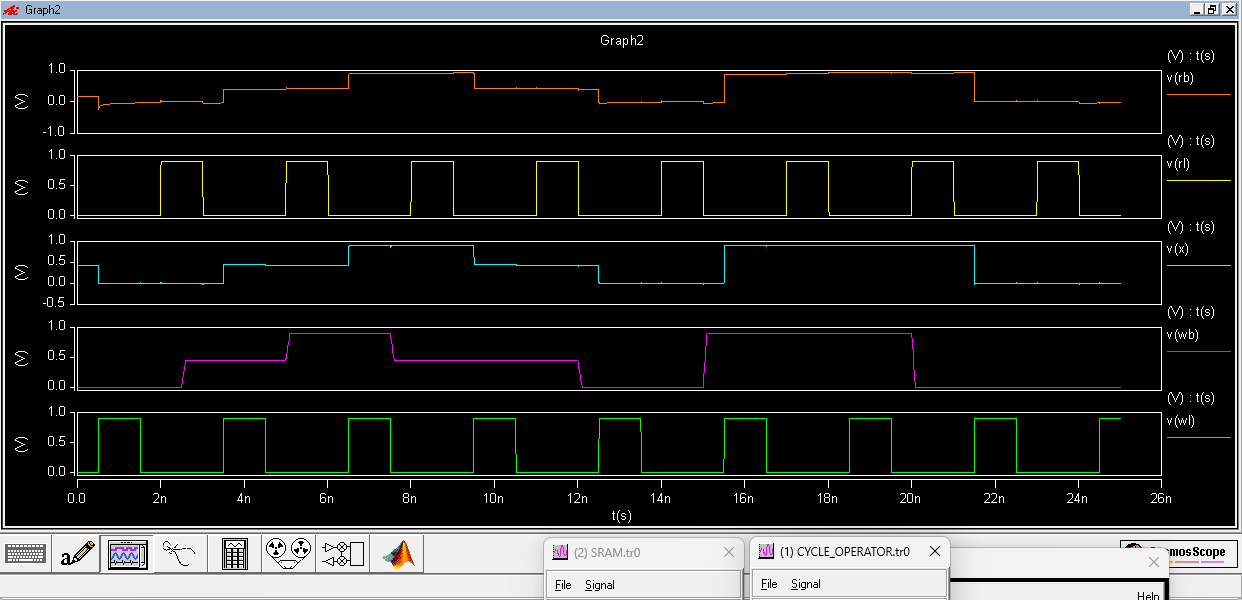
* **Write and Read Operation:**
  + WL (Write Line) is high, allowing data to pass into the transmission gate.
  + Data is stored using cycle operator feedback.
  + RL (Read Line) is high, allowing stored data to be output without affecting power efficiency
* **Advantages:**

Stores data without intermediate state changes, minimizing dynamic

* **Write Operation:**
  + WL is high, allowing the data to pass through the transmission gates and into the buffer.
* **Read Operation:**
  + RL is high, and data is retrieved from the buffer without additional switching.

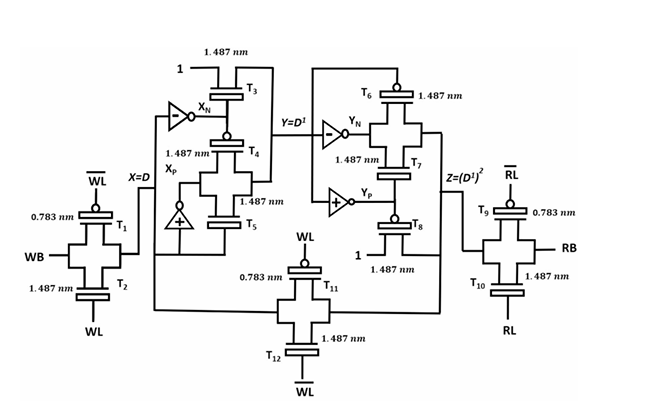


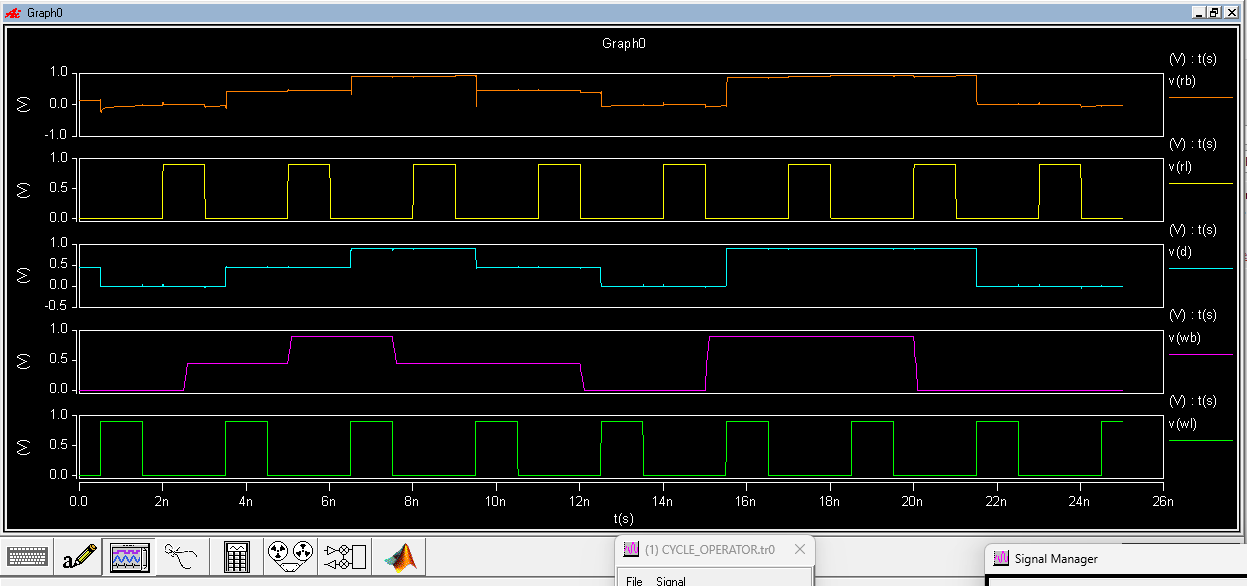




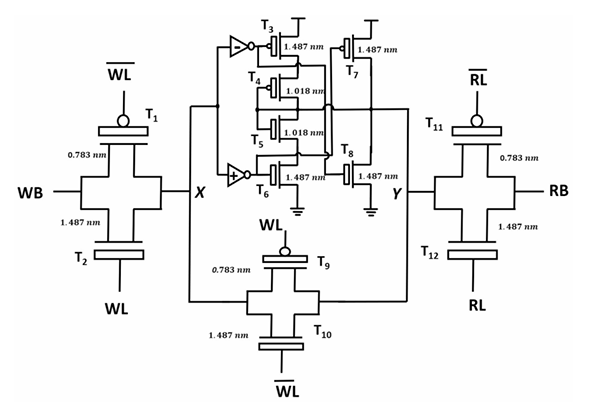
GNRFET:

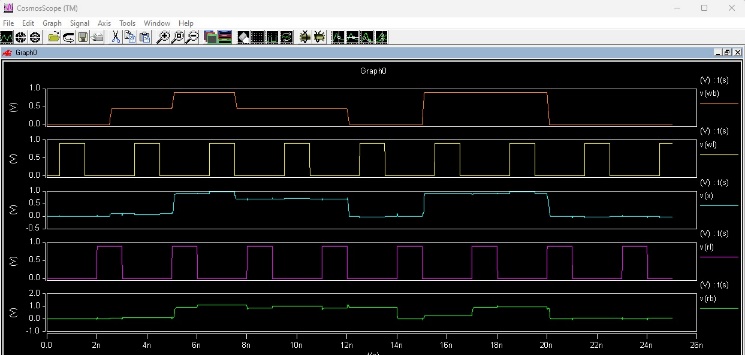
SRAM USING CYCLE OPERATOR:



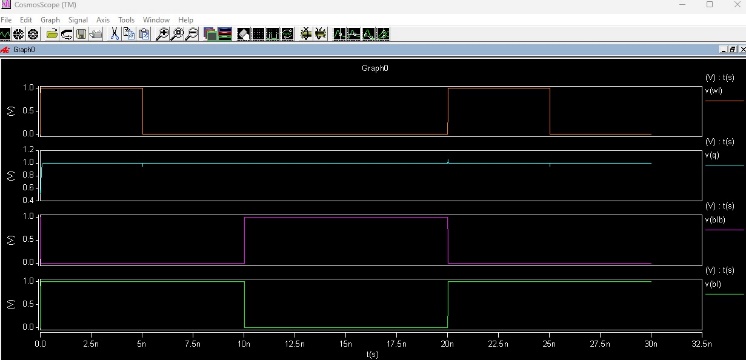


SRAM USING BUFFER:

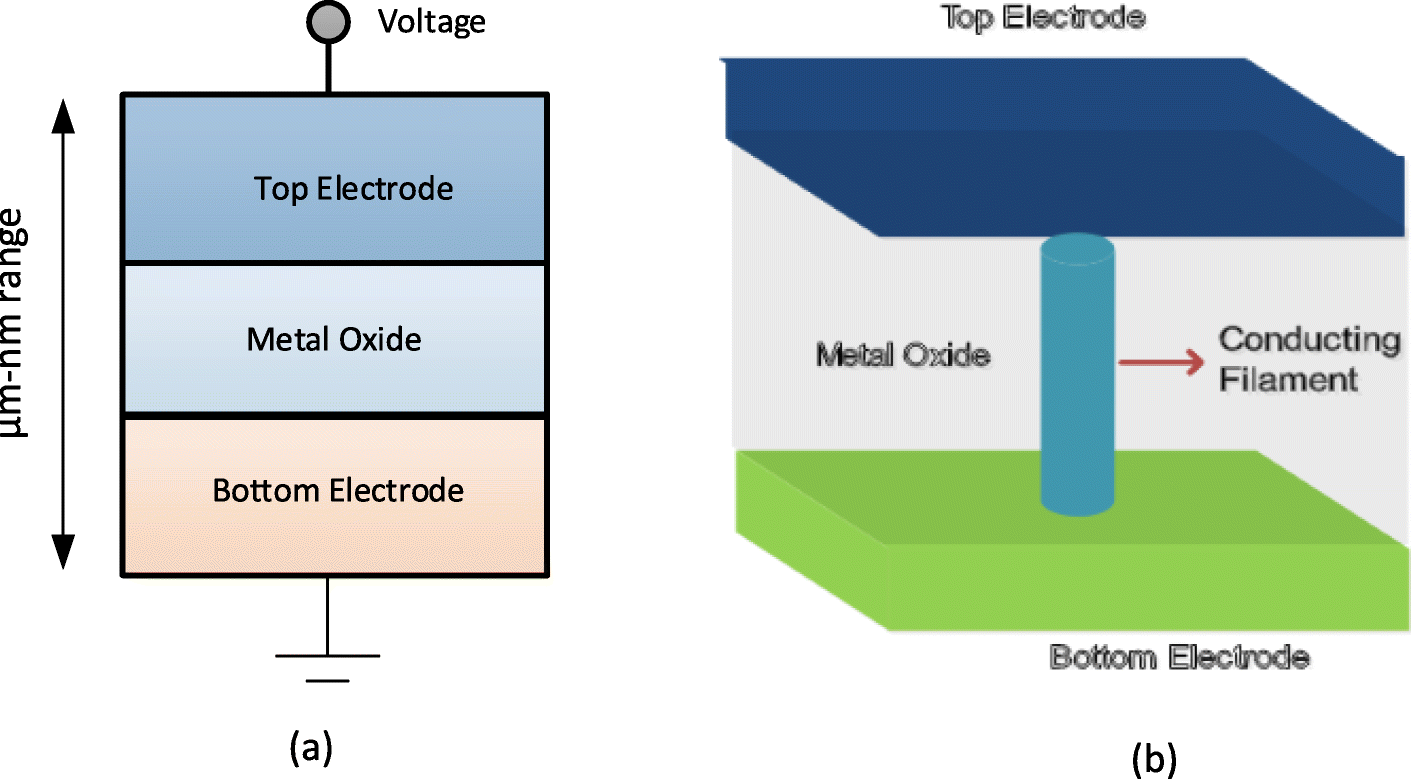




6T SRAM using GNRFET:



RRAM:



* RRAM has a Metal-Insulator-Metal (MIM) structure, where the insulator layer is positioned between two metal electrodes.
* Common materials for the switching layer include HfO₂, TiO₂, Al₂O₃, or Ta₂O₅, which enable resistive switching through the formation and rupture of conductive filaments.
* The top and bottom electrodes are typically made of Pt, Ti, TiN, W, or Cu, ensuring stable electrical contact and interaction with the insulating layer.
* Metal oxides are selected for their CNTFET compatibility, scalability, and reliable switching, while noble and refractory metals like Pt excellent conductivity and chemical stability at nanoscale.
* **RRAM** is a memory device that switches between two resistance states:

**HRS (High Resistance State):** Represents "OFF" or 0.

**LRS (Low Resistance State):** Represents "ON" or 1.

* **Switching Mechanisms:**

**SET Operation:** Transitions from HRS to LRS

(conductive state).

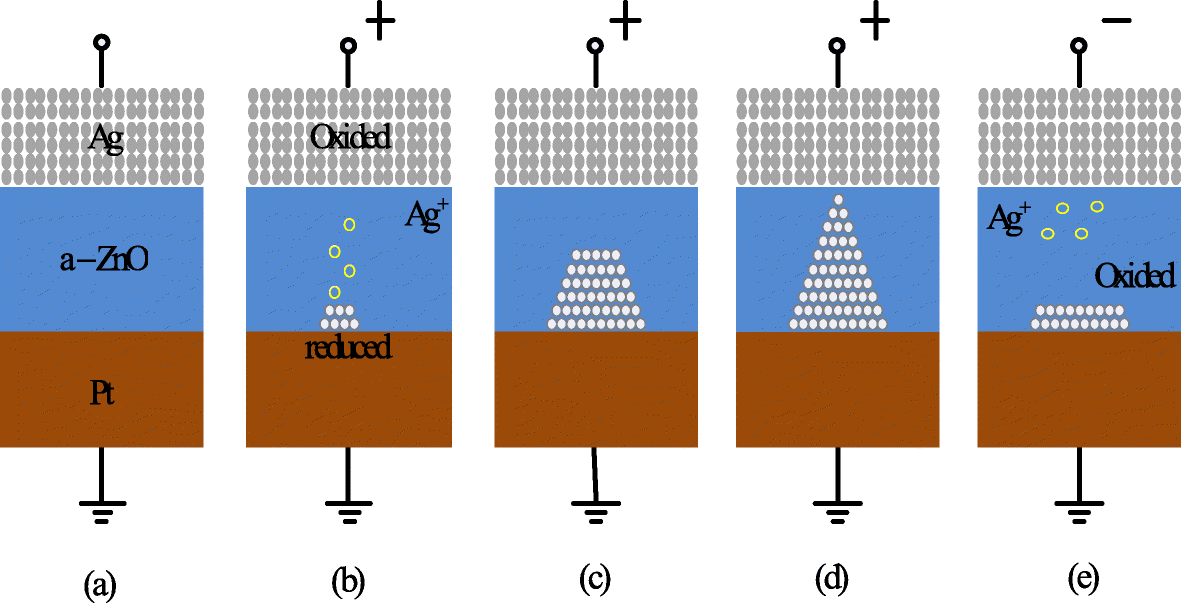
**RESET Operation:** Transitions from LRS to HRS

(non-conductive state).

* **Switching Types:**

**Unipolar:** Same polarity for SET and RESET.

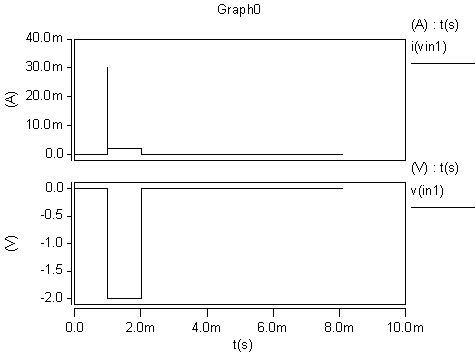
**Bipolar:** Opposite polarity for SET and RESET.



HRS:the gap between the electrodes are high

**HRS initial: set (standard mode)**

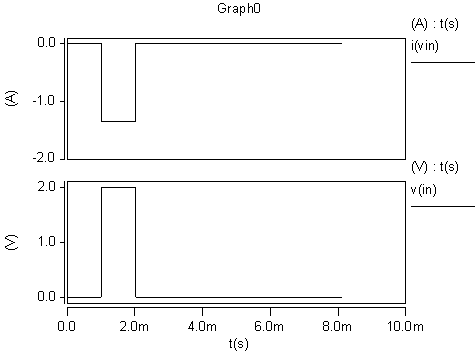
**X3 in 0 rram\_v\_1\_0\_0 gap\_ini = 19e-10 model\_switch = 0 deltaGap0 = 1e-4**



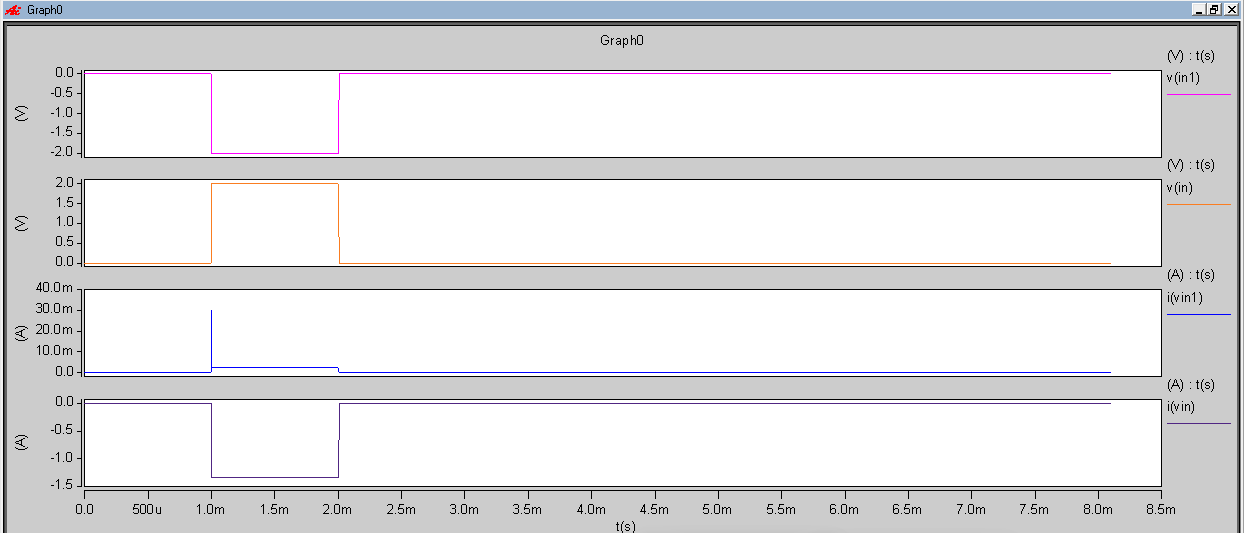
LRS:the gap between the electrodes are less

**\* LRS initial: reset (standard mode)**

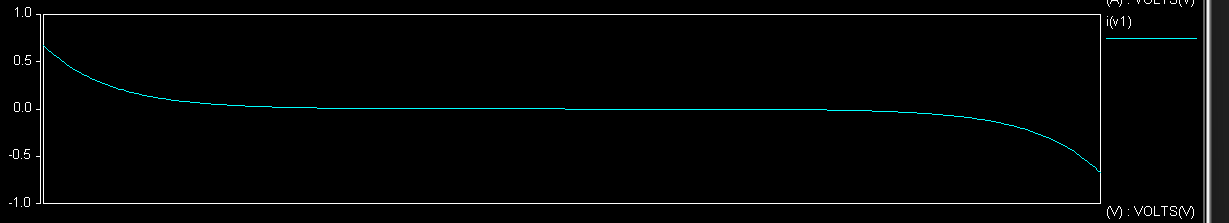
**X4 in1 0 rram\_v\_1\_0\_0 gap\_ini = 2e-10 model\_switch = 0 deltaGap0 = 1e-4**



DC SWEEP:



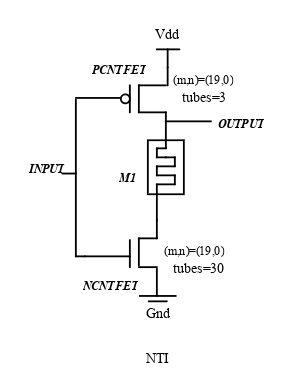
TRANSIENT RESPONSE:

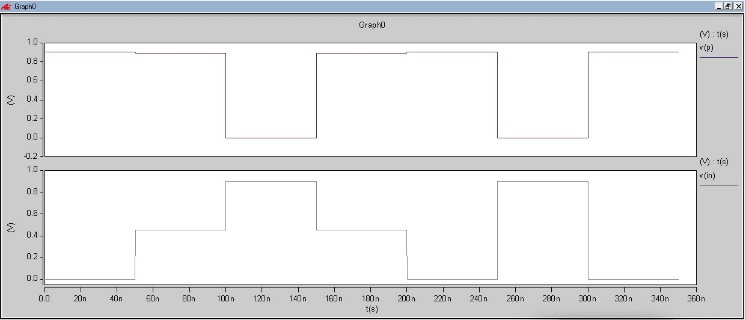


NTI:

In this circuit design two transisters are used (one PNCFET and one NCNFET) With one RRAM. In which

n,m 19,0 are same for both the transistor but transistors tubes are different(PCNFET tubes=3, and NCNFET tubes=30)

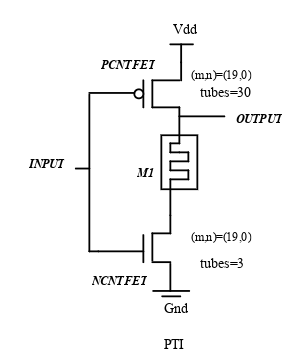


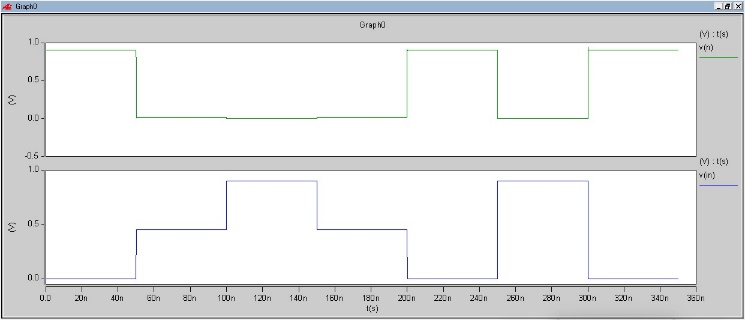


PTI:

In this circuit design two transisters are used (one PNCFET and one NCNFET) With one RRAM. In which

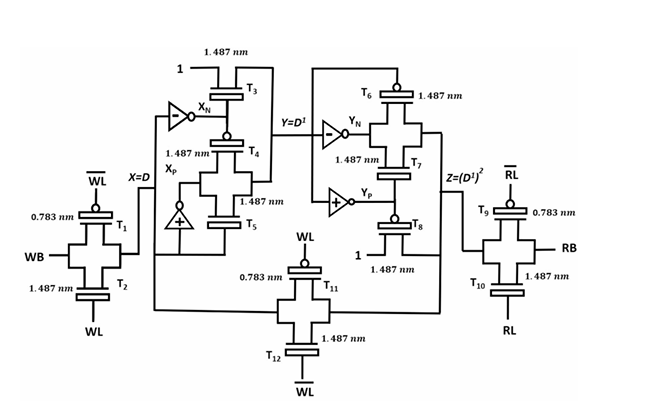
n,m =19,0 are same for both the transistor but transistors tubes are different(PCNFET tubes=30, and NCNFET tubes=3)

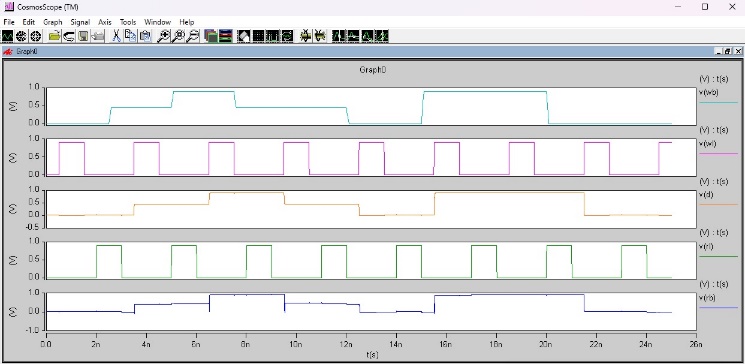




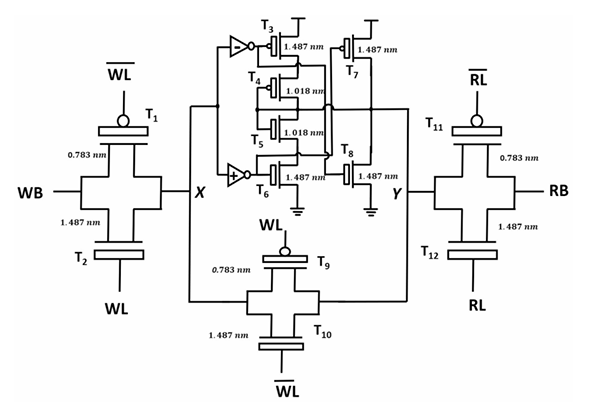
CYCLE OPERATOR using RRAM and CNTFET:

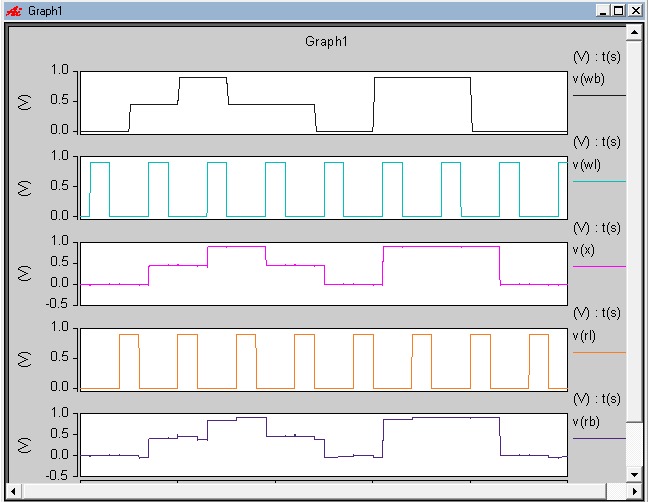
Same circuit is used for designing SRAM but the key elements that is nti and pti are build using RRAM.





BUFFER using RRAM and CNTFET:  
Same circuit is used for designing SRAM but the key elements that is nti and pti are build using RRAM.





RESULTS:

**Cycle operator Write Power dissipation comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µW)** | **Gnrfet (µW)** |
| **0** | **0.51058** | **3.4385** |
| **1** | **0.57375** | **4.6311** |
| **2** | **0.34589** | **5.3293** |

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µW)** | **Gnrfet (µW)** |
| **0** | **0.62914** | **2.4558** |
| **1** | **0.045090** | **4.522** |
| **2** | **0.025965** | **3.8478** |

**Cycle operator Read Power dissipation comparison table:**

**Write Power dissipation comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µW)** | **Gnrfet (µW)** |
| **0** | **1.8411** | **0.1815** |
| **1** | **1.8434** | **2.1918** |
| **2** | **2.3084** | **1.0859** |

**Buffer Read Power dissipation comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µW)** | **Gnrfet (µW)** |
| **0** | **1.3007** | **0.40447** |
| **1** | **0.38692** | **0.10389** |
| **2** | **0.2792** | **0.171096** |

**6T Write Power dissipation comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µW)** | **Gnrfet (µW)** |
| **0** | **2.0892** | **1.2097** |
| **1** | **2.3013** | **1.6493** |
| **2** | **2.3034** | **1.8914** |

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µW)** | **Gnrfet (µW)** |
| **0** | **2.3032** | **0.79271** |
| **1** | **2.3035** | **0.69267** |
| **2** | **2.3036** | **0.13648** |

**6T Read Power dissipation comparison table:**

**Cycle operator Write delay comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µs)** | **Gnrfet(µs)** |
| **0** | **0.003279** | **0.18185** |
| **1** | **0.002487** | **0.21918** |
| **2** | **0.0024505** | **0.10859** |

**Cycle operator Read Time delay comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µs)** | **Gnrfet (µs)** |
| **0** | **0.015404** | **0.04447** |
| **1** | **0.000887** | **0.170388** |
| **2** | **0.005125** | **0.17109** |

**6T Write delay comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µs)** | **Gnrfet (µs)** |
| **0** | **0.0124014** | **0.120515** |
| **1** | **0.0010050** | **0.0096** |
| **2** | **0.83034** | **0.808559** |

**6T Read Time delay comparison table:**

|  |  |  |
| --- | --- | --- |
| **Logic** | **Cntfet (µs)** | **Gnrfet (µs)** |
| **0** | **0.0010214** | **0.12015** |
| **1** | **0.012560** | **0..09876** |
| **2** | **0.0083036** | **0.00342** |

**6T SRAM MOSFET Time delay table :**

|  |  |  |
| --- | --- | --- |
| **logic** | **Write (µs)** | **Read (µs)** |
| **0** | **0.0017** | **0.00986** |
| **1** | **0.377887** | **0.00986** |

**6T SRAM MOSFET Power dissipation comparison table :**

|  |  |  |
| --- | --- | --- |
| **logic** | **Write (µW)** | **Read (µW)** |
| **0** | **0.06875** | **0.344408** |
| **1** | **0.100075** | **0.05678** |

**Rram results:**

**Sram(Cycle operator with rram and cntfet):**

**Power dissipation:**

|  |  |  |
| --- | --- | --- |
| **logic** | **Read (µW)** | **Write(µW)** |
| **0** | **5.0800** | **1.7622** |
| **1** | **0.00132** | **7.2464** |
| **2** | **0.000146** | **1.7514** |

**Time delay:**

|  |  |  |
| --- | --- | --- |
| **logic** | **Read (ns)** | **Write(ns)** |
| **0** | **1.5100** | **3.0871** |
| **1** | **0.49556** | **0.0998** |
| **2** | **0.53358** | **2.4858** |

**Sram(buffer with rram and cntfet):**

|  |  |  |
| --- | --- | --- |
| **logic** | **Read (µW)** | **Write(µW)** |
| **0** | **0.68858** | **7.8883** |
| **1** | **0.00142** | **1.0673** |
| **2** | **0.00286** | **1.3239** |

**Power dissipation:**

**Time delay:**

|  |  |  |
| --- | --- | --- |
| **logic** | **Read (ns)** | **Write(ns)** |
| **0** | **1.6100** | **3.1043** |
| **1** | **0.49535** | **0.1318** |
| **2** | **0.58358** | **2.5858** |

**Comparision between the power dissipation and the time delays of the ssram circuits which is desighned using rram and without rram in cntfet technology:**

**Sram(cycle operator):**

**Power dissipation**

**Read:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (µW)** | **CNTFET(µW)** |
| **0** | **5.0800** | **0.62914** |
| **1** | **0.00132** | **0.045090** |
| **2** | **0.000146** | **0.025965** |

**Write:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (µW)** | **CNTFET(µW)** |
| **0** | **1.7622** | **0.51058** |
| **1** | **7.2464** | **5.7375** |
| **2** | **1.7514** | **0.34589** |

**Time delay:**

**Read:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (ns)** | **CNTFET(ns)** |
| **0** | **1.5100** | **1.5040** |
| **1** | **0.49556** | **0.8876** |
| **2** | **0.53358** | **0.5125** |

**Write:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (ns)** | **CNTFET(ns)** |
| **0** | **3.0871** | **3.0279** |
| **1** | **0.0998** | **0.02248** |
| **2** | **2.4858** | **2.4505** |

**Sram(buffer):**

**Power dissipation :**

**Read:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (ns)** | **CNTFET(ns)** |
| **0** | **3.0871** | **3.0279** |
| **1** | **0.0998** | **0.02248** |
| **2** | **2.4858** | **2.4505** |

**Write:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (µW)** | **CNTFET(µW)** |
| **0** | **0.8883** | **1.8411** |
| **1** | **1.0673** | **1.8434** |
| **2** | **1.3239** | **2.3084** |

**Time delay:**

**Read:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (ns)** | **CNTFET(ns)** |
| **0** | **1.6100** | **2.6204** |
| **1** | **0.49535** | **1.4725** |
| **2** | **0.58358** | **0.6453** |

**Write:**

|  |  |  |
| --- | --- | --- |
| **logic** | **RRAM\_CNTFET (ns)** | **CNTFET(ns)** |
| **0** | **3.1043** | **3.0089** |
| **1** | **0.1318** | **0.0244** |
| **2** | **2.5858** | **0.25858** |

**Conclusion:**

Ternary SRAM architectures were designed using cycle operators and buffer-based designs.Advanced CNTFET and GNRFET technologies were leveraged for enhanced performance.Significant improvements in power efficiency and delay reduction were observed compared to MOSFET-based designs.Incorporation of RRAM-based resistive switching mechanisms improved stability, scalability, and performance.The proposed design is suitable for next-generation low-power applications.Results confirm the viability of ternary SRAM with memristors for high-performance computing.Future research can focus on optimizing designs for large-scale integration.