```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3   use IEEE.STD_LOGIC_ARITH.ALL;
4   use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6   entity display is
7   port (
8         clk : in std_logic;
9           bcd : in std_logic_vector(3 downto 0);  --BCD input
10          segment7 : out std_logic_vector(6 downto 0)  -- 7 bit decoded output.
11      );
12  end display;
13  --'a' corresponds to MSB of segment7 and g corresponds to LSB of segment7.
14  architecture Behavioral of display is
15
16  begin
17  process (clk,bcd)
18  BEGIN
19  if (clk'event and clk='1') then
20  case  bcd is
21  when "0000"=> segment7 <="0000001";  -- '0'
22  when "0001"=> segment7 <="1001111";  -- '1'
23  when "0010"=> segment7 <="0010010";  -- '2'
24  when "0011"=> segment7 <="0000110";  -- '3'
25  when "0100"=> segment7 <="1001100";  -- '4'
26  when "0101"=> segment7 <="0100100";  -- '5'
27  when "0110"=> segment7 <="0100000";  -- '6'
28  when "0111"=> segment7 <="0001111";  -- '7'
29  when "1000"=> segment7 <="0000000";  -- '8'
30  when "1001"=> segment7 <="0000100";  -- '9'
31   when "1010" => segment7 <="0001000";
32   when "1011" => segment7 <="1100000" ;
33
34    when "1100"=> segment7 <= "1110010";
35    when "1101"=> segment7 <=  "1000010" ;
36   when "1110"=> segment7 <= "0110000" ;
37    when "1111"=> segment7 <= "0111000";
38   --nothing is displayed when a number more than 9 is given as input.
39  when others=> segment7 <="1111111";
40  end case;
41  end if;
42
43  end process;
44
45  end Behavioral;
```