Physical category (5%)		
Design Stage	Description	Value
P&R	Number of DRC violation (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violation (ex: 0) (Verify -> Verify Connectivity…)	0
	Core area (um^2)	117276.76
	Die area (um^2)	252871.11
Prost-layout Gate-level Seimulation	Cycle time for Post-layout Simulation (ex. 10ns)	4544 ns
N/A	Add IO PAD? (Yes/No)	NO

- **Any other information you want to specify:**