Homework 3 Report

CVSD **Student ID: R07943158**

a. Attached data table

Area (um ^ 2)	16595.479748
Clock cycle (ns)	6
Total simulation time (ns)	768
Cost (um^2 *ns)	12745328.4465

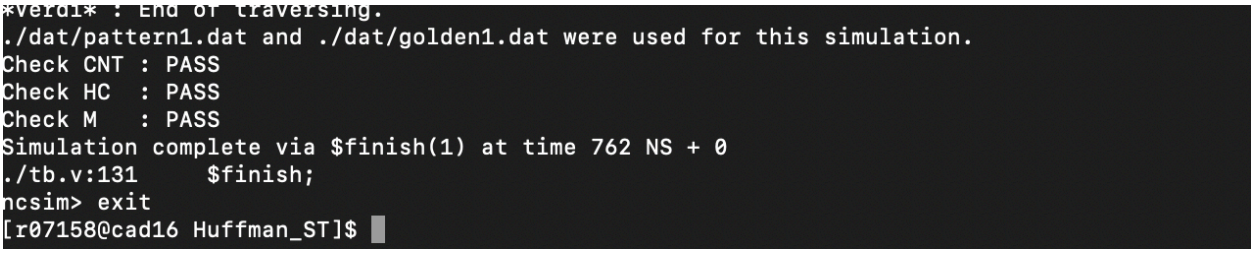
b. Necessary snapshots

b-1. Snapshot of area (total cell area) in Design Compiler

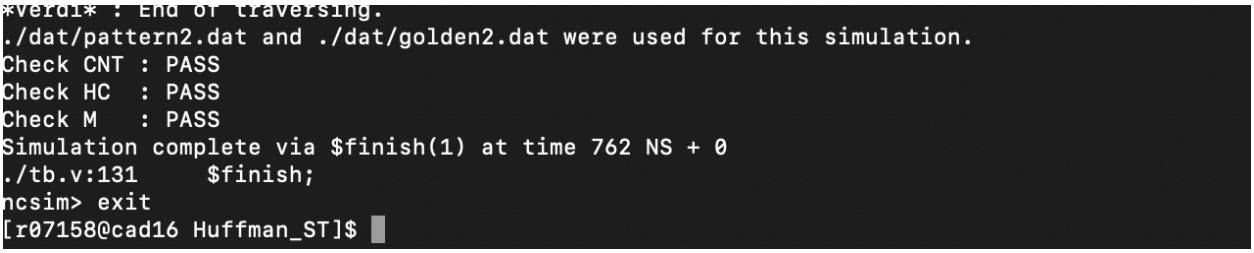
```
****************************************
Report : area
Design : huffman
Version: N-2017.09-SP2
Date   : Wed Nov 13 18:23:00 2019
****************************************

Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)
    sram_1024x8_t13 (File: /home/raid7_2/user07/r07158/CVSD3/final/Huffman_ST/Memory/sram_1
/sram_1024x8_t13_slow_syn.db)

Number of ports:                          153
Number of nets:                          1424
Number of cells:                         1246
Number of combinational cells:           1066
Number of sequential cells:               171
Number of macros/black boxes:               1
Number of buf/inv:                        275
Number of references:                     145

Combinational area:              10539.156538
Buf/Inv area:                     1573.489783
Noncombinational area:            4482.833427
Macro/Black Box area:            69557.296875
Net Interconnect area:          154840.785248

Total cell area:                 84579.286840
Total area:                     239420.072088
```

b-2. Snapshot of RTL/gate-level ncverilog simulation

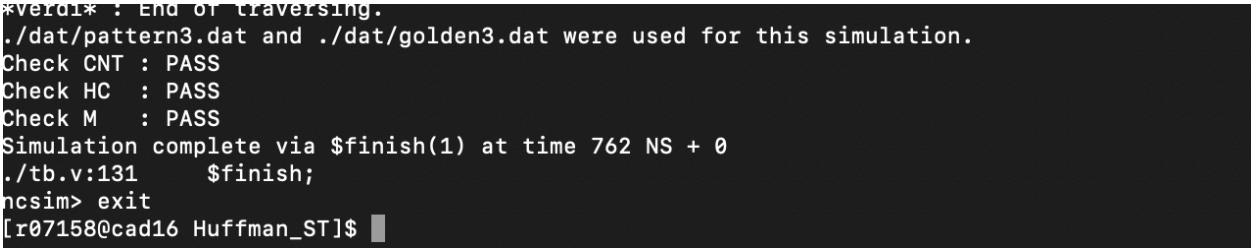
- Snapshot of tb1 RTL simulation



- Snapshot of tb2 RTL simulation



- Snapshot of tb3 RTL simulation



- Snapshot of tb1 Gate Level simulation

```
./dat/pattern1.dat and ./dat/golden1.dat were used for this simulation.
SDF File ./huffman_syn.sdf were used for this simulation.

Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8742 PS,  0.272 : 272 PS,  -0.128 : -128 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\CNT_reg[0][6]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[1]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[2]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[3]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[0]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][1]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][5]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][2]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][4]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][3]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8741 PS,  0.261 : 261 PS,  -0.096 : -96 PS );
            File: ./tsmc13.v, line = 18010
           Scope: tb.u_huffman.\CNT_reg[0][5]
            Time: 9 NS

Check CNT : PASS
Check HC  : PASS
Check M   : PASS
Simulation complete via $finish(1) at time 768 NS + 0
./tb.v:131     $finish;
ncsim> exit
[r07158@cad16 Huffman_ST]$
```

- Snapshot of tb2 Gate Level simulation

```
./dat/pattern2.dat and ./dat/golden2.dat were used for this simulation.
SDF File ./huffman_syn.sdf were used for this simulation.

Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8742 PS,  0.272 : 272 PS,  -0.128 : -128 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\CNT_reg[0][6]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[1]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[2]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[3]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
            File: ./tsmc13.v, line = 18057
           Scope: tb.u_huffman.\sram_d_reg[0]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][1]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][5]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][2]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][4]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
            File: ./tsmc13.v, line = 17859
           Scope: tb.u_huffman.\index_value_reg[0][3]
            Time: 9 NS


Warning!  Timing violation
           $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8741 PS,  0.261 : 261 PS,  -0.096 : -96 PS );
            File: ./tsmc13.v, line = 18010
           Scope: tb.u_huffman.\CNT_reg[0][5]
            Time: 9 NS

Check CNT : PASS
Check HC  : PASS
Check M   : PASS
Simulation complete via $finish(1) at time 768 NS + 0
./tb.v:131     $finish;
ncsim> exit
[r07158@cad16 Huffman_ST]$
```

- Snapshot of tb3 Gate Level simulation

```
./dat/pattern3.dat and ./dat/golden3.dat were used for this simulation.
SDF File ./huffman_syn.sdf were used for this simulation.

Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8742 PS,  0.272 : 272 PS,  -0.128 : -128 PS );
           File: ./tsmc13.v, line = 18057
          Scope: tb.u_huffman.\CNT_reg[0][6]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
           File: ./tsmc13.v, line = 18057
          Scope: tb.u_huffman.\sram_d_reg[1]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
           File: ./tsmc13.v, line = 18057
          Scope: tb.u_huffman.\sram_d_reg[2]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
           File: ./tsmc13.v, line = 18057
          Scope: tb.u_huffman.\sram_d_reg[3]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8761 PS,  0.287 : 287 PS,  -0.147 : -147 PS );
           File: ./tsmc13.v, line = 18057
          Scope: tb.u_huffman.\sram_d_reg[0]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
           File: ./tsmc13.v, line = 17859
          Scope: tb.u_huffman.\index_value_reg[0][1]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
           File: ./tsmc13.v, line = 17859
          Scope: tb.u_huffman.\index_value_reg[0][5]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
           File: ./tsmc13.v, line = 17859
          Scope: tb.u_huffman.\index_value_reg[0][2]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
           File: ./tsmc13.v, line = 17859
          Scope: tb.u_huffman.\index_value_reg[0][4]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8856 PS,  0.277 : 277 PS,  -0.108 : -108 PS );
           File: ./tsmc13.v, line = 17859
          Scope: tb.u_huffman.\index_value_reg[0][3]
           Time: 9 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):9 NS, negedge D:8741 PS,  0.261 : 261 PS,  -0.096 : -96 PS );
           File: ./tsmc13.v, line = 18010
          Scope: tb.u_huffman.\CNT_reg[0][5]
           Time: 9 NS

Check CNT : PASS
Check HC  : PASS
Check M   : PASS
Simulation complete via $finish(1) at time 768 NS + 0
./tb.v:131     $finish;
ncsim> exit
[r07158@cad16 Huffman_ST]$
```

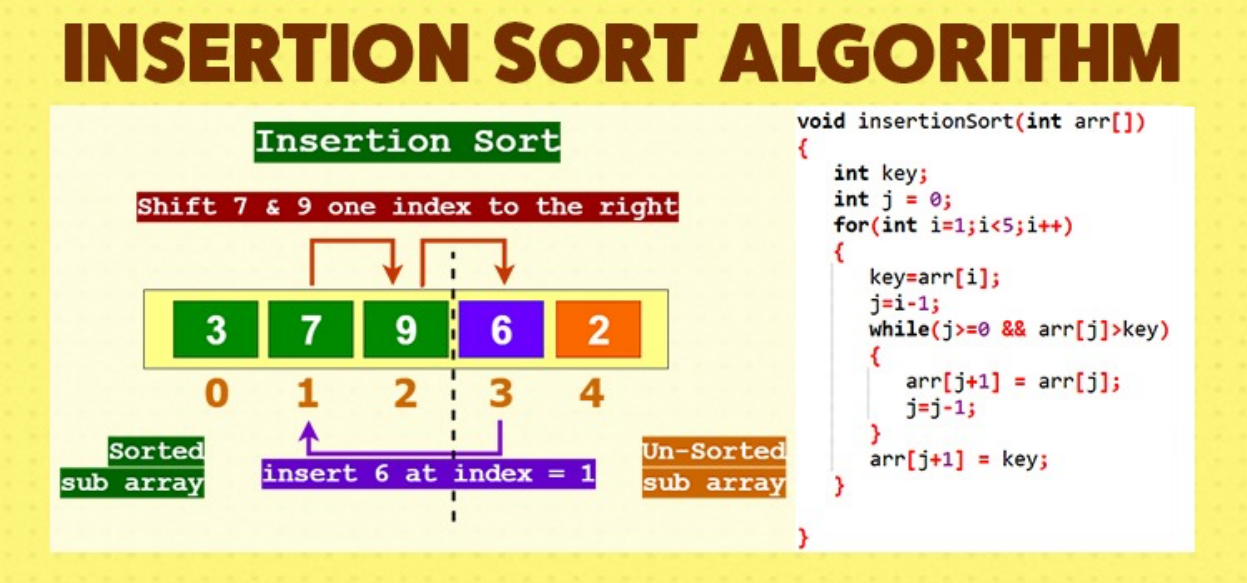
C. Describe your design structure

Huffman Code Implementation:

I use simple method to generate Huffman code.

Step 1: Initially the input is stored 0~99. So after reset, memory is read at 128 address.
Step 2: After reading CNT, sorting is done. After sorting, I proceed to encoding.
Step 3: Then comes the procedure to build HC and M
Step 4: And Finally output HC and M

Sorting is the critical step in the entire process. I use insertion sort method in this.



Then I build tree and obtain merged nodes.
Further HC and Mask value are obtained simultaneously.