CVSD HW4 Report **R07943158**

a. Identify all bugs in interconnect.v. Explain how to fix them, and which assertions will be violated, i.e. will cause counter example?

1. assign s_b_handshake =mem_bready || mem_bvalid;

Corrected as:
assign s_b_handshake = mem_bready && mem_bvalid;

Slave response handshake will be done only when above two flags are high

2. M0_B : NEXT_STATE = (m0_b_handshake) ? (counter_r == 9 ? M1_AW : M0_AW) : M0_B;

Corrected as:
M0_B : NEXT_STATE = (m0_b_handshake) ? (counter_r == 7 ? M1_AW : M0_AW) : M0_B;

m0_b_handshake will be high only when counter is till 7 not 9, this will cause violation in access of masters.

3. M1_B : NEXT_STATE = (counter_r == 7) ? M0_AW : M1_AW;

Corrected as:
M1_B : NEXT_STATE = (m1_b_handshake) ? (counter_r == 7 ? M0_AW : M1_AW) : M1_B;

Next state needs to be defined on basis of handshake from master 1. It needs to switch access between master after 8 successive transactions. m0_data_good_bb will get violated by this.

4. S_B : NEXT_STATE = priority_r ? M1_B : M0_B;

Corrected as:
S_B : NEXT_STATE = (s_b_handshake) ? (priority_r ? M1_B : M0_B) : S_B;

Next state needs to be defined on basis of handshake from slave

5. if (STATE == M0_W) data_buf_w = (m0_w_handshake) ? ~m0_wdata : data_buf_r;

Corrected as:
if (STATE == M0_W) data_buf_w = (m0_w_handshake) ? m0_wdata : data_buf_r;

m0_wdata needs not to be complemented if there is write handshake on m0

6. priority_r <= priority_r;

Corrected as:
priority_r <= priority_w;

Priority_r needs to be updated

b. **Attach the snapshot of all assertions' verification result of (1) original RTL code with bug (2) Modified RTL code proving on JasperGold. (2 Images)**

1. RTL Code with bug:

Type	Name	Engine	Bound	Time
Assert	fv_tb.memory.genParamChk.assert_param_READONLY_INTERFACE_WRITEONLY_INTERFACE_limitation	PRE	Infinite	
Assert	fv_tb.memory.genParamChk.assert_param_EXCL_ACCESS_ON_limitation	PRE	Infinite	
Assert	fv_tb.memory.genParamChk.assert_param_EXCL_ACCESS_ON_with_AXI4_LITE_limitation	PRE	Infinite	
Assert	fv_tb.memory.genParamChk.assert_param_MAX_PENDING	PRE	Infinite	
Assert	fv_tb.memory.genParamChk.genNoRd.assert_param_MAX_PENDING_RD	PRE	Infinite	
Assert	fv_tb.memory.genStableChks.genStableChksWRInf.master_aw_awvalid_stable	Hp (2)	Infinite	
Assert	fv_tb.memory.genStableChks.genStableChksWRInf.master_aw_awaddr_stable	Hp (2)	Infinite	
Assert	fv_tb.memory.genStableChks.genStableChksWRInf.master_w_wvalid_stable	Hp (2)	Infinite	
Assert	fv_tb.memory.genStableChks.genStableChksWRInf.master_w_wdata_stable	Hp (2)	Infinite	
Assert	fv_tb.memory.genPropWrOnlyInf.master_arvalid_low_when_wr_only_inf	PRE	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genAXI4Full.master_aw_awaddr_wrap_aligned	PRE	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genAXI4Full.gen4KawaddrChk.master_aw_awaddr_never_cross_4...	PRE	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genNoWrTblOverflow.master_aw_wr_tbl_no_overflow	Ht	10	
Assert	fv_tb.memory.genPropChksWRInf.assert_aw_wr_tbl_no_overflow	Hp (1)	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genNoWrDatTblOverflow.master_w_wr_tbl_no_overflow	N (11)	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.assert_w_wr_tbl_no_overflow	Hp (1)	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genLiveWr.genDBC.master_aw_awvalid_eventually	PRE	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genLiveWr.master_w_wvalid_eventually	PRE	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genLiveWr.master_b_bready_eventually	PRE	Infinite	
Assert	fv_tb.memory.genPropChksWRInf.genLiveWaitWr.master_b_bvalid_bready_eventually	PRE	Infinite	
Assert (live)	fv_tb.assert_m0_addr_good_bb	AM (49)	Infinite	
Assert (live)	fv_tb.assert_m1_addr_good_bb	N (14)	Infinite	
Assert (live)	fv_tb.assert_m0_data_good_bb	B	3 + 48	
Assert (live)	fv_tb.assert_m1_data_good_bb	N (14)	Infinite	
Assert (live)	fv_tb.assert_m0_resp_good_bb	N (9)	Infinite	
Assert (live)	fv_tb.assert_m1_resp_good_bb	PRE	Infinite	
Assert (live)	fv_tb.assert_m0_aready_good_wb	AM (127)	Infinite	
Assert (live)	fv_tb.assert_m0_dready_good_wb	AM (145)	Infinite	
Assert (live)	fv_tb.assert_m1_aready_good_wb	N (14)	Infinite	
Assert (live)	fv_tb.assert_m1_dready_good_wb	N (14)	Infinite	
Assert	fv_tb.master0.genParamChk.genAXI4.assert_param_DATA_WIDTH_legal	PRE	Infinite	
Assert	fv_tb.master0.genParamChk.assert_param_ALL_STROBES_HIGH_ON_limitation	PRE	Infinite	
Assert	fv_tb.master0.genParamChk.assert_param_MAX_WAIT_CYCLES_ON_legal	PRE	Infinite	
Assert	fv_tb.master0.genParamChk.assert_param_READONLY_INTERFACE_WRITEONLY_INTERFACE_limitation	PRE	Infinite	
Assert	fv_tb.master0.genParamChk.assert_param_EXCL_ACCESS_ON_limitation	PRE	Infinite	
Assert	fv_tb.master0.genParamChk.assert_param_EXCL_ACCESS_ON_with_AXI4_LITE_limitation	PRE	Infinite	
Assert	fv_tb.master0.genParamChk.assert_param_MAX_PENDING	PRE	Infinite	
Assert	fv_tb.master0.genParamChk.genNoRd.assert_param_MAX_PENDING_RD	PRE	Infinite	
Assert	fv_tb.master0.genStableChks.genStableChksWRInf.slave_b_bvalid_stable	Hp (2)	Infinite	
Assert	fv_tb.master0.genStableChks.genStableChksWRInf.slave_b_bresp_stable	PRE	Infinite	

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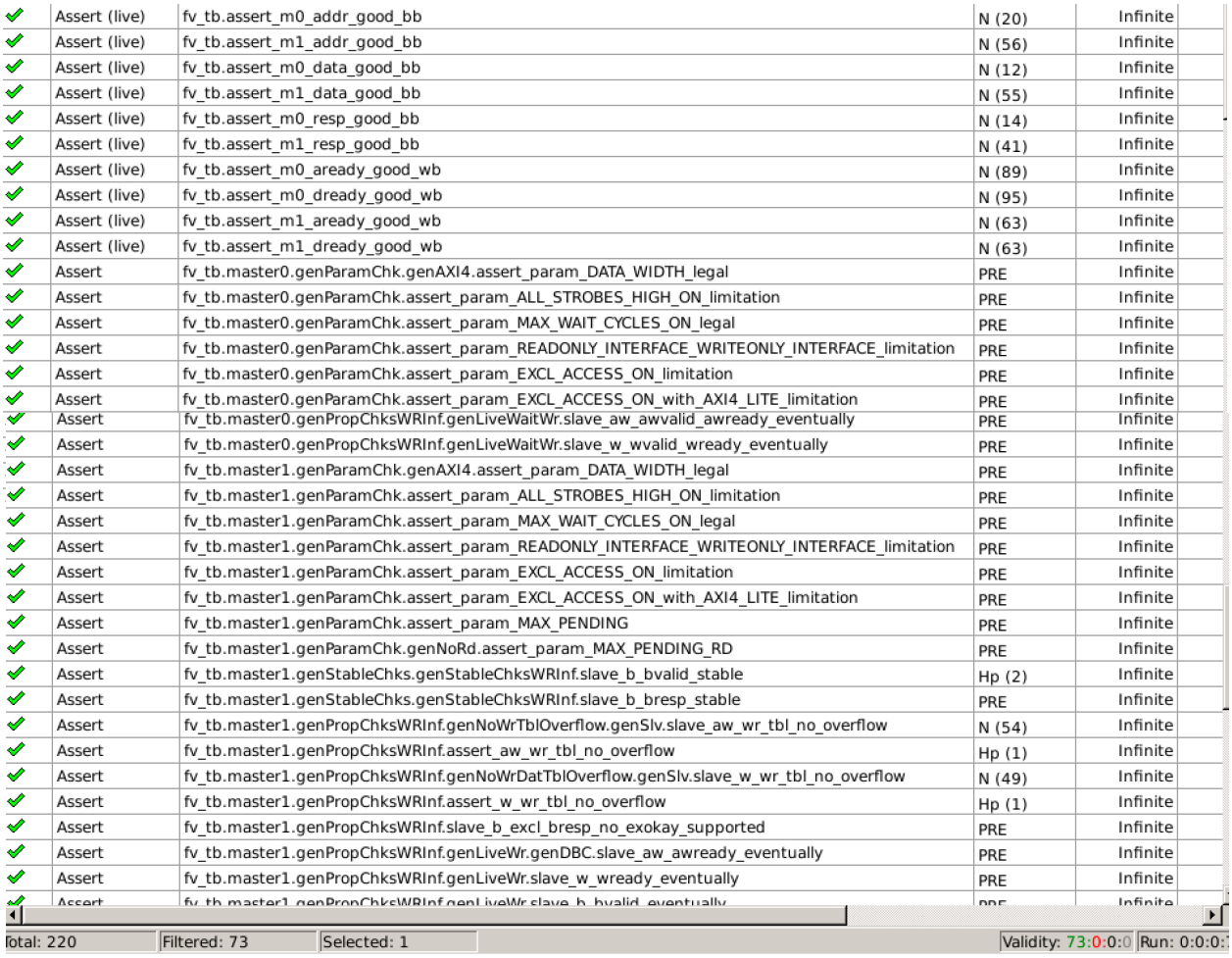
2. Modified RTL code proving on JasperGold.



✔	Assert (live)	fv_tb.assert_m0_addr_good_bb	N (20)	Infinite
✔	Assert (live)	fv_tb.assert_m1_addr_good_bb	N (56)	Infinite
✔	Assert (live)	fv_tb.assert_m0_data_good_bb	N (12)	Infinite
✔	Assert (live)	fv_tb.assert_m1_data_good_bb	N (55)	Infinite
✔	Assert (live)	fv_tb.assert_m0_resp_good_bb	N (14)	Infinite
✔	Assert (live)	fv_tb.assert_m1_resp_good_bb	N (41)	Infinite
✔	Assert (live)	fv_tb.assert_m0_aready_good_wb	N (89)	Infinite
✔	Assert (live)	fv_tb.assert_m0_dready_good_wb	N (95)	Infinite
✔	Assert (live)	fv_tb.assert_m1_aready_good_wb	N (63)	Infinite
✔	Assert (live)	fv_tb.assert_m1_dready_good_wb	N (63)	Infinite
✔	Assert	fv_tb.master0.genParamChk.genAXI4.assert_param_DATA_WIDTH_legal	PRE	Infinite
✔	Assert	fv_tb.master0.genParamChk.assert_param_ALL_STROBES_HIGH_ON_limitation	PRE	Infinite
✔	Assert	fv_tb.master0.genParamChk.assert_param_MAX_WAIT_CYCLES_ON_legal	PRE	Infinite
✔	Assert	fv_tb.master0.genParamChk.assert_param_READONLY_INTERFACE_WRITEONLY_INTERFACE_limitation	PRE	Infinite
✔	Assert	fv_tb.master0.genParamChk.assert_param_EXCL_ACCESS_ON_limitation	PRE	Infinite
✔	Assert	fv_tb.master0.genParamChk.assert_param_EXCL_ACCESS_ON_with_AXI4_LITE_limitation	PRE	Infinite
✔	Assert	fv_tb.master0.genPropChksWRInf.genLiveWaitWr.slave_aw_awvalid_awready_eventually	PRE	Infinite
✔	Assert	fv_tb.master0.genPropChksWRInf.genLiveWaitWr.slave_w_wvalid_wready_eventually	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.genAXI4.assert_param_DATA_WIDTH_legal	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.assert_param_ALL_STROBES_HIGH_ON_limitation	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.assert_param_MAX_WAIT_CYCLES_ON_legal	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.assert_param_READONLY_INTERFACE_WRITEONLY_INTERFACE_limitation	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.assert_param_EXCL_ACCESS_ON_limitation	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.assert_param_EXCL_ACCESS_ON_with_AXI4_LITE_limitation	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.assert_param_MAX_PENDING	PRE	Infinite
✔	Assert	fv_tb.master1.genParamChk.genNoRd.assert_param_MAX_PENDING_RD	PRE	Infinite
✔	Assert	fv_tb.master1.genStableChks.genStableChksWRInf.slave_b_bvalid_stable	Hp (2)	Infinite
✔	Assert	fv_tb.master1.genStableChks.genStableChksWRInf.slave_b_bresp_stable	PRE	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.genNoWrTblOverflow.genSlv.slave_aw_wr_tbl_no_overflow	N (54)	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.assert_aw_wr_tbl_no_overflow	Hp (1)	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.genNoWrDatTblOverflow.genSlv.slave_w_wr_tbl_no_overflow	N (49)	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.assert_w_wr_tbl_no_overflow	Hp (1)	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.slave_b_excl_bresp_no_exokay_supported	PRE	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.genLiveWr.genDBC.slave_aw_awready_eventually	PRE	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.genLiveWr.slave_w_wready_eventually	PRE	Infinite
✔	Assert	fv_tb.master1.genPropChksWRInf.genLiveWr.slave_b_bvalid_eventually	PRE	Infinite

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c. List all assertions that will not be violated even verifying the original RTL code with bug.

The assertions that not will not be violated even verifying the original RTL code with bug are:

1. Assert_m0_addr_good_bb
2. assert_m1_addr_good_bb
3. assert_m1_data_good_bb
4. assert_m0_resp_good_bb
5. assert_m1_resp_good_bb
6. assert_m0_aready_good_bb
7. assert_m1_aready_good_bb
8. assert_m0_dready_good_bb
9. assert_m1_dready_good_bb

d. Attach the snapshot of all the properties being proved.

Type	Name	Engine	Bound	Time
Assert (live)	fv_tb.assert_m0_addr_good_bb	N (20)	Infinite	
Assert (live)	fv_tb.assert_m1_addr_good_bb	N (56)	Infinite	
Assert (live)	fv_tb.assert_m0_data_good_bb	N (12)	Infinite	
Assert (live)	fv_tb.assert_m1_data_good_bb	N (55)	Infinite	
Assert (live)	fv_tb.assert_m0_resp_good_bb	N (14)	Infinite	
Assert (live)	fv_tb.assert_m1_resp_good_bb	N (41)	Infinite	
Assert (live)	fv_tb.assert_m0_aready_good_wb	N (89)	Infinite	
Assert (live)	fv_tb.assert_m0_dready_good_wb	N (95)	Infinite	
Assert (live)	fv_tb.assert_m1_aready_good_wb	N (63)	Infinite	
Assert (live)	fv_tb.assert_m1_dready_good_wb	N (63)	Infinite	