VLSI Testing Proposal

N-detect TDF ATPG and Compression

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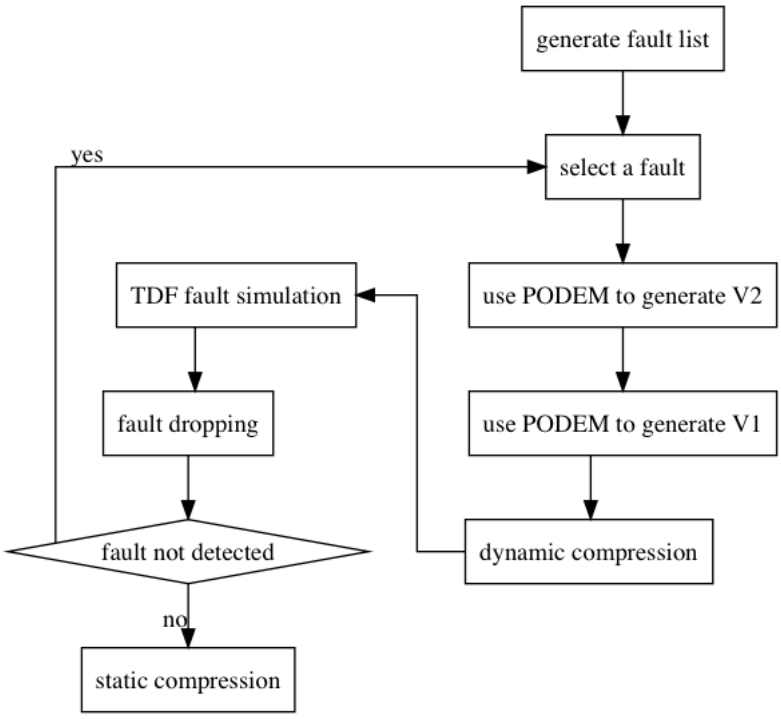
0.1 Schedule

- basic version without compression: 12/12
- progress presentation slide: 12/16
- compression: 12/23
- remaining part, optimization: 1/2
- report, optimization: 1/8
- demo: 1/15

0.2 Proposed Method



0.3 Job Partition

- static compression: Divya
- constraint aware PODEM: 黃韋智
- fault simulation: 錢柏均

- fault dropping: 錢柏均
- overall TDF ATPG flow: 朱宇融
- dynamic compression: optional
- fault dictionary: optional
- test suit: 錢柏均

0.4 Reference

- B. Benware, C. Schuermyer, S. Ranganathan, R. Madge, P. Krishnamurthy, "Impact of multipledetect test patterns on product quality", IEEE Int'l Test Conference, 2003.
- I.Hamzaoglu, J.Patel, "Test set compaction algorithms for combinational circuits", ICCAD 1998.
- Xiang, Dong, et al. "Compact test generation with an Influence input measure for launch-on-capture transition fault testing", IEEE Transactions on Very Large Scale Integration (VLSI) Systems 22.9 (2014)
- H. Ichihara, A. Ogawa, T. Inoue, A. Tamura, "Dynamic test compression using statistical codeing", IEEE Proceedings 10th Asian Test Symposium, 2001.
- Yu-Wei Chen, et al. "Parallel order atpg for test compaction", IEEE International Symposium on VLSI Design, Automation and Test, 2018