CAD contest A

Team 11

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Outline

- Terminology
- Proposed Algorithm
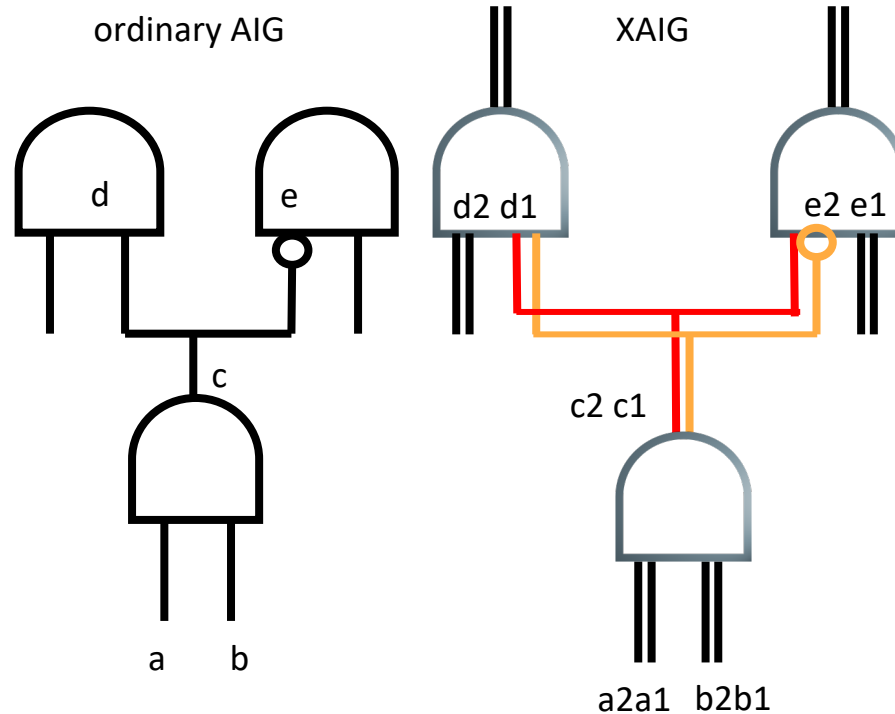- Experimental Result
- Conclusion

Outline

- **Terminology**
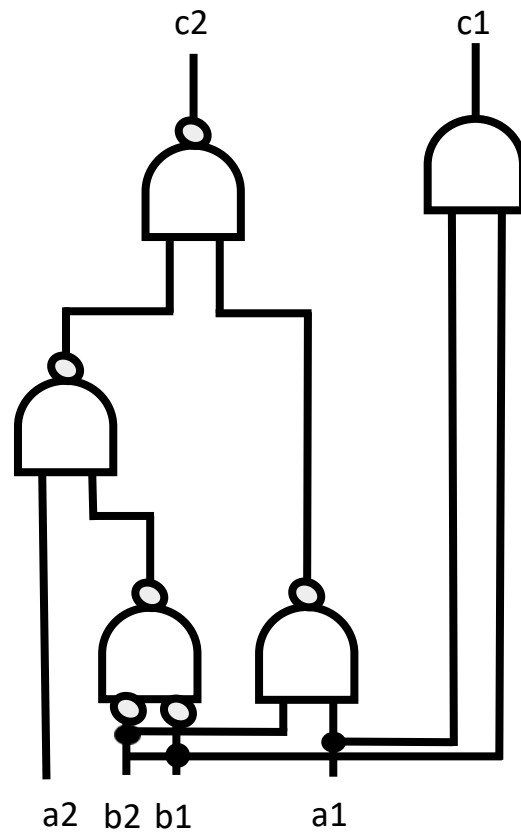- Proposed Algorithm
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Terminology

- CE : compatible equivalent
- XAIG
- CMiter

XAIG

ordinary AIG   XAIG

Encode : (a→a2 a1)
- 0 → 00
- 1 → 01
- X → 11 or 10 (1X)

Our XAIG has four bit input, two bit output
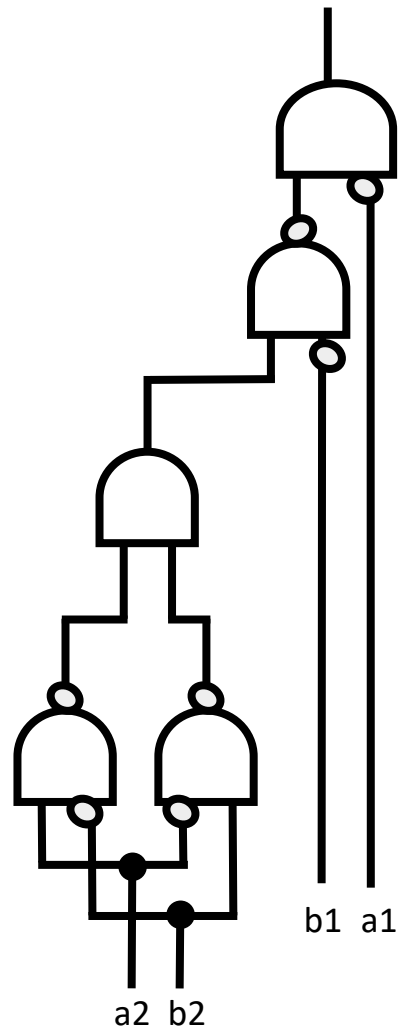
XAIG
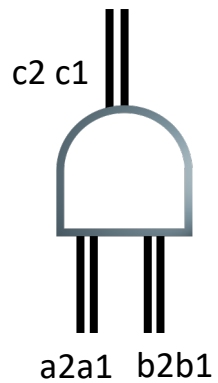
CMiter : a CE b

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Algorithm Flow

- Use yosys to read gf.v rf.v
- Use yosys to convert verilog to aig, and encode const 1'bx as latches
- Use yosys to strash and optimize the circuit
- Build XAIG
- Random Simulation on XAIG to witness compatible inequivalence early.
- Write out blif
- XCEC in Abc
  - Add CMiter
  - Fraig+Simulation
  - SAT

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Experimental Result

Alpha Test results

Time	case1	case2	case3	case4	case5	case6	case7	case8	case9
Rank0	189.57	0.67	266.9	1.82	41.72	42.17	0.52	636.06	0.27
Rank1	199.04	0.92	709.83	4.83	62.12	59.41	0.77	1249.86	1.32
Rank2	679.49	2.12	1201.34	5.03	75.14	77.09	3.13	1402.34	8.04
Result	EQ	NEQ	EQ	NEQ	EQ	EQ	NEQ	EQ	NEQ

#Aig	case1	case2	case3	case4	case5	case6	case7	case8	case9
yosys	0.96	1.2		5.46	10.12	9.7	4.02		12.264
abc	1259.31	0.1	TIMEOUT	-	3.52	3.15	-	TIMEOUT	-
runtime	1260.27	1.3		5.46	13.64	12.85	4.02		12.264
Result	EQ	NEQ		NEQ	EQ	EQ	NEQ		NEQ

Discussion

#Aig	case1	case2	case3	case4	case5	case6	case7	case8	case9
gf	4000	4000	28776	28776	26997	26997	50702	309907	111056
rf	4275	4375	28935	29380	26825	26825	50217	289085	111056
runtime	1260.27	1.3	TIMEOUT	5.46	13.64	12.85	4.02	TIMEOUT	12.264
Result	EQ	NEQ		NEQ	EQ	EQ	NEQ		NEQ

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Conclusion

- For NEQ cases, we have correct answers for released cases.
- For some EQ cases, it will time out during SAT solving stage.
- For some EQ cases that we have proved successfully, our performance is better than the alpha test result released by CAD contest.
- For NEQ cases, most of our runtime is spent on reading files and simulation.

	case1	case2	case4	case5	case6	case7	case9
rank0 total / our total	0.15	0.52	0.33	3.06	3.28	0.13	0.02
rank0 total / our abc	0.15	6.7	-	11.86	13.39	-	-

To Improve Runtime, We Can Modify…

- Process of reading file
- Simulation pattern
- Fraig
  - Hierarchical Fraig
  - Balance X
- SAT solver
  - Add learnt clause

Theorem

O1 CE O2 if V1 CE V1' and V2 CE V2'.