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| **(01)**  **Design & Implement 4-bit BCD code to Excess-3 code converter circuit.** |
| **(02)**  **Design & Implement 2:1 Multiplexer using logic gates**  **Implement the following function**  **F(A,B,C,D)=∑m( 1,2,4,6,8,10,15) using IC-74153** |
| **(03)**  **Design & Implement the following ckt. Using IC-74LS153**  **Implement 8:1 multiplexer using 4:1 multiplexer**  **Implement the function F(A,B,C,D)=∑m(1,3, 7, 8, 11, 14)**  **using 4:1 multiplexer (Assume A,B are select lines)** |
| **(04)**  **Verify the function table of IC-74LS138.**  **Design & Implement Full Adder using IC 74138.** |
| **(05)**  **Design & Implement BCD adder ckt. Using IC-7483. Illustrate your design with following addition**   1. **4+3 ii) 6+4 iii) 8+7**   **Design 9’s complement ckt.using IC-7483** |
| **(06)**  **Design & Implement 3-bit Asynchronous up counter using IC 7476.**  **Implement MOD - 6 up counter use IC-4027 / 7476.**  **Draw timing diagram for 3 bit Asynchronous up counter.** |
| **(07)**  **Design & Implement 3-bit Synchronous Down counter using MS JK**  **Flip-Flop.**  **Implement divide-by-5 counter using use IC-4027 / 7476.**  **Draw timing diagram.** |
| **(08)**  **Design & Implement sequence generator circuit to generate the following sequence :**  **2 3 5 7**  **What is Lock out condition? How to avoid it?** |
| **(09)**  **Design & Implement sequence detector circuit to detect the following sequence :**  **--- 1 0 1 ---**  **using Mealy’s model.** |
| **(10)**  **Design & Implement MOD – 7 and Mod - 96 Counter using IC-7490.** |
| **(11)**  **To verify the function table of IC-74191.**  **Design & Implement pressetable MOD - 6 UP counter using IC-74191.**  **What is significance of TC and RC?** |
| **(12)**  **Verify the function table of IC-74194**  **Design & Implement Pseudo Random Binary Sequence (PRBS) Generator using IC-74194.**  **Why it is called universal counter?** |
| **(13)**  **Design & Simulation of Full Adder Using Dataflow/Behavioral/Structural modeling style.** |
| **(14)**  **Design & Simulation of 4 : 1 Multiplexer**  **using Dataflow/Behavioral/Structural modeling style.** |
| **(15)**  **Design & Simulation of 4 bit Synchronous U/D counter**  **using Dataflow/Behavioral/Structural modeling style.** |
| **(16)**  **Design & Simulation of 4 bit Asynchronous Down counter**  **using Dataflow/Behavioral/Structural modeling style.** |
| **(17)**  **Design & Implement 4-bit Gray to Binary code converter circuit.** |
| **(18)**  **Design & Implement the following circuit using IC-74LS153**  **Implement 8:1 multiplexer using 4:1 multiplexer**  **Implement the function F(A,B,C,D)=∑m( 0, 2, 5, 10, 13, 15)**  **using 4:1 multiplexer (Assume C,D are select lines)** |
| **(19)**  **Design & Implement 3- bit binary to 3-bit gray code converter circuit using IC-74LS153.** |
| **(20)**  **Design & Implement the following function using IC-74LS138**  **F1(A,B,C) )=∑m( 0, 2, 3, 6 )**  **F2(A,B,C) )=∑m( 1, 3, 4, 5 )** |
| **(21)**  **Design & Implement BCD adder ckt. Using IC-7483. Illustrate your design with following addition**   1. **6+3 ii) 6+2 iii) 9+9** |
| **(22)**  **Design & Implement 3-bit parity generator & checker using logic gates.** |
| **(23)**  **Design & Implement 3-bit Synchronous U/D counter using control switch M.**  **When M=0 up counting**  **When M=1 down counting use IC-4027 / 7476.** |
| **(24)**  **Design & Implement 4-bit Excess-3 code to BCD code converter Circuit.** |
| **(25)**  **Design & Implement the following function**  **F(A,B,C,D)=∑m( 1,3,5,7,9,11,13,15) using 8:1 multiplexer.** |
| **(26)**  **Design & Implement 1:2 Demultiplexer using logic gates.**  **Verify the function table of IC-74LS138.** |
| **(27)**  **Verify the function table of IC-74LS138.**  **Design & Implement 3 bit binary to 3 bit gray code converter using**  **IC 74138.** |
| **(28)**  **Design & Implement 3-bit Asynchronous U/D counter using IC 4027/IC 7476.** |