

# Cache Quiz

**Due** Mar 12 at 11:59pm**Points** 100**Questions** 11**Available** until Mar 13 at 11:59pm**Time Limit** None**Allowed Attempts** 3

## Instructions

- This quiz should be done by yourself
- If you have questions please come to office hours
- If you find any mistakes in any of the questions, please let us know about them and we will fix them as soon as possible.

[Take the Quiz Again](#)

## Attempt History

	Attempt	Time	Score
KEPT	<a href="#">Attempt 2</a>	51 minutes	87.96 out of 100
LATEST	<a href="#">Attempt 2</a>	51 minutes	87.96 out of 100
	<a href="#">Attempt 1</a>	21,431 minutes	82.24 out of 100

❗ Correct answers are hidden.

Score for this attempt: **87.96** out of 100

Submitted Mar 12 at 6:56pm

This attempt took 51 minutes.

### Question 1

**9 / 9 pts**

You have a Direct Mapped cache with following parameters

Cache Data Size (C)	128
Block Size (b)	4

After partitioning the address, which is 32 bits big, into Tag, Set, and Offset, how many bits will be in each field?

	Tag	Set	Offset
Bits per field	[ Select ] ▼	[ Select ] ▼	[ Select ] ▼

**Answer 1:**

25

**Answer 2:**

5

**Answer 3:**

2

Partial

## Question 2

3 / 9 pts

You have a Fully Associative cache with following parameters

Cache Data Size (C)	8192
Block Size (b)	64

After partitioning the address, which is 32 bits big, into Tag, Set, and Offset, how many bits will be in each field?

	Tag	Set	Offset
Bits per field	21	5	6

**Answer 1:**

21

**Answer 2:**

5

**Answer 3:**

6

**Question 3****9 / 9 pts**

You have a K-Way set associative cache with following parameters

Cache Data Size (C)	2048
Block Size (b)	16
Blocks/Ways per set (K)	4

After partitioning the address, which is 32 bits big, into Tag, Set, and Offset, how many bits will be in each field?

	Tag	Set	Offset
Bits per field	<input type="text" value="[ Select ]"/>	<input type="text" value="[ Select ]"/>	<input type="text" value="[ Select ]"/>

**Answer 1:**

23

**Answer 2:**

5

**Answer 3:**

4

**Question 4****9 / 9 pts**

You have a single level cache system with the following setup

- CPU -- Cache -- Memory

The system has the following properties

Cache Access Time	763ns
Cache Hit Rate	76%
Memory Access Time	2,397ns

What is the average memory access time?

Report your answer to **TWO** decimal places.

**Question 5****9 / 9 pts**

You have a two-level cache system with the following set up

- CPU -- Cache 1 -- Cache 2 -- Memory

The system has the following properties

Cache1 Access Time	40ns
Cache1 Hit Rate	75%
Cache2 Access Time	257ns
Cache2 Hit Rate	90%
Memory Access Time	2,264ns

What is the average memory access time?

Report your answer to **TWO** decimal places.

## Question 6

9 / 9 pts

You have a three-level cache system with the following set up

- CPU -- Cache 1 -- Cache 2 -- Cache 3 -- Memory

The system has the following properties

Cache1 Access Time	26ns
Cache1 Hit Rate	92%
Cache2 Access Time	298ns
Cache2 Hit Rate	78%
Cache3 Access Time	129ns
Cache3 Hit Rate	100%
Memory Access Time	1,623ns

What is the average memory access time?

Report your answer to **TWO** decimal places.

**Question 7****9 / 9 pts**

Select all of the statements that are **TRUE**

- ☐ A Write Through Cache DOES have a dirty bit
- ☒ A Write Through Cache does NOT have a dirty bit
- ☒ A Write Back Cache DOES have a dirty bit
- ☐ A Write Back Cache does NOT have a dirty bit

**Partial****Question 8****7.2 / 9 pts**

For each of the following overhead bits, select whether there are these bits per cache, per set, per block, or per value.

- Assume the cache is a K-way set associative cache.

	Instance Per
Valid Bit	[ Select ] ▼
Dirty Bit	Block
Tag Bits	[ Select ] ▼
Counter if using FIFO replacement policy	[ Select ] ▼
Counters if using LRU replacement policy	[ Select ] ▼

**Answer 1:**

Block

**Answer 2:**

Block

**Answer 3:**

Block

**Answer 4:**

Set

**Answer 5:**

Set

Partial

## Question 9

6.43 / 9 pts

For each action, match it with when it occurs. For this problem assume the cache is a K-way set associative cache using a Least Recently Used replacement policy.

**Valid Bit Is set to 0 when**

The computer is turned

**Valid bit is set to 1 when**

The cache reads a block

**Dirty Bit is set to 0 when**

The computer is turned

**Dirty Bit is set to 1 when**

The CPU writes to this block

**A block is evicted from the cache when**

The block is not in the set

**Tag bits are written to when**

The block is not in the s

**The LRU counters of a set are updated when**

A block that maps to tha

### Question 10

9 / 9 pts

Match each type of miss with its definition.

**Compulsory Miss**

A miss that occurs beca

**Capacity Miss**

A miss that occurs beca

**Conflict Miss**

A miss that occurs beca

Partial

### Question 11

8.33 / 10 pts

For each of the cache modifications that we could perform, select whether it will increase, decrease, have no effect, or have an unknown effect on the parameter.

- An unknown effect means that it could either decrease or increase the parameter in question.
- No effect also includes marginal or very little effect
- When answering for multilevel caching, answer based on the caching system as a whole.



Improvement	Hit Rate	Cache Access Time
Increase Cache Size (C)	[ Select ] ▼	[ Select ]
Increase Associativity(K)	[ Select ] ▼	[ Select ]
Increase Block Size(b)	[ Select ] ▼	[ Select ]
Use Multilevel Caching	[ Select ] ▼	[ Select ]

**Answer 1:**

Increase

**Answer 2:**

Increase

**Answer 3:**

Unknown

**Answer 4:**

Increase

**Answer 5:**

Increase

**Answer 6:**

Unknown

**Answer 7:**

Unknown

**Answer 8:**

Increase

---

**Answer 9:**

Unknown

---

**Answer 10:**

Increase

---

**Answer 11:**

Increase

---

**Answer 12:**

Increase

Quiz Score: **87.96** out of 100