Assignment:
Scheduling Exercise

MIPS Program

```
 1:        lw        $r2, 0($r5)
 2:        subi      $r4, $r2, 1
 3:        lw        $r1, 0($r6)
 4:        add       $r3, $r0, $r4
 5:        subi      $r2, $r6, 1
 6:        subi      $r4, $r3, 5
 7:        add       $r3, $r2, $r4
 8:        lw        $r2, 0($r7)
 9:        or        $r4, $r2, $r1
10:        subi      $r7, $r3, 9
```

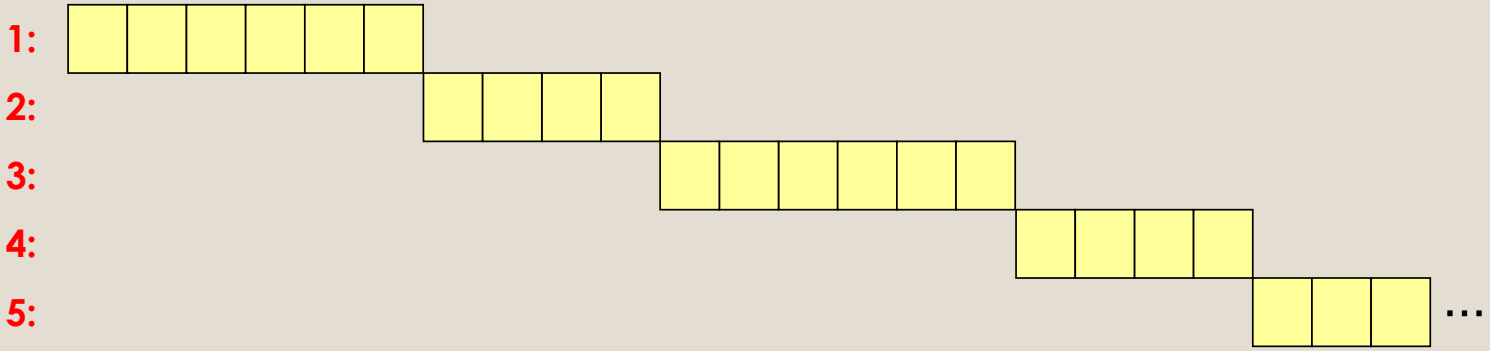
Goal of the Assignment

- Determine the execution schedule for this code in five different architectures (and indicate all forwarding paths used)
- Compare the number of cycles required by the five architectures
- Compute the CPI of all architectures on this program

Architecture #1

- Sequential execution: a processor with no pipelining
- Execution latencies:
  - ALU Operations → 4 cycles
  - Memory Operations → 6 cycles

Solution: Schedule on Architecture #1




```
1:lw    $r2, 0($r5)
2:subi  $r4, $r2, 1
3:lw    $r1, 0($r6)
4:add   $r3, $r0, $r4
5:subi  $r2, $r6, 1
6:subi  $r4, $r3, 5
7:add   $r3, $r2, $r4
8:lw    $r2, 0($r7)
9:or    $r4, $r2, $r1
10:subi $r7, $r3, 9
```

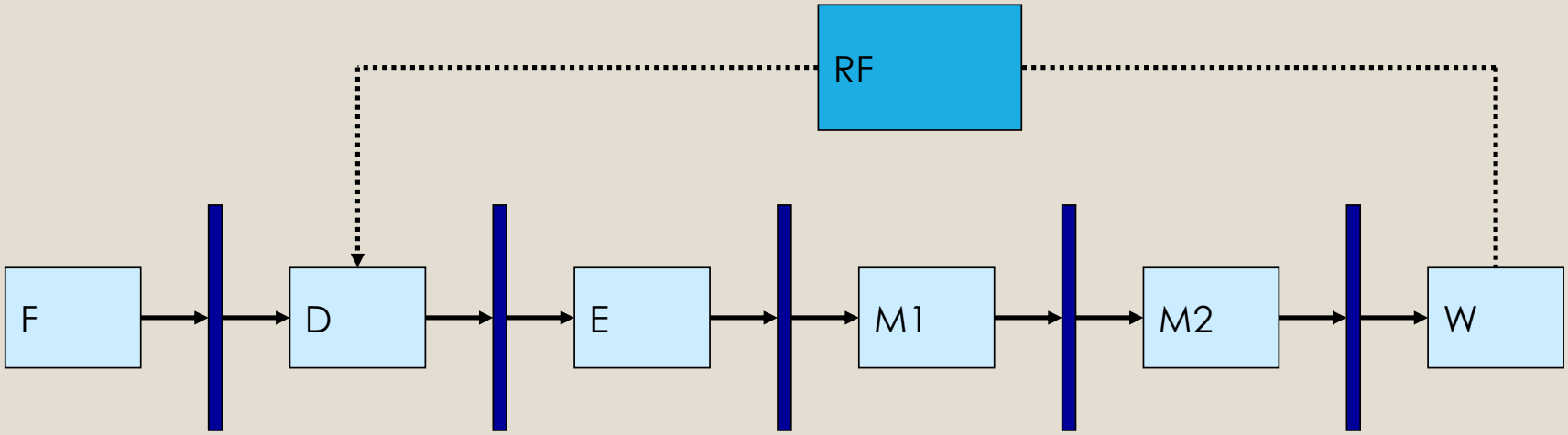
→ 6 cycles
→ 4 cycles
→ 6 cycles
→ 4 cycles
→ 4 cycles
→ 4 cycles
→ 4 cycles
→ 6 cycles
→ 4 cycles
→ 4 cycles

= **46 cycles**

CPI = 46/10 = 4.6

Architecture #2

- 6-stage pipelined, no forwarding paths

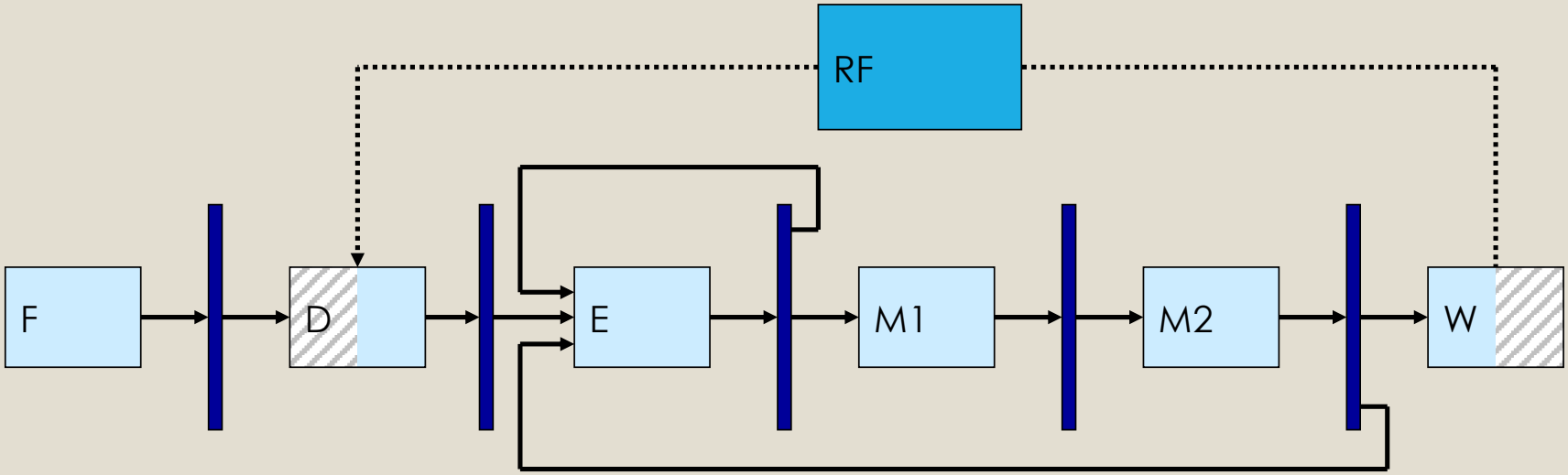


Schedule on Architecture #2

?

Architecture #3

- 6-stage pipelined, <u>some</u> forwarding paths:
  - **E→E**, **M2→E**
  - **W→D**

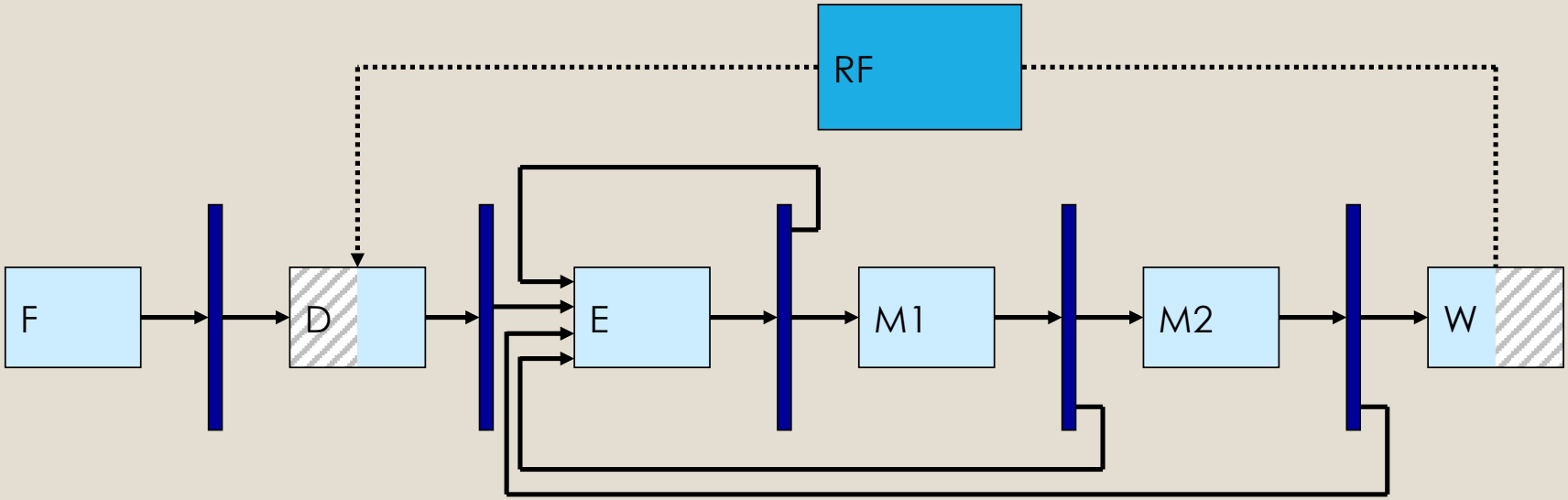


Schedule on Architecture #3

?

Architecture #4

- 6-stage pipelined, all forwarding paths:
  - **E→E**, **M1→E**, **M2→E**
  - **W→D**

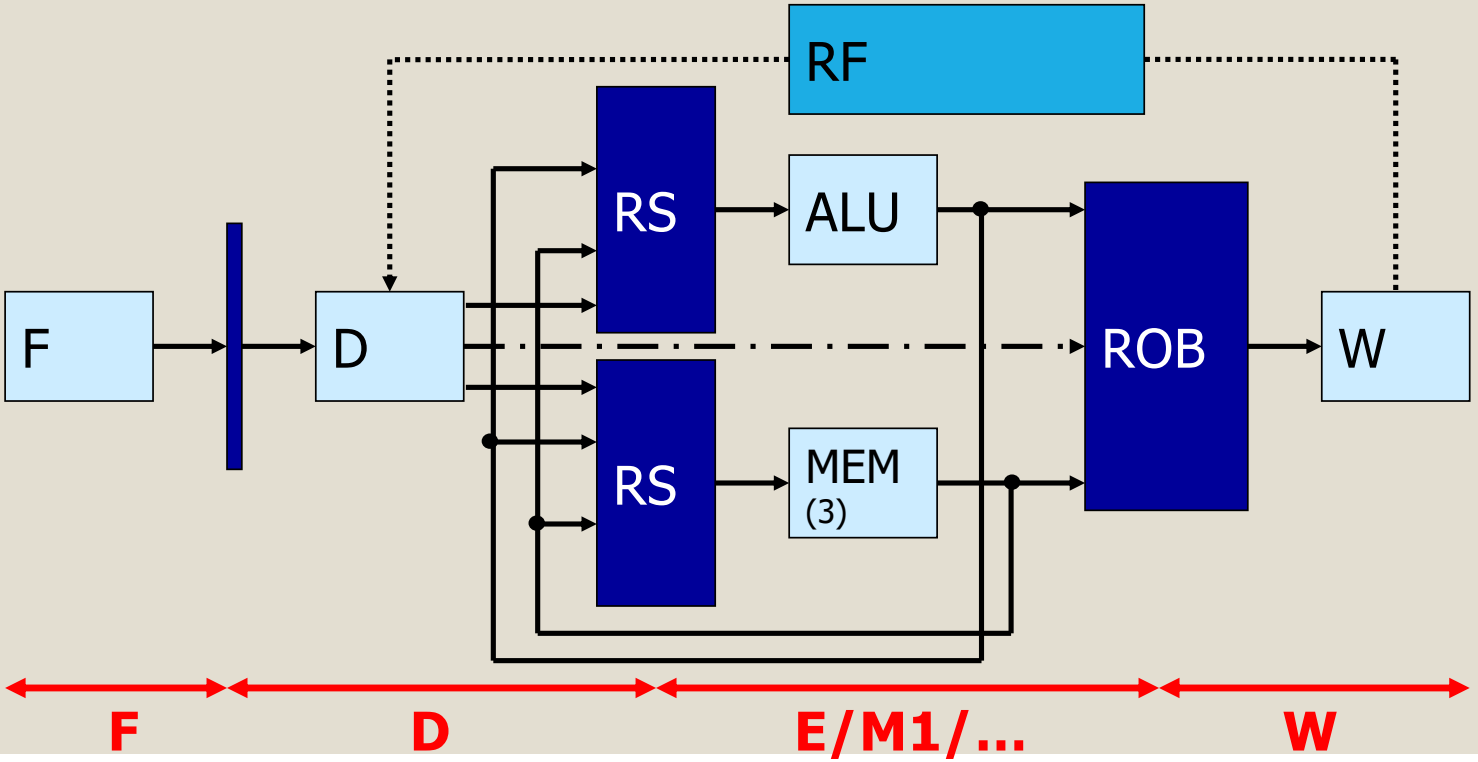


Schedule on Architecture #4

?

Architecture #5

- Dynamically scheduled, out-of-order (OOO) execution. Assume in-order commit
- 1 ALU (latency 1) , 1 Memory Unit (latency 3)



Schedule on Architecture #5