VL 503 - Digital CMOS VLSI Design
Project Proposal

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Paper Topic:

High-speed hybrid logic full adder using high performance 10-T XOR/X-NOR cell:

https://ieeexplore.ieee.org/document/9068497

The paper presents several key outcomes:

1. Simulation of circuits in a 90-nm generic process design kit (GPDK) CMOS process technology using Cadence Virtuoso.
2. Comparative analysis of the proposed XOR-XNOR design with other existing designs and traditional designs concerning delay and power.
3. Examination of Full adder circuit designs using a high-performance 10-T XOR/XNOR cell to estimate power and delay.
4. Comparison of various n-bit adders (e.g., 2-bit, 4-bit, etc.) in terms of delay, power, power-delay product (PDP), across four proposed designs and designs from previously published papers.
5. Evaluation of different proposed Full Adder designs under process corner variations.
6. Layout design of the proposed XOR-XNOR circuit and the best proposed Full Adder design.

The intended implementation of these results involves:

1. Putting the proposed XOR-XNOR circuits into practice using Cadence and validating their performance by comparing them with other suggested designs and traditional designs in terms of delay and power.
2. Implementing the Full adder circuits as outlined in the paper and previous publications, employing the simulated XOR-XNOR circuits and confirming the power and delay comparisons presented in the paper.