

VL 503- Digital CMOS VLSI Design Project Report

High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR–XNOR Cell

Link to paper: <https://ieeexplore.ieee.org/document/9068497>

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Results we planned to implement:

- Implement the proposed XOR-XNOR circuits in cadence and verify the results with other suggested designs and conventional design for delay and power.
- Implement the proposed Full adder circuits in the paper and the previously published papers using the simulated XOR-XNOR circuits and verify the power and delay comparisons made in the paper.

Results we implemented:

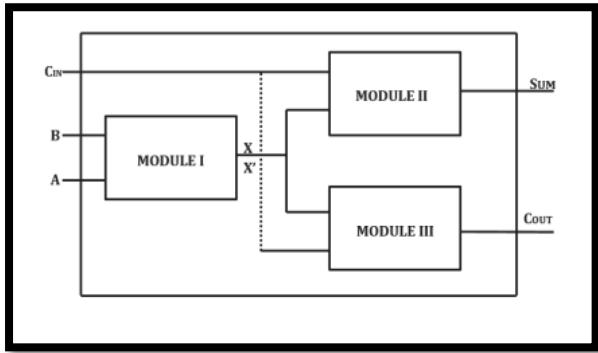
- We implemented all the proposed hybrid logic style XOR-XNOR circuits in cadence and plotted their respective input/output waveforms.
- We implemented Bhattacharyya's Full Adder Circuit and compared its performance with the XOR-XNOR FA circuits.
- Compared 2,4,8 bit cascaded adders of the proposed XOR-XNOR circuits with Bhattacharyya's FA.

INTRODUCTION:

- Hybrid logic style is used to implement full adder (FA) circuits. Performance of hybrid FA depends on the performance of XOR-XNOR circuit. This paper proposes a high-speed, low-power 10-T XOR-XNOR circuit.
- The performance is measured by simulating it in cadence virtuoso environment using 90-nm CMOS technology.
- Four different designs of FAs are proposed in the paper using the proposed XOR-XNOR, sum and carry modules.

- To measure the driving capabilities, the FAs are converted into 2-, 4- and 8-bit cascaded full adders (CFA)

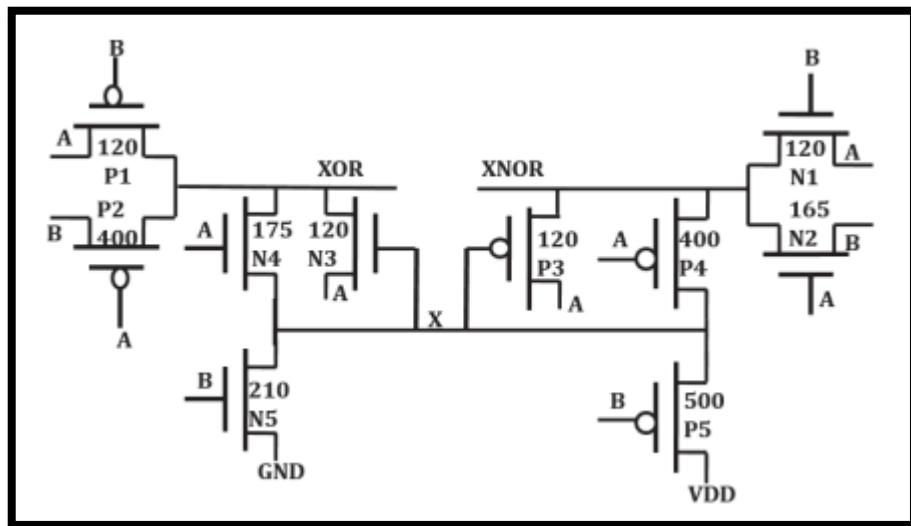
Schematic of hybrid logic FA circuit:



Module I : Proposed XOR-XNOR circuit generates full swing output of 2 input signals- A and B

Module II and III : Sum and Carry circuits which produces Cout and Sum using outputs of module I and input signal- Cin

Proposed XOR-XNOR Circuit in the paper:



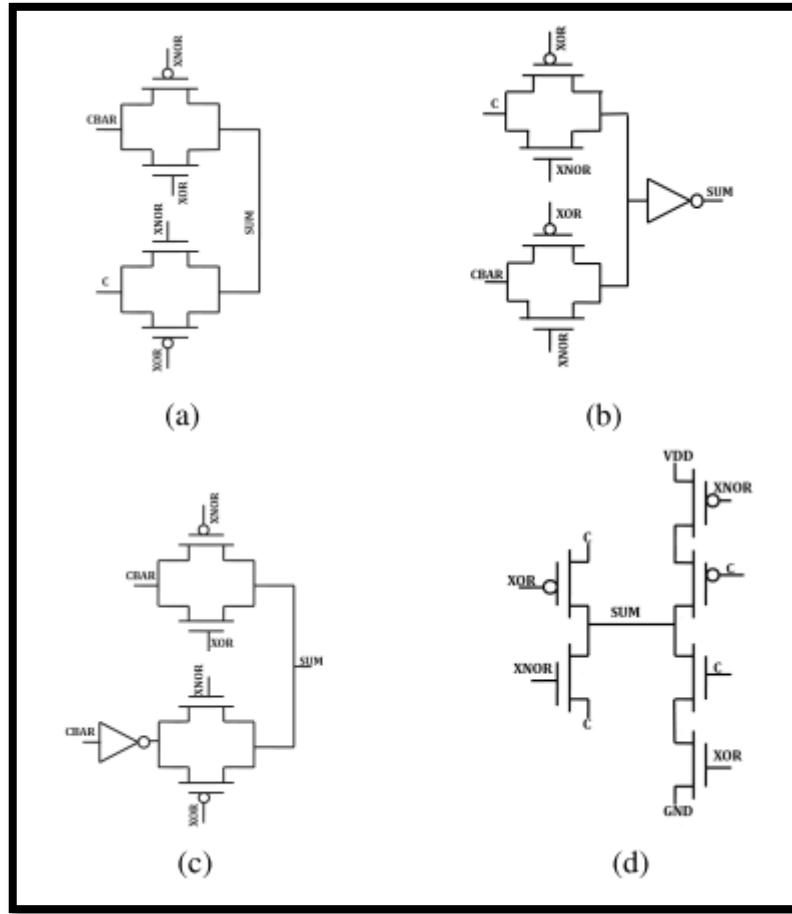
- Structure uses 2 pMOS(P1 and P2) and 3 nMOS (N3, N4 and N5) at XOR output side and 2 nMOS (N1 and N2) and 3 pMOS (P3, P4 and P5) at the XNOR output side.
- In the circuit NOT logic has been included without using external NOT gate. Thus, capacitance equal to one inverter at the input is reduced which reduces the overall delay.
- The output nodes of the circuit are charged or discharged through different paths for different input combinations. Therefore, it has different delay for different input combinations.

Proposed SUM Circuit:

$$\text{SUM} = (A \oplus B) \oplus C'_{\text{IN}} + (A \oplus B)' \oplus C_{\text{IN}}$$

Equation of SUM

4 different designs of the SUM circuit are shown below:



Description of the SUM circuits:

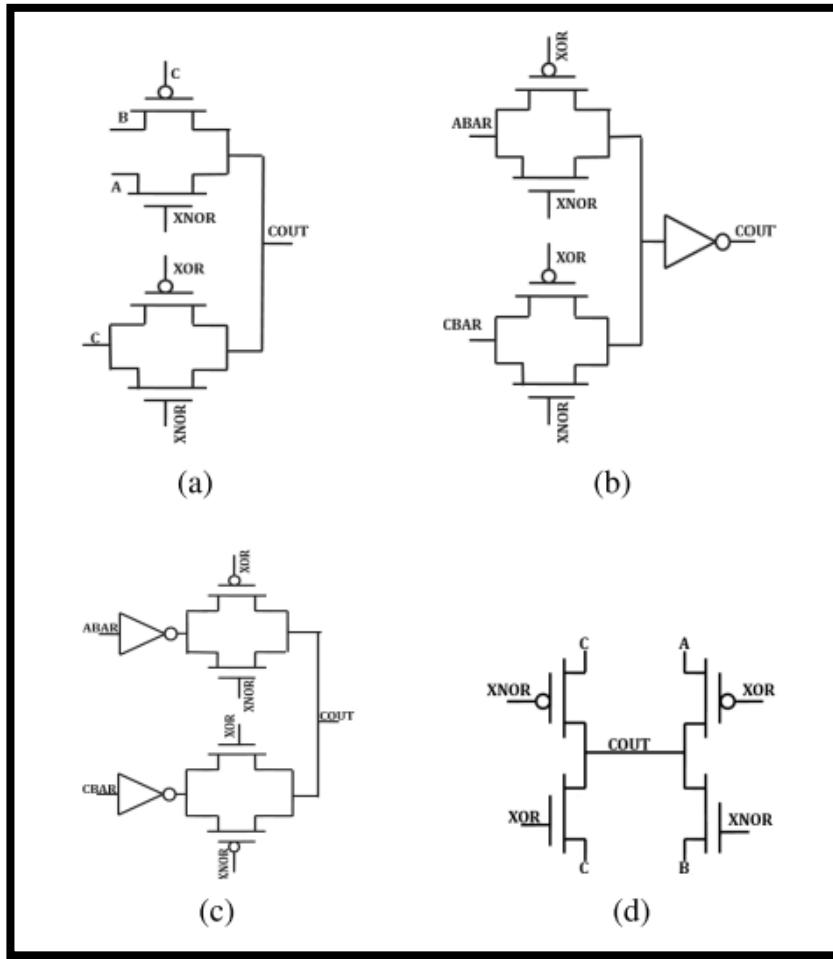
- It is implemented using Transmission Gates (TG) as 2 to 1 multiplexer. XOR and XNOR signals are used as inputs to the gate and Cin and Cin' are used as input to the sources of two TGs. The circuit provides worst performance in the cascading systems since it has a driving capability problem due to creation of parasitic capacitance and resistance.
- To overcome the driving capability issue, an inverter is added at the output. This extra inverter leads to higher power consumption.
- A buffer (Cin' followed by an inverter) is used at the input side. The buffer at the input increases driving capability of the circuit.
- A CMOS logic style based circuit is made which provides good driving capability.

Proposed Carry Circuit:

$$C_{OUT} = (A \oplus B)'A + (A \oplus B)C_{IN}.$$

Equation of Carry

4 different designs of the Carry circuit are shown below:

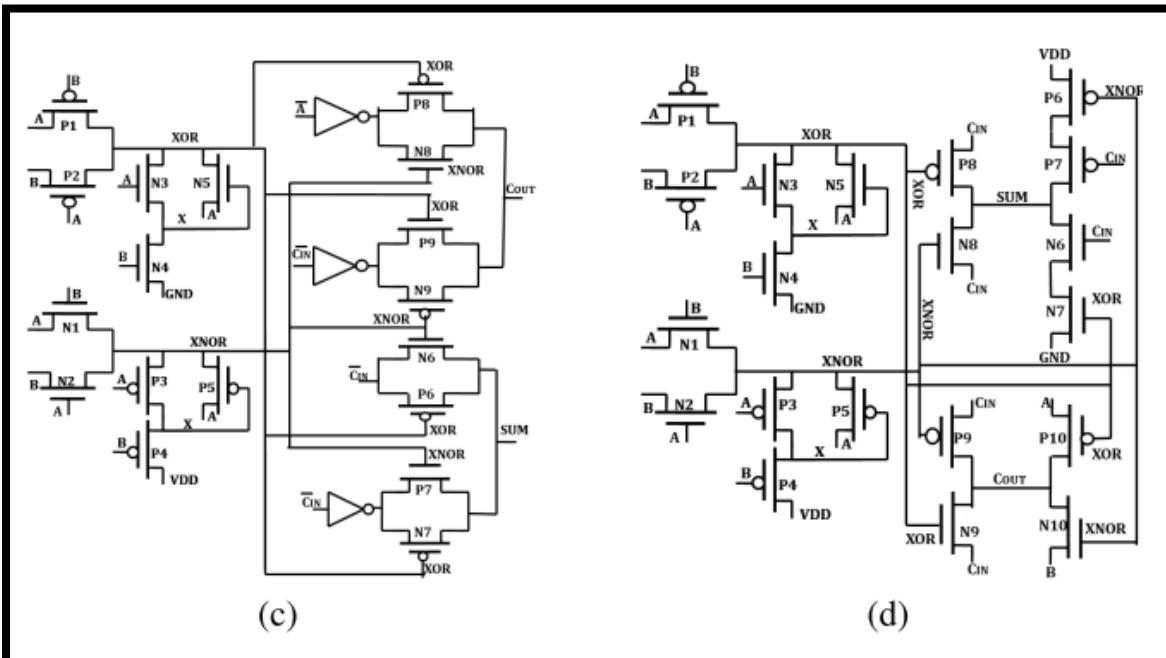
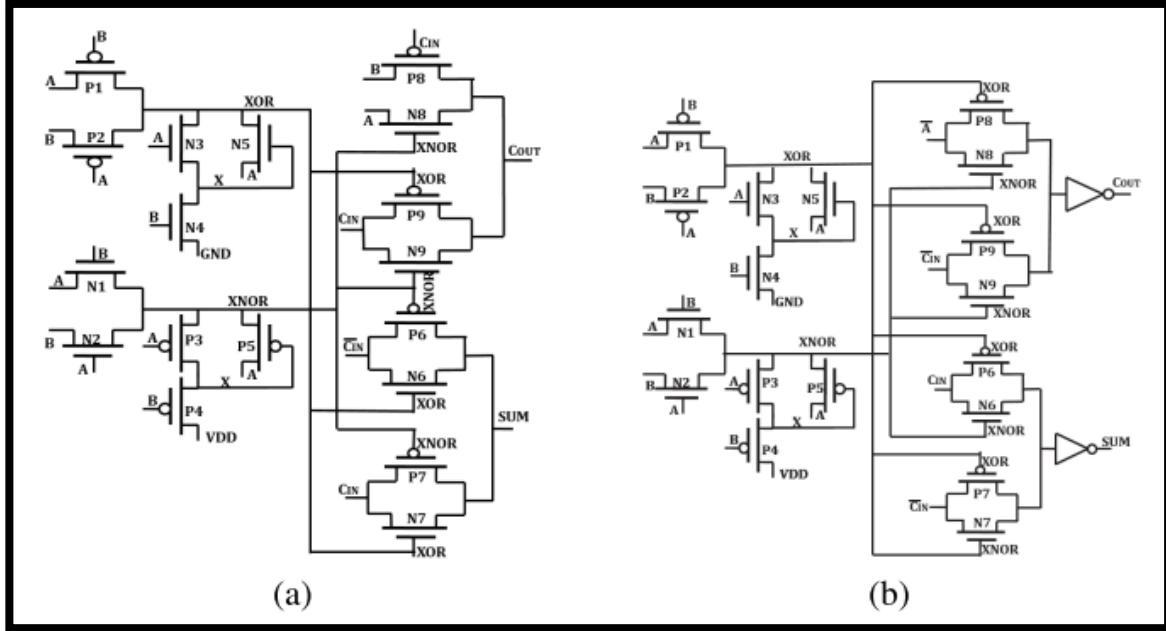


Description of the Carry circuits:

- Cout is generated by passing the value of either A or B or Cin at the output based on intermediate signals (output of module I).
- For improving the driving capability of circuit (a), a buffer (as an inverter) is added at the output. This leads to higher power consumption.
- For improving the driving capability of circuit (a), a buffer (A' followed by an inverter and Cin' followed by an inverter) is added in the input side. This leads to higher delay.
- A CMOS logic style based circuit uses 4 transistors and consumes lesser power and providing better delay performance is proposed.

Full Adder Circuits:

- The hybrid-logic FA is designed by combining the above 3 modules.
- Following 4 circuits are built using the proposed XOR-XNOR circuit and 4 different SUM and Carry modules.

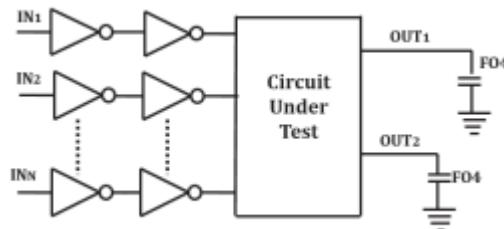


Description of the circuits:

1. Hybrid FA design-1 (FA1) built using XOR-XNOR circuit and TG-based SUM and Carry circuits. This circuit has driving capability problems in the cascaded stages such as ripple carry adder. The circuit uses 20 transistors.
2. Hybrid FA design-2 (FA2) uses 26 transistors and has better driving capability by using buffers at the output of SUM and Carry modules.
3. Hybrid FA design-3 (FA3) also uses 26 transistors. It uses inverters on the input side in SUM and Carry modules.
4. Hybrid FA design-4 (FA4) is implemented using CMOS logic style and uses 20 transistors. This circuit gives the best performance in terms of PDP among all the other FAs.

Simulations:

- We have simulated the circuits using cadence virtuoso in 90-nm generic process design kit (GPKD) CMOS process technology.
- Supply voltage and maximum operating frequency are taken as 1.2V and 1GHz respectively.
- The testbench passes input to the circuits through 2 inverters and uses capacitive load equivalent to FO4 at the output.

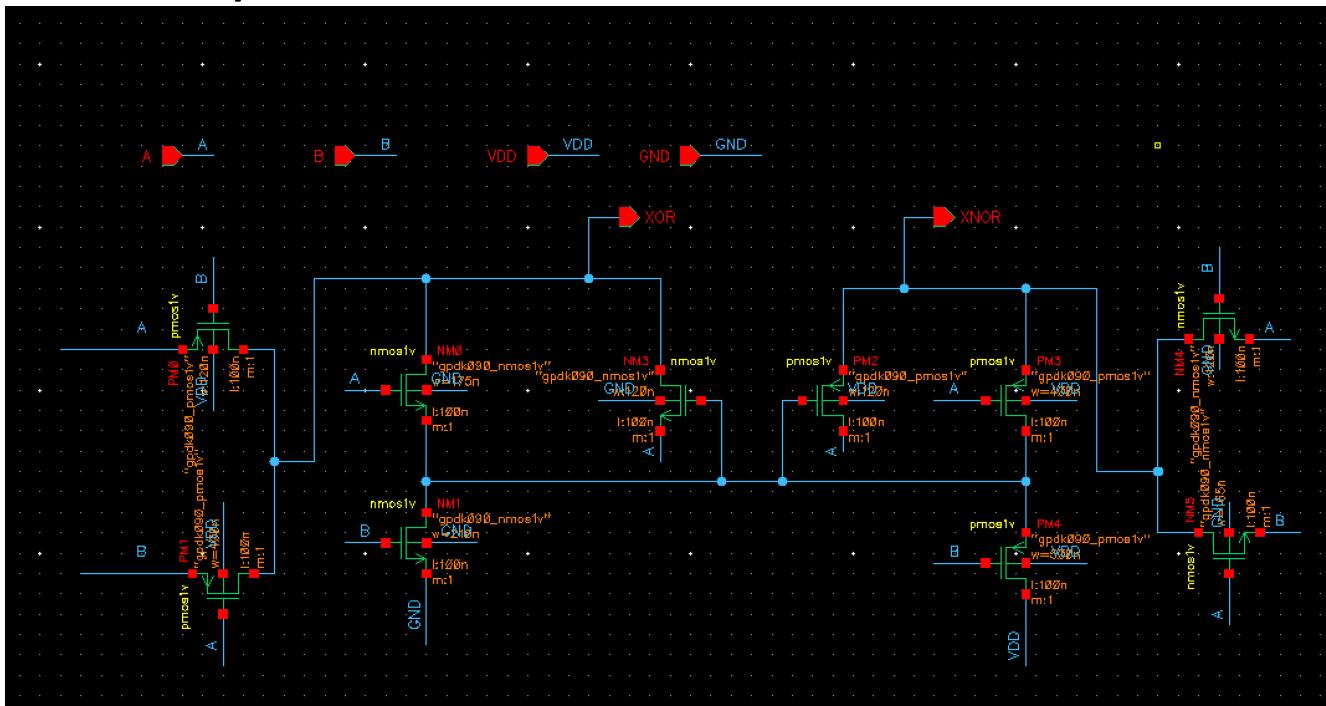


Testbench for simulation of the circuits

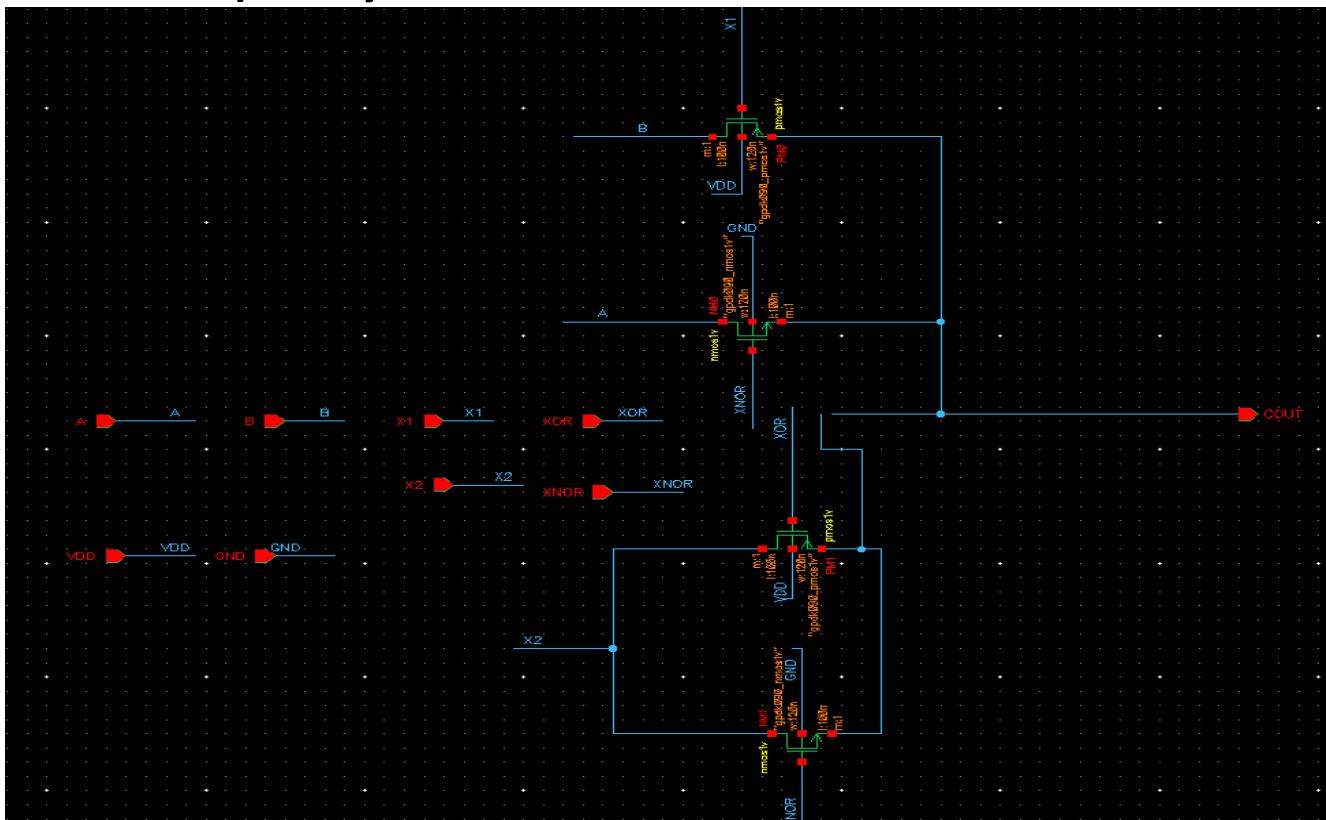
Circuit simulations:

1. Full Adder 1 (Design-1)

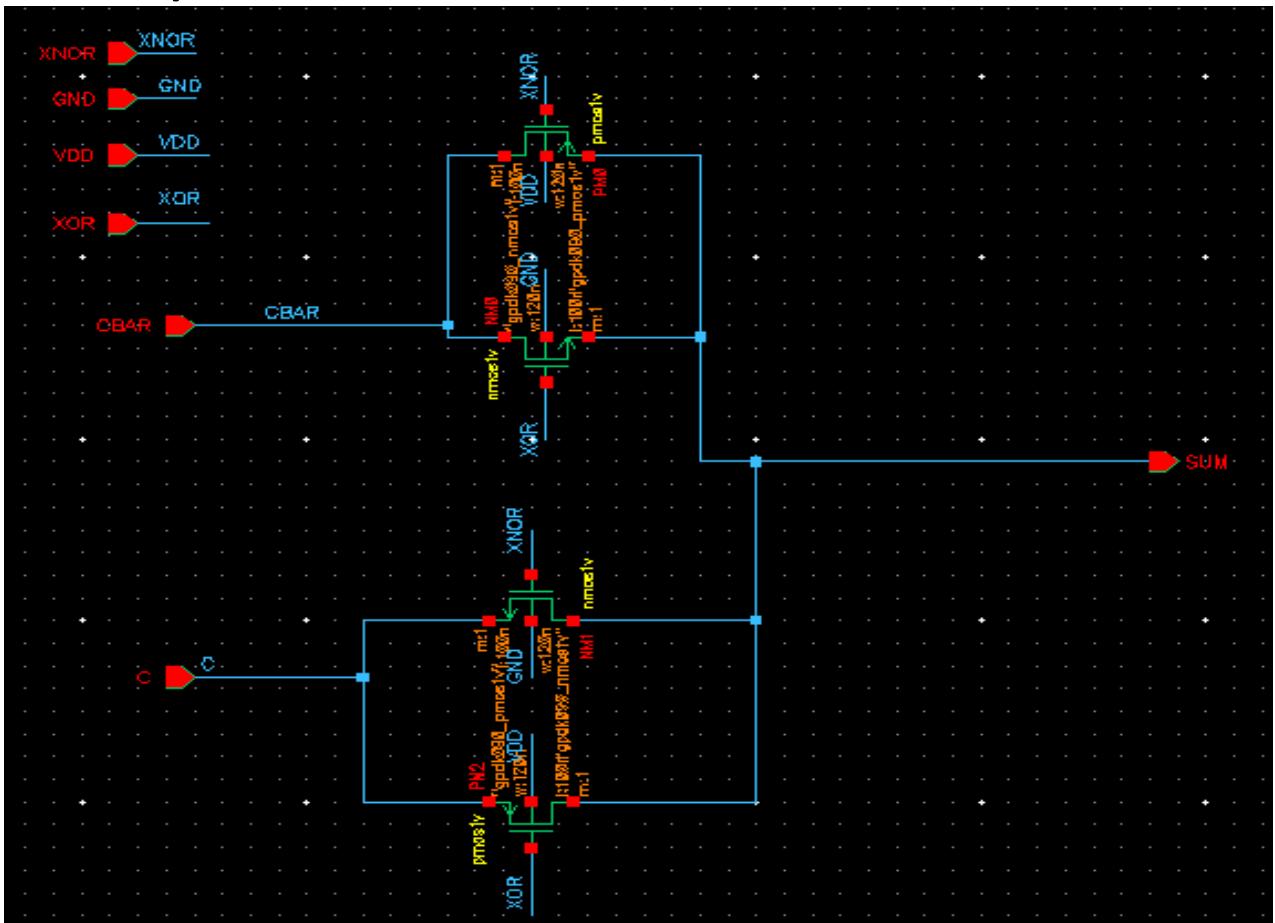
a) XOR-XNOR circuit



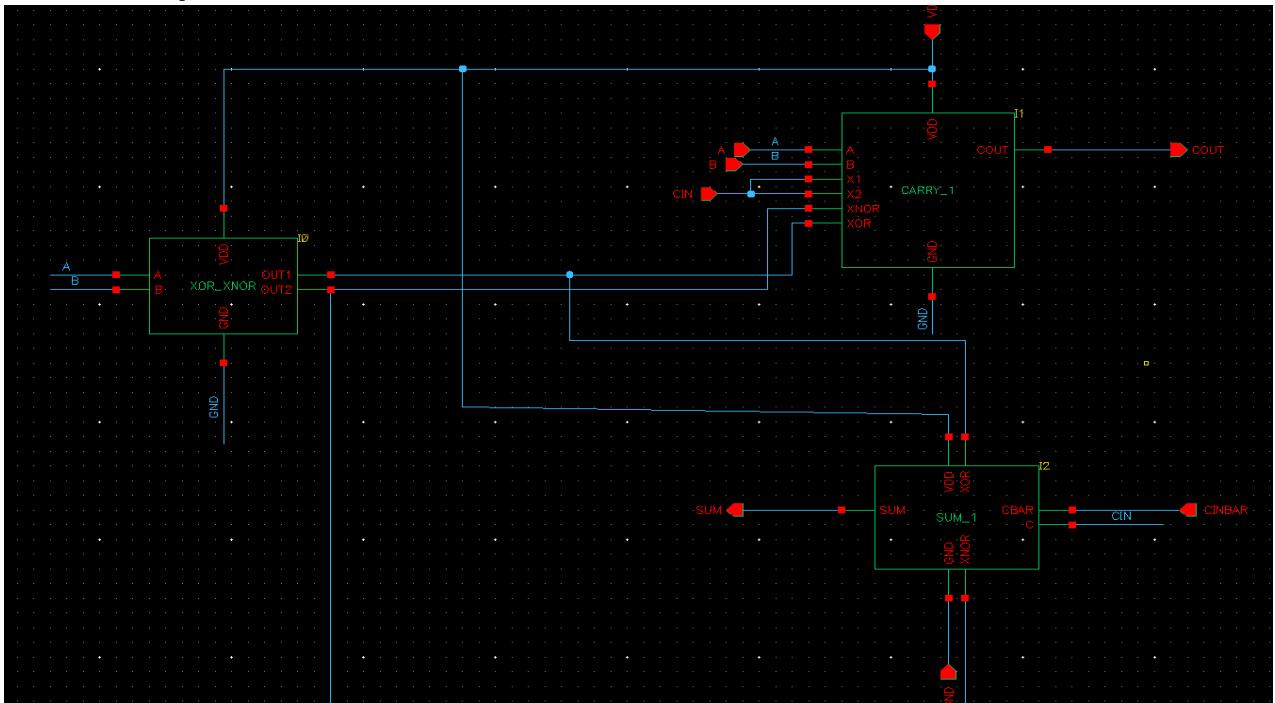
b) Carry module of FA1



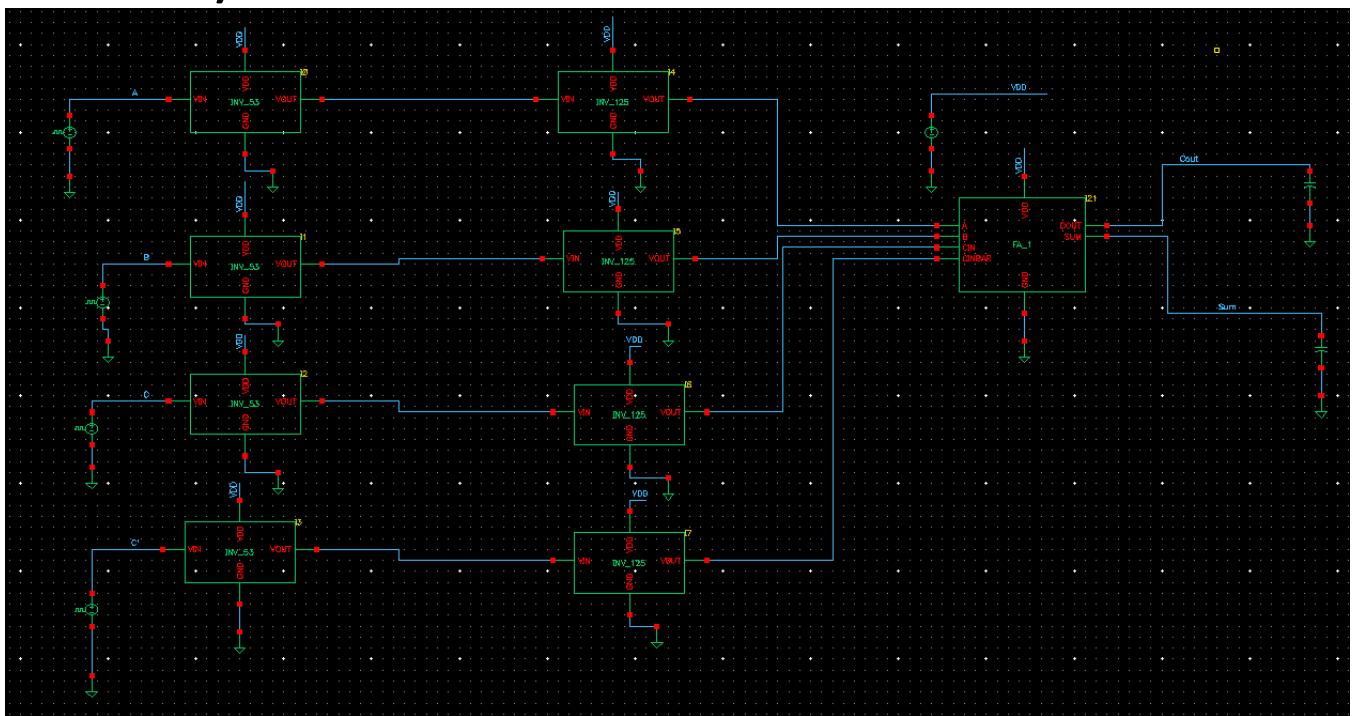
c) Sum module of FA1



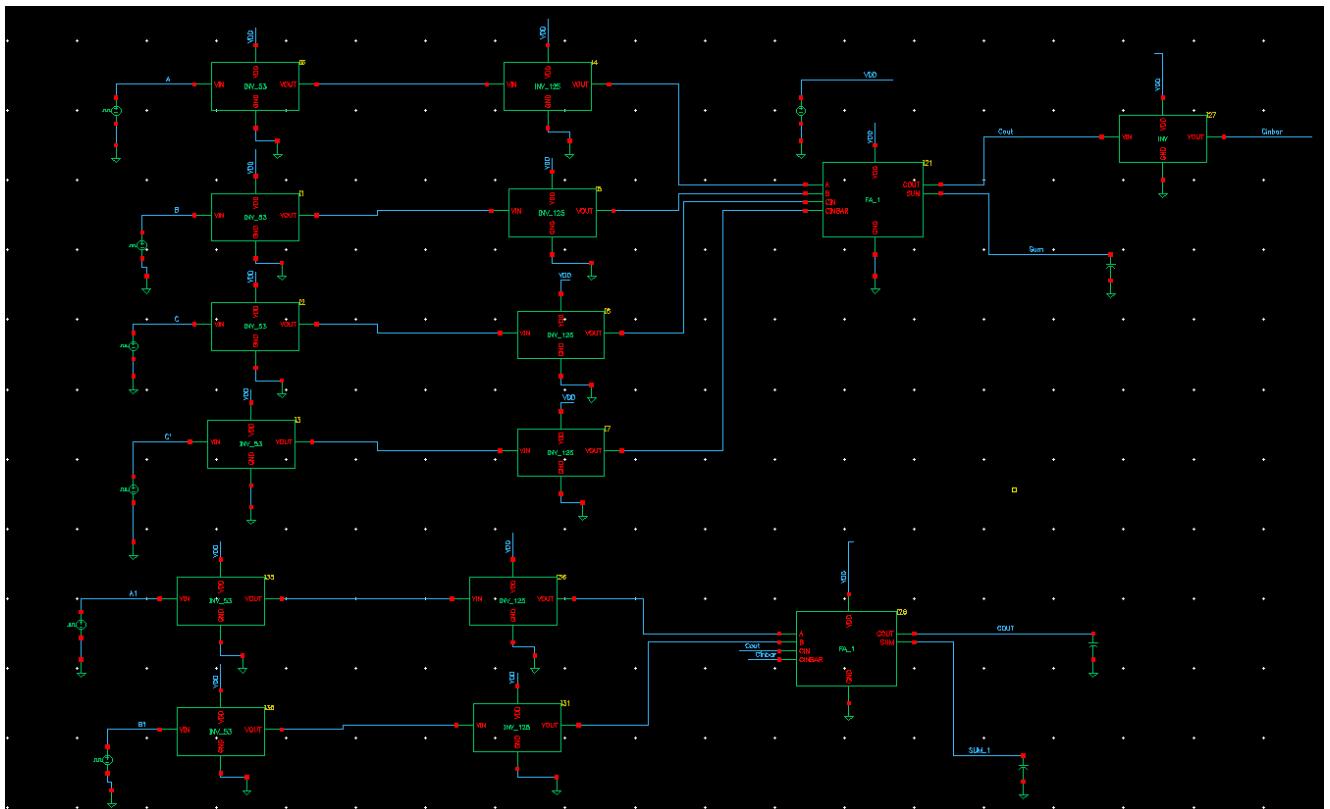
d) FA1 circuit



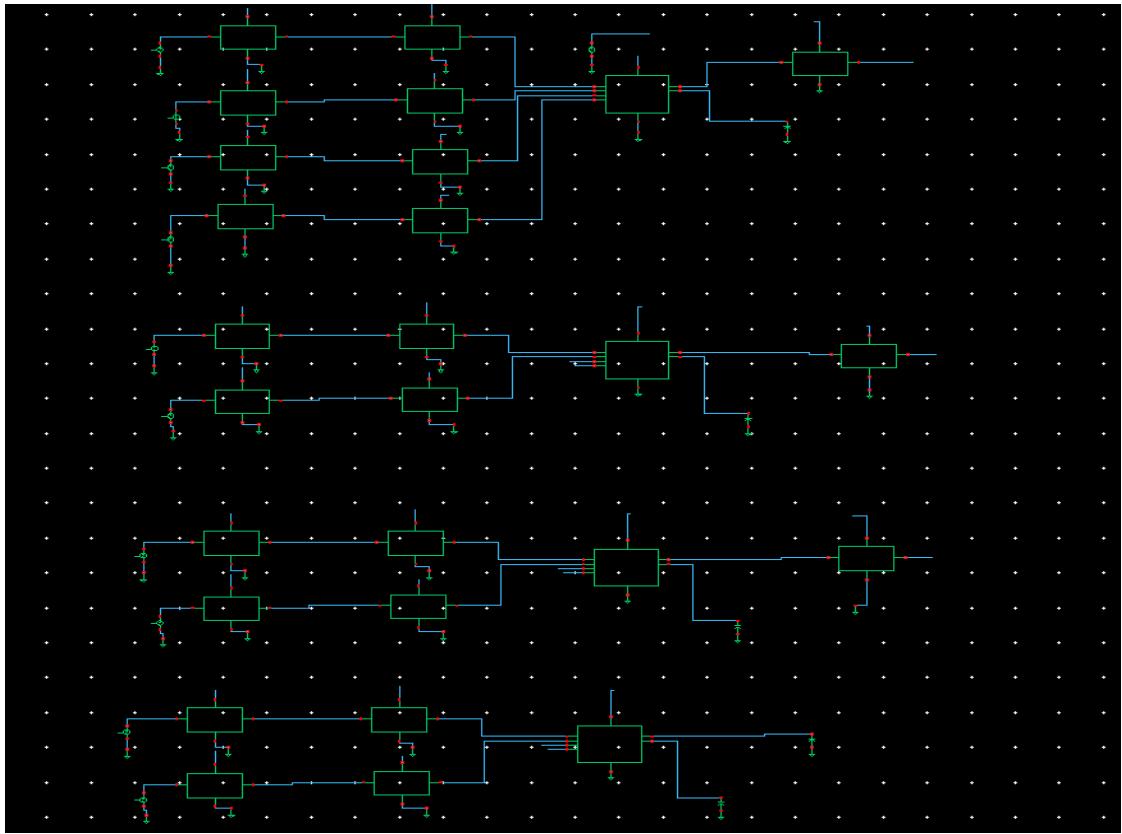
e) FA1 test bench



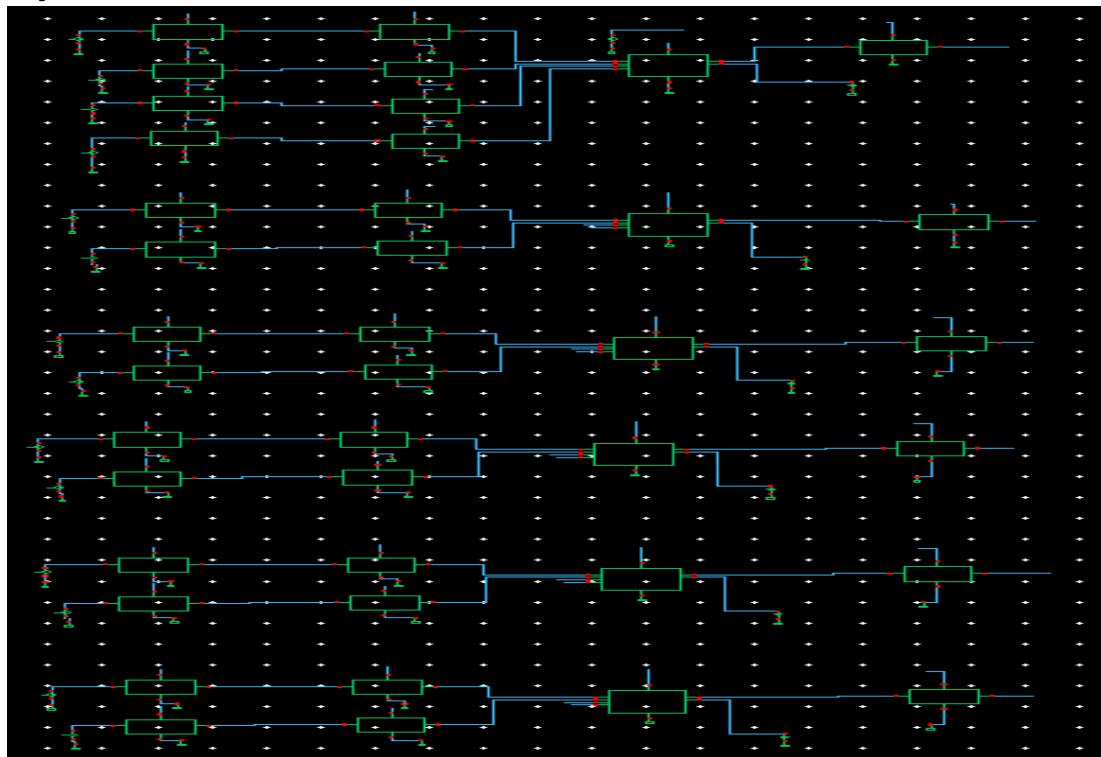
f) 2-bit FA1



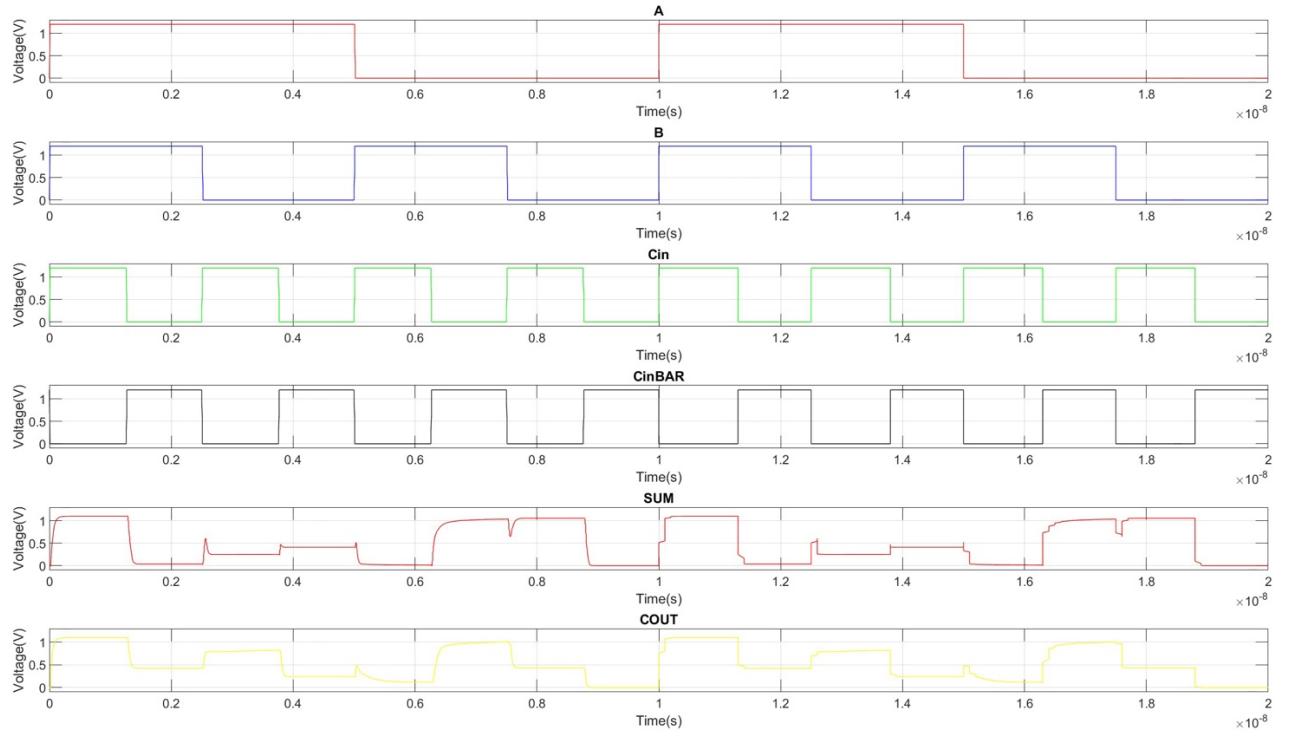
g) 4-bit FA1



h) 8-bit FA1

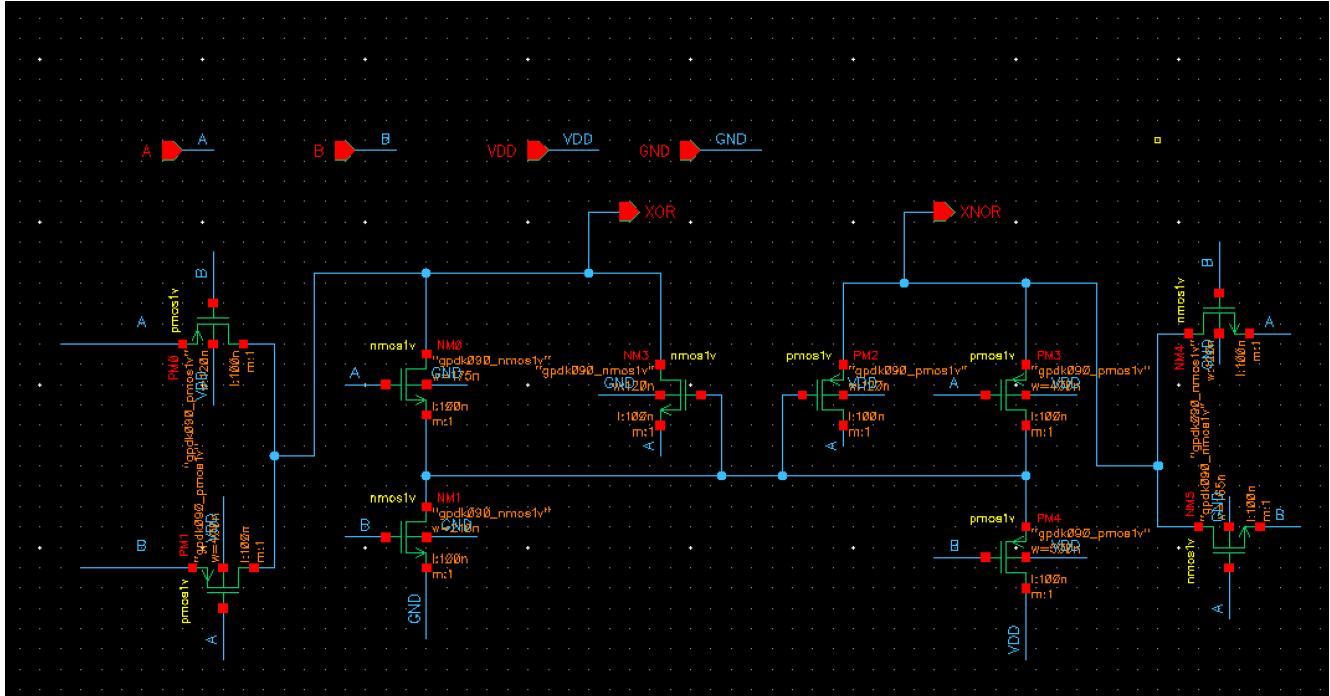


i) FA1 waveforms

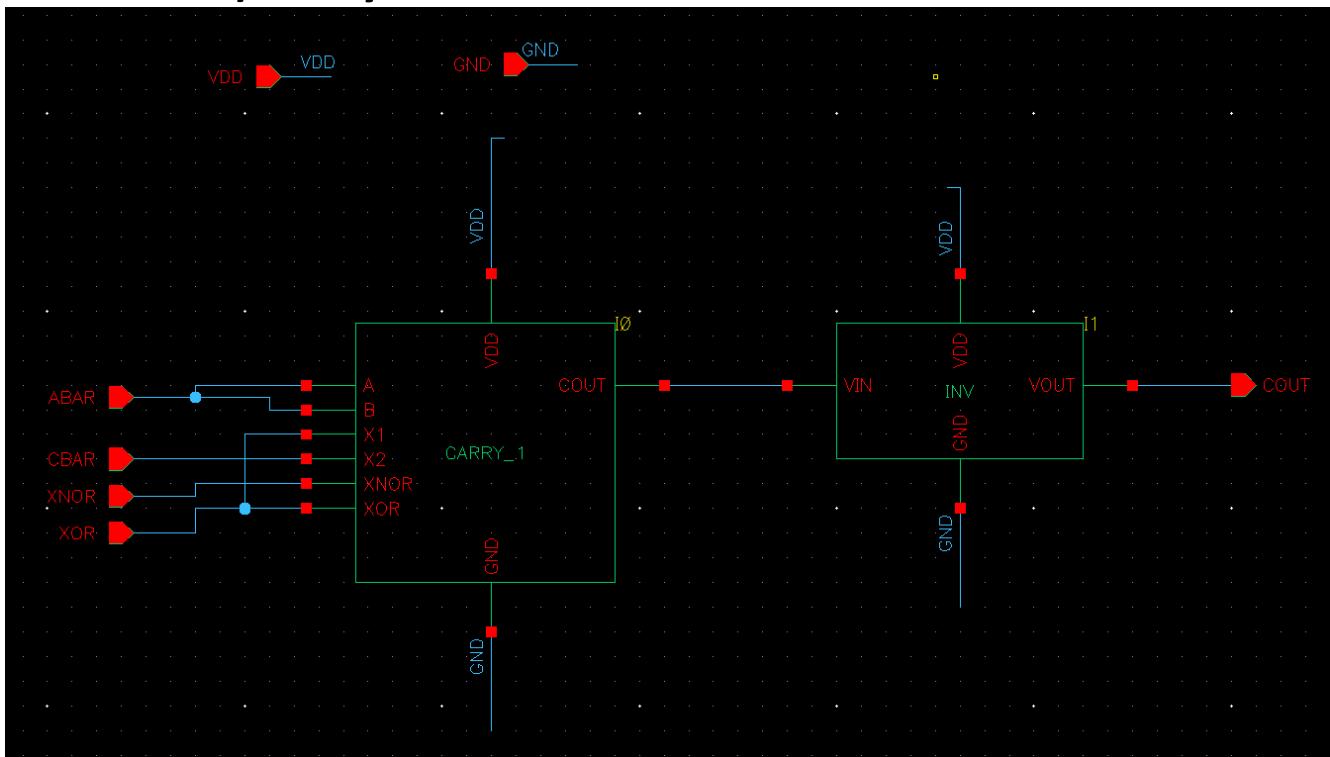


2. Full Adder 2 (Design-2)

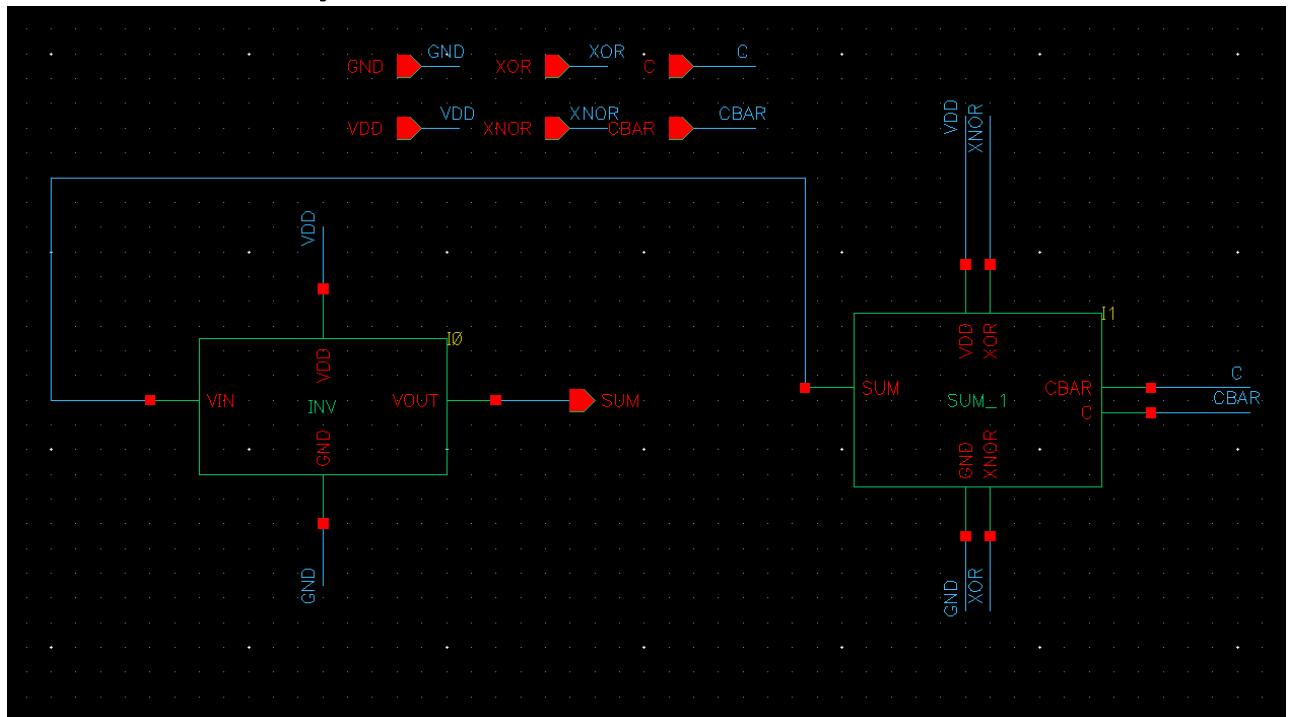
a) XOR-XNOR circuit



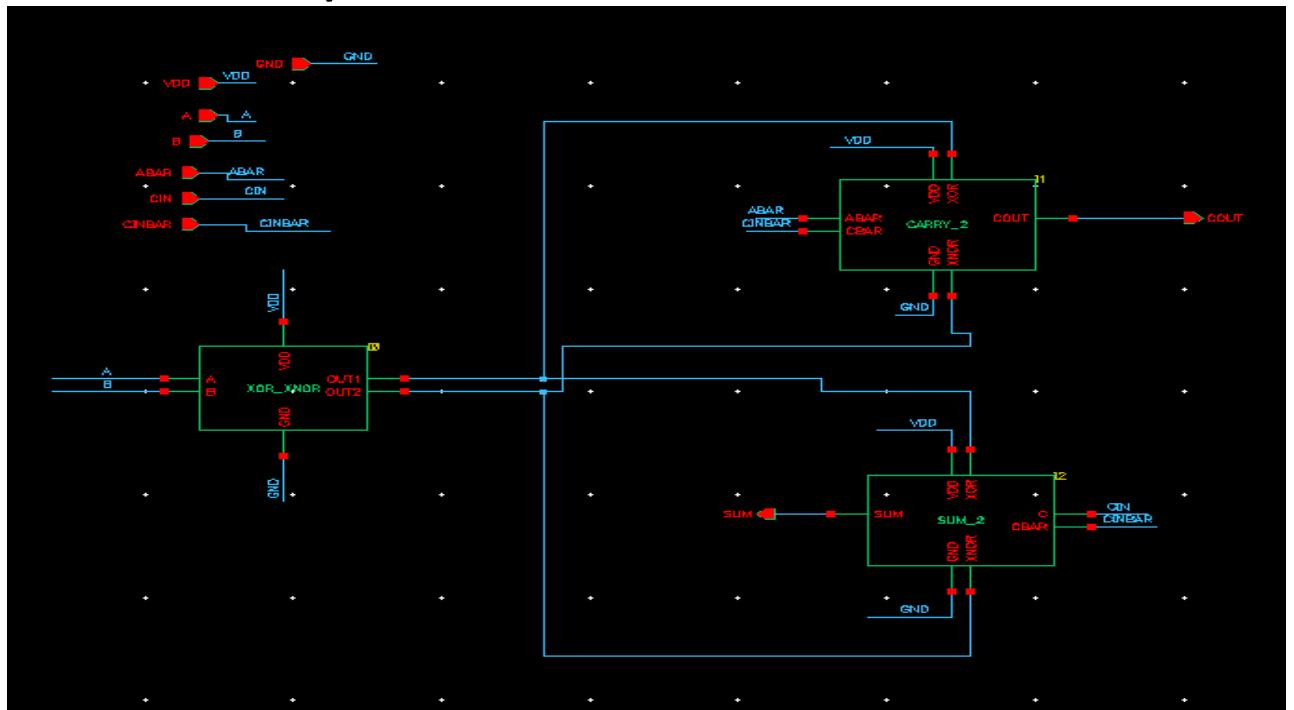
b) Carry module of FA2



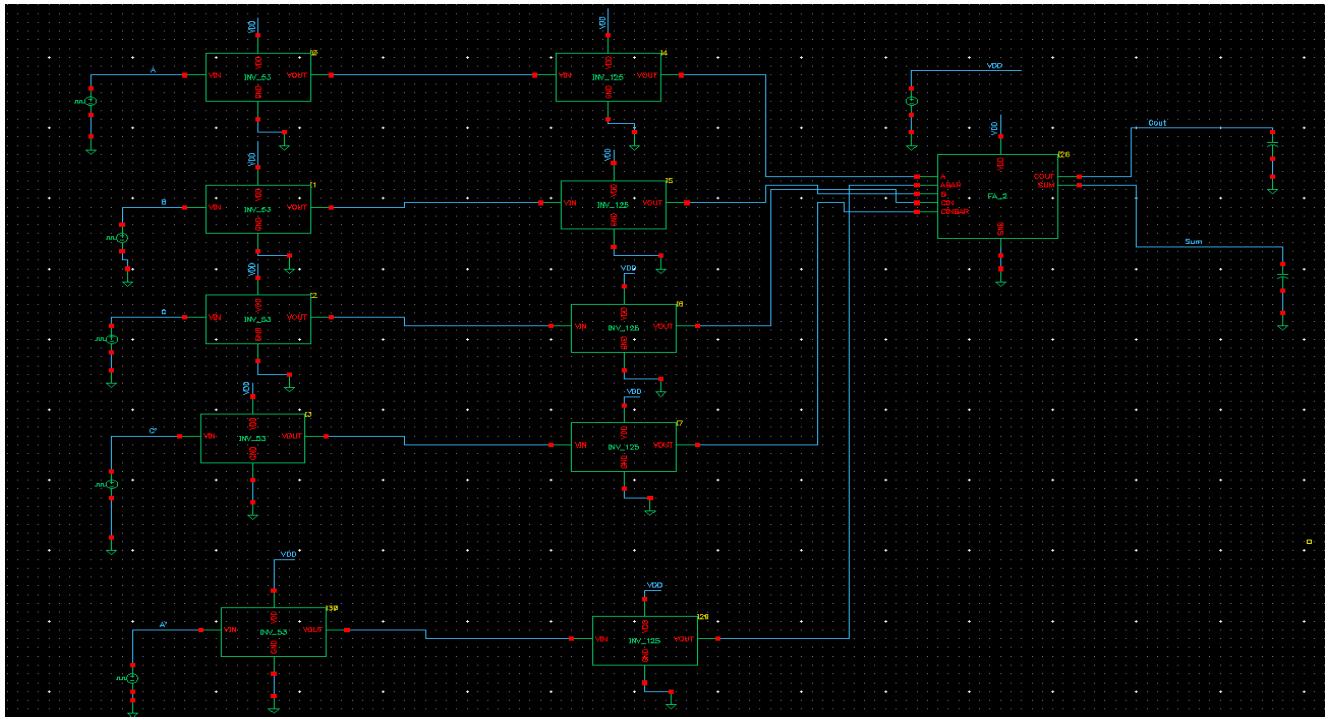
c) Sum module of FA2



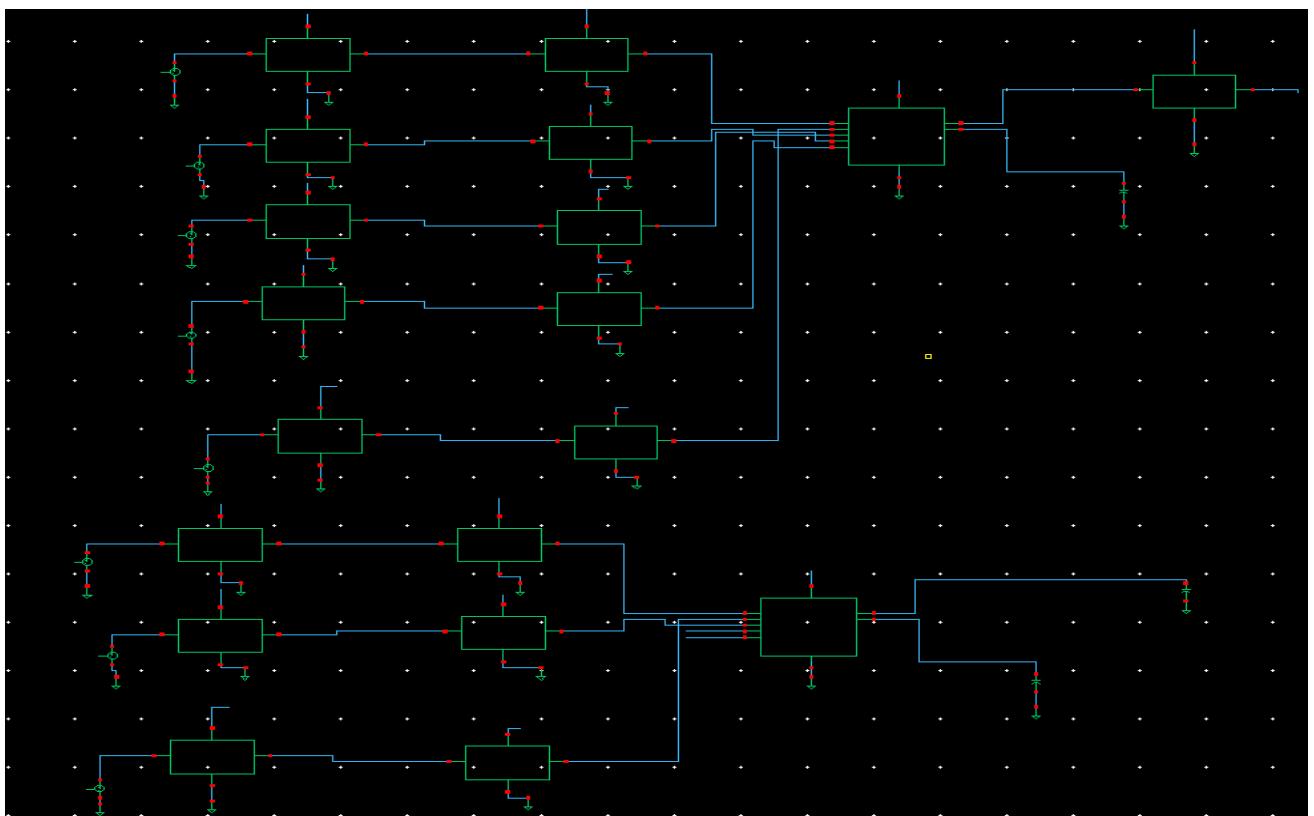
d) FA2 circuit



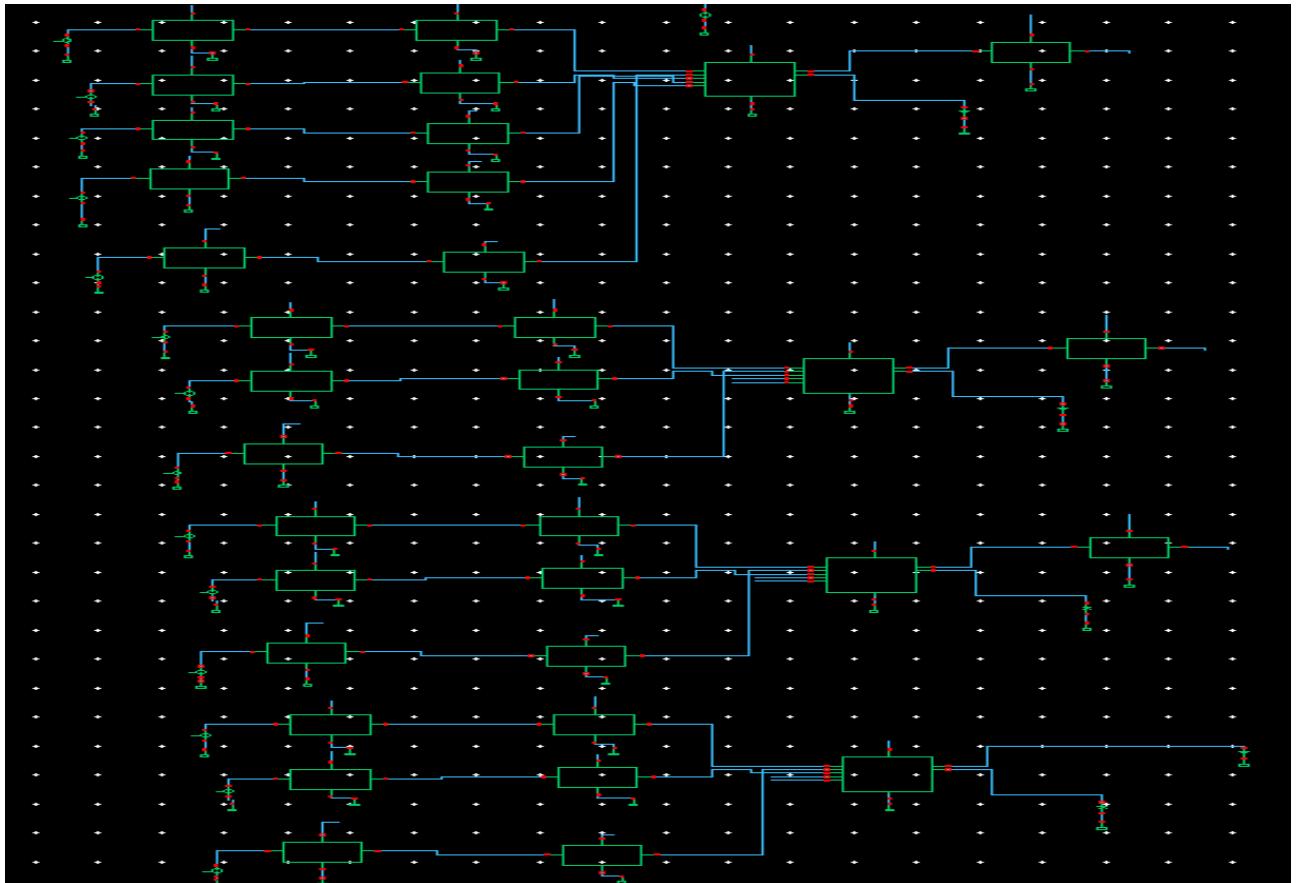
e) FA2 test bench



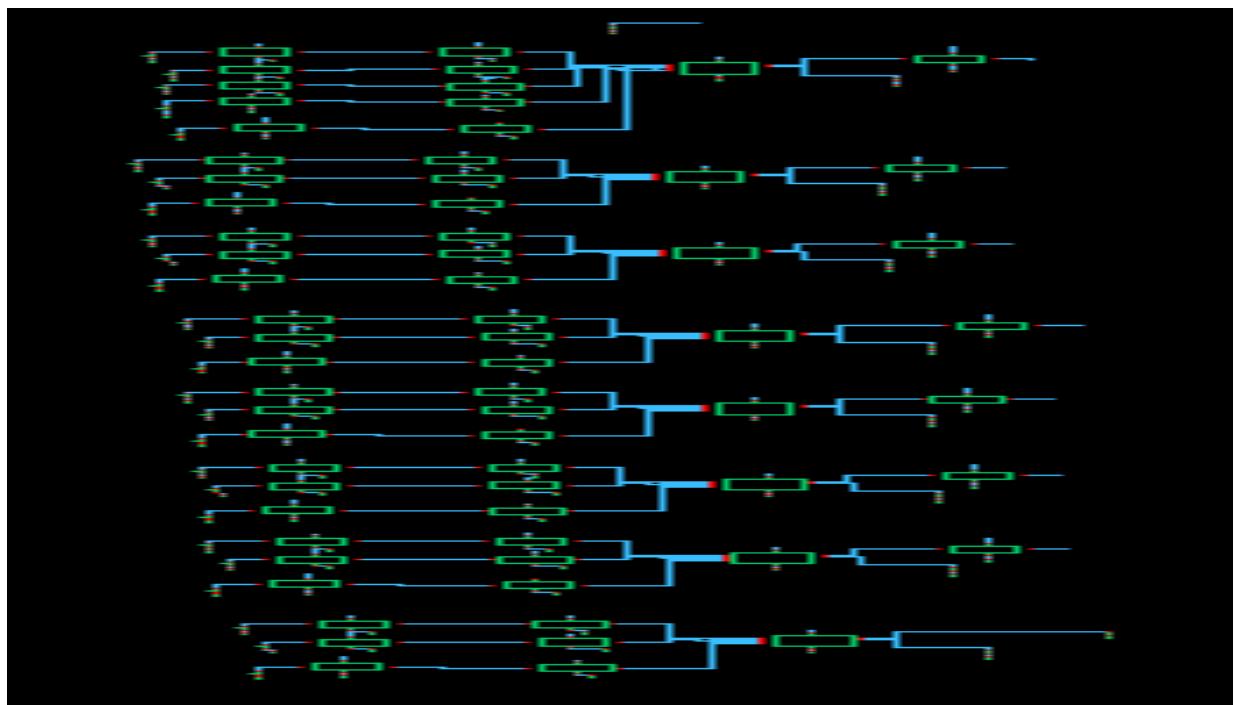
f) 2-bit FA2



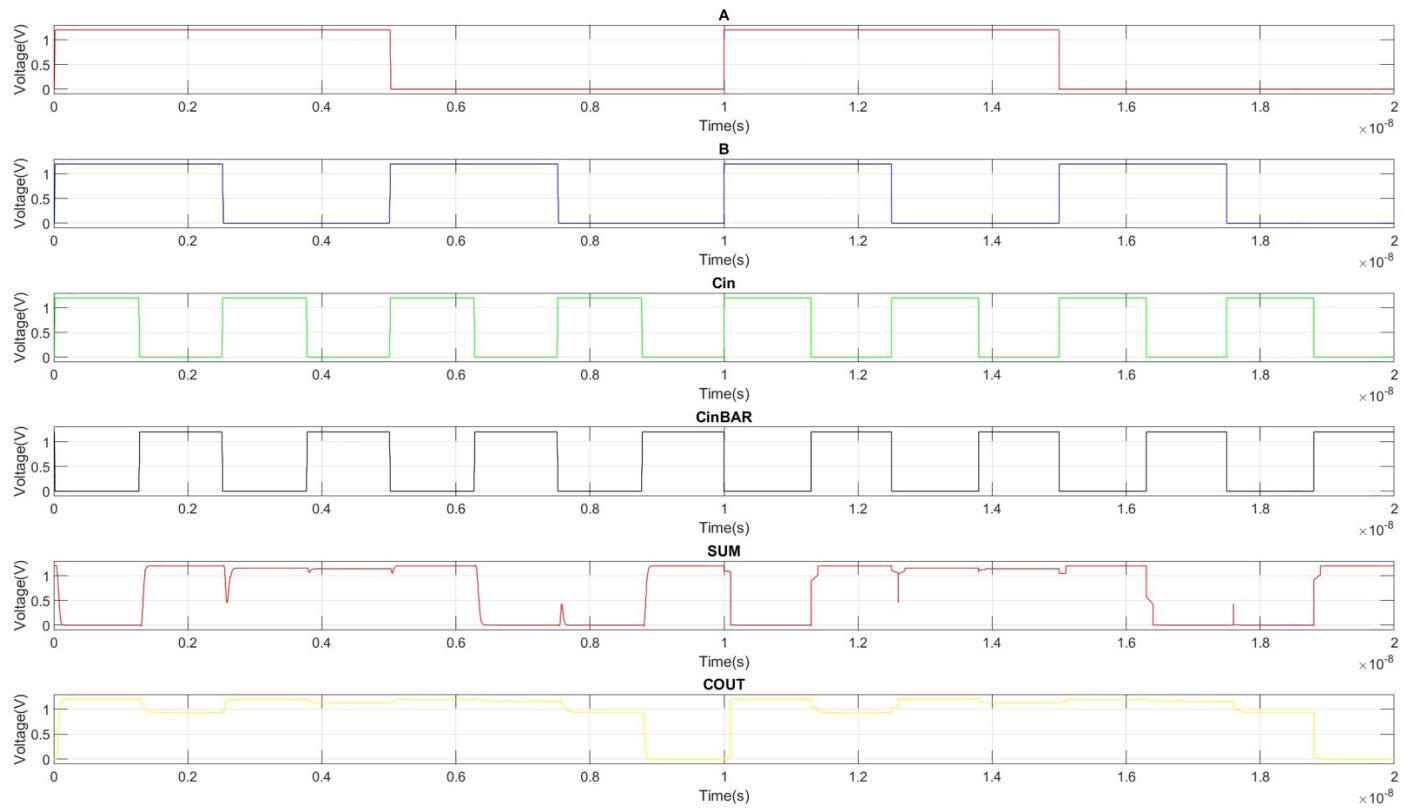
g) 4-bit FA2



h) 8-bit FA2

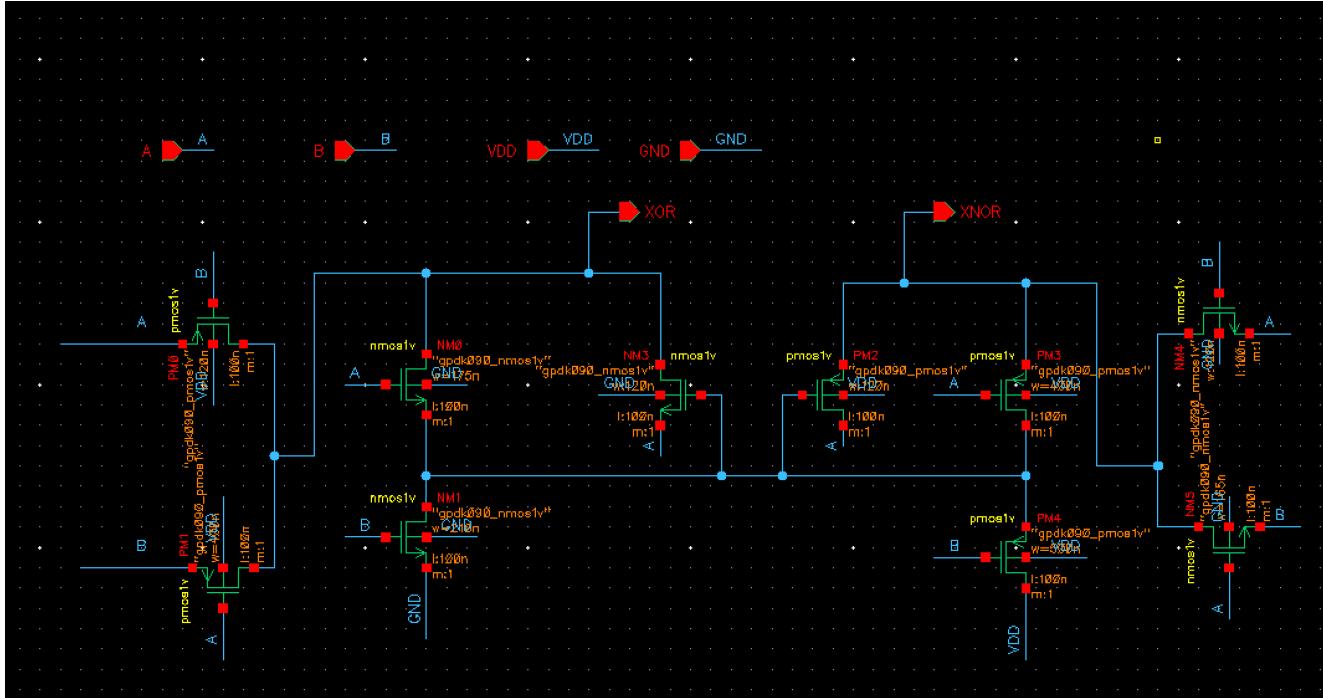


i) FA2 waveforms

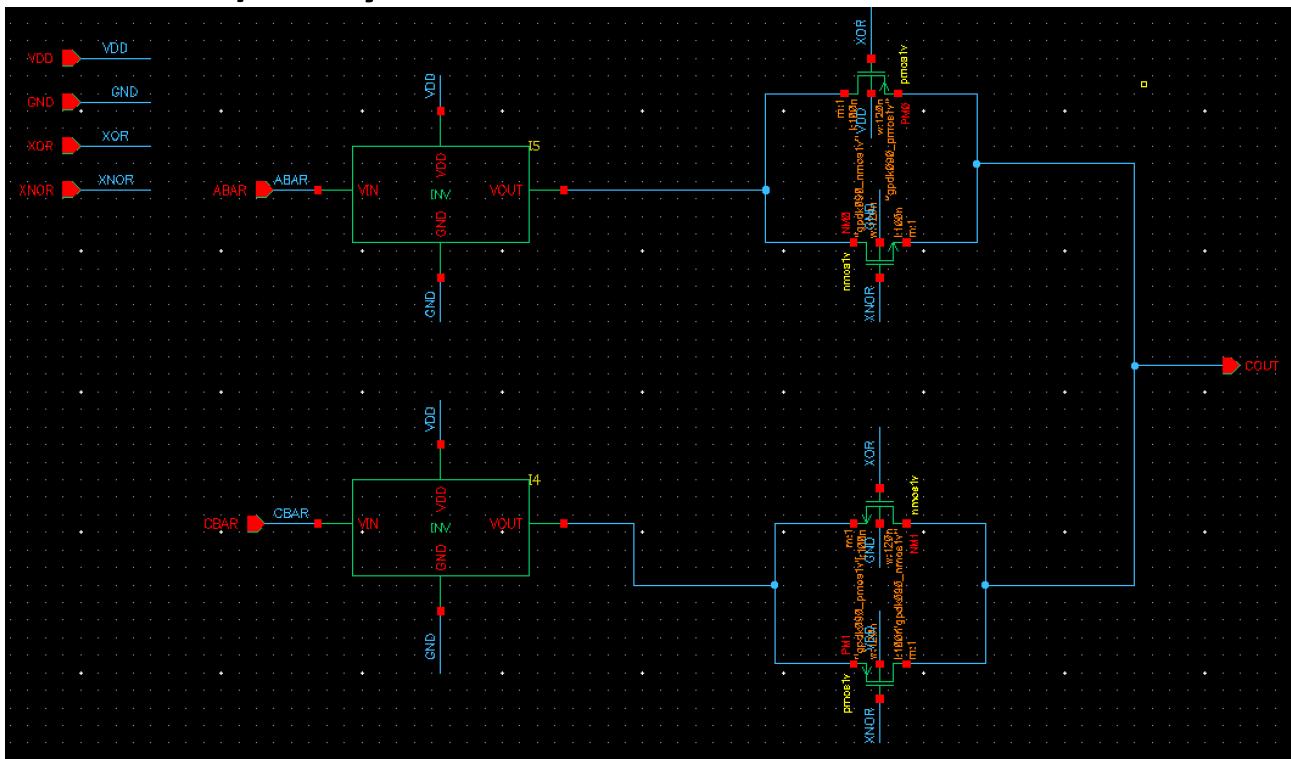


3. Full Adder 3 (Design-3)

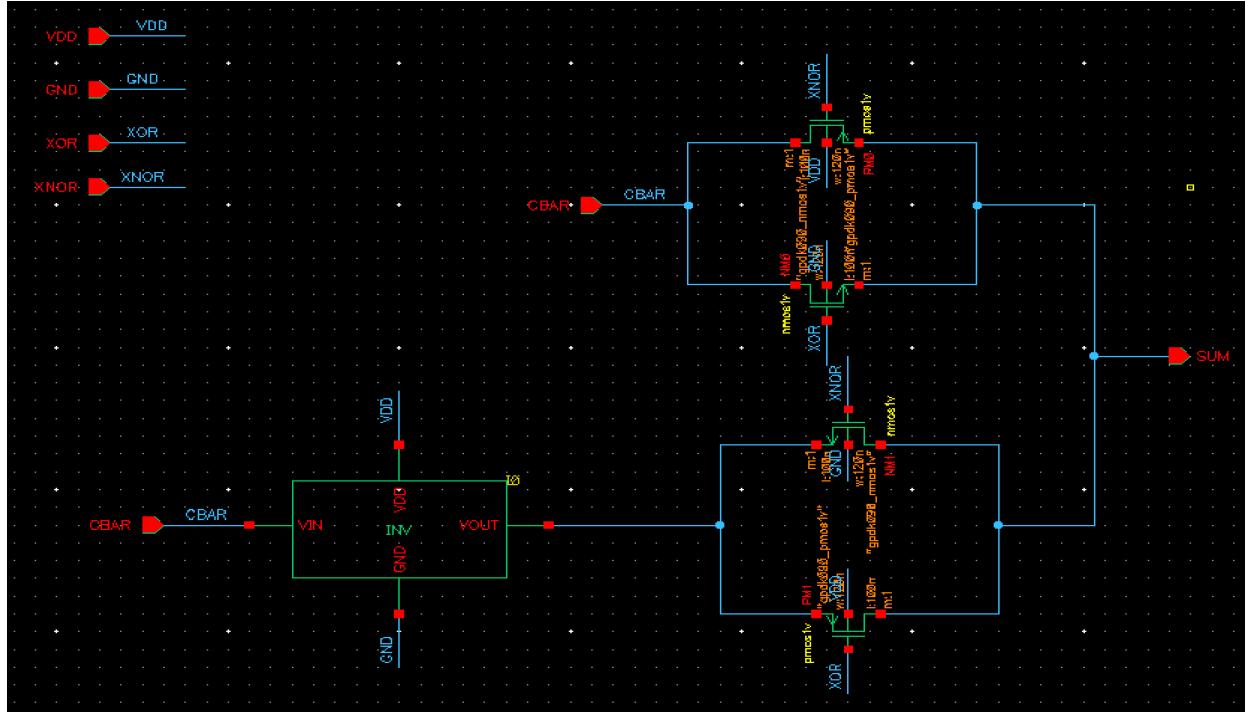
a) XOR-XNOR circuit



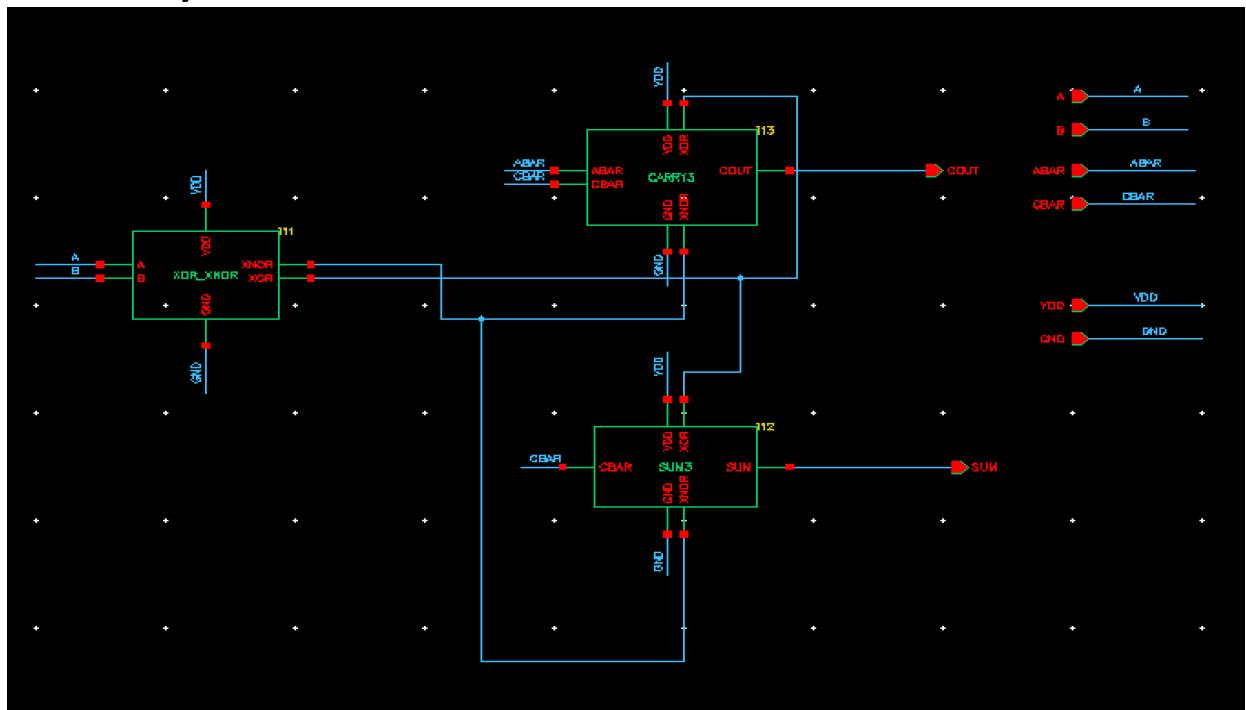
b) Carry module of FA3



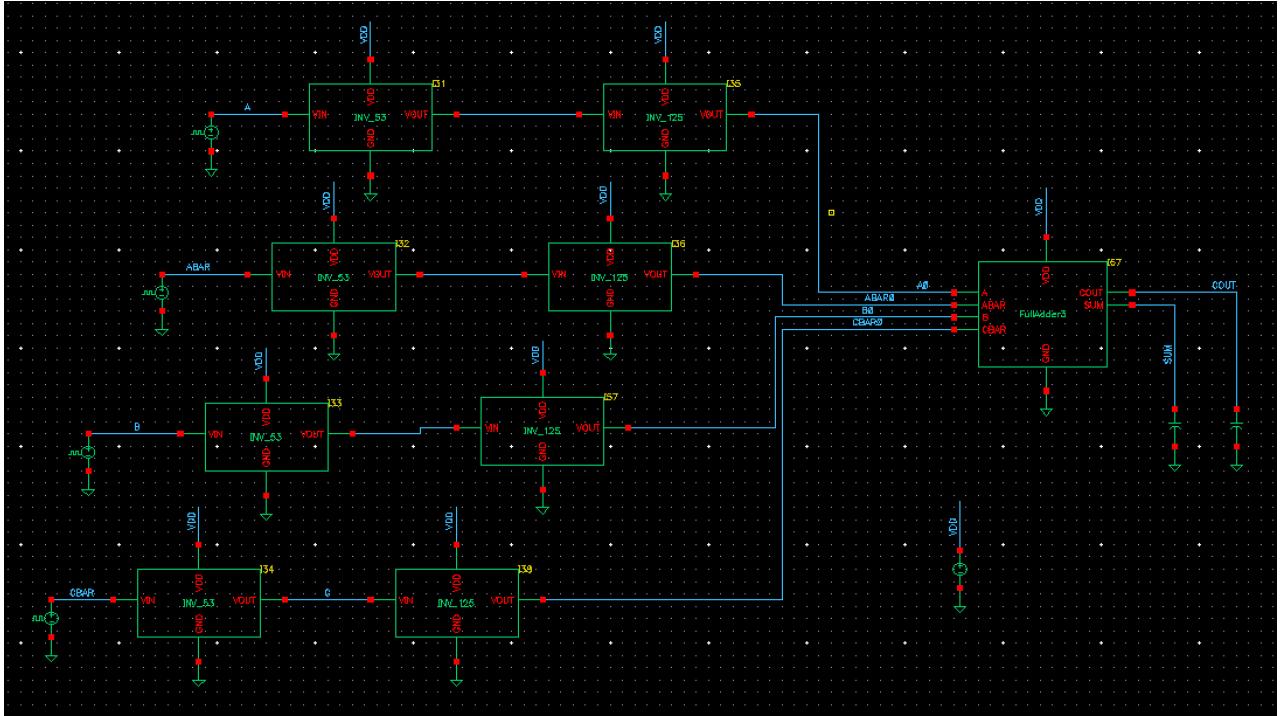
c) Sum module of FA3



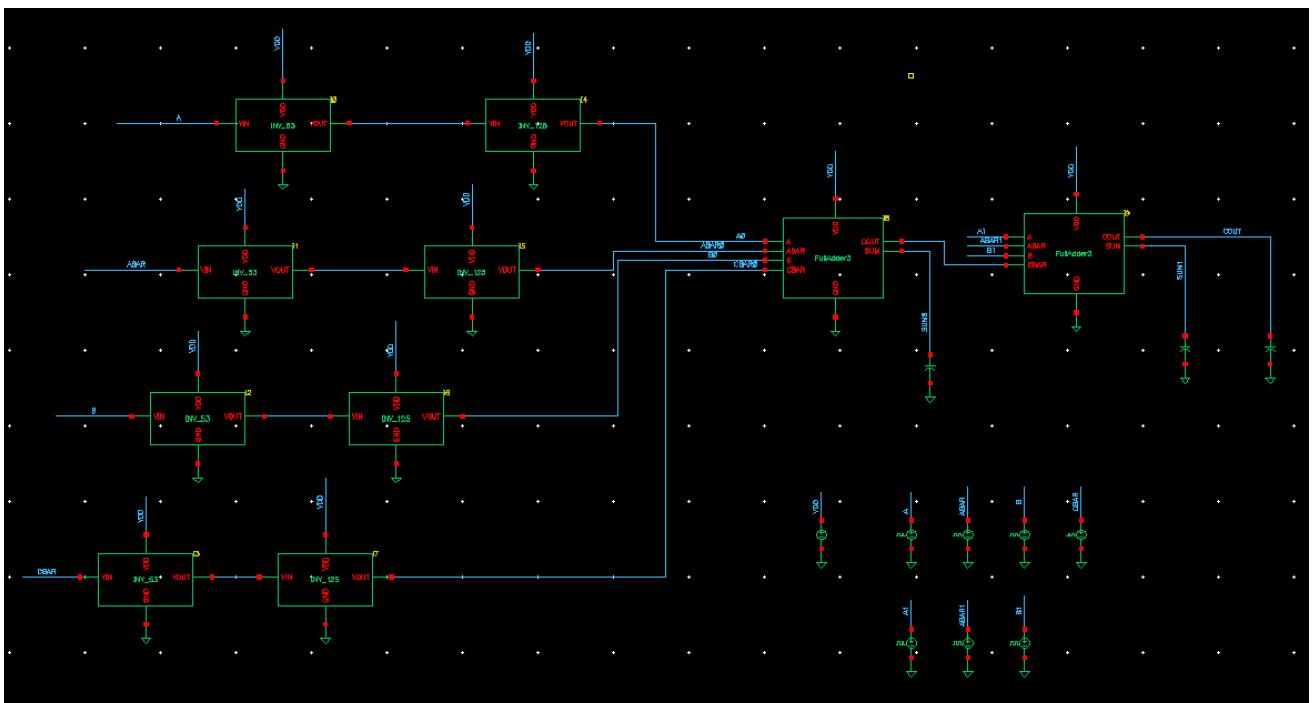
d) FA3 circuit



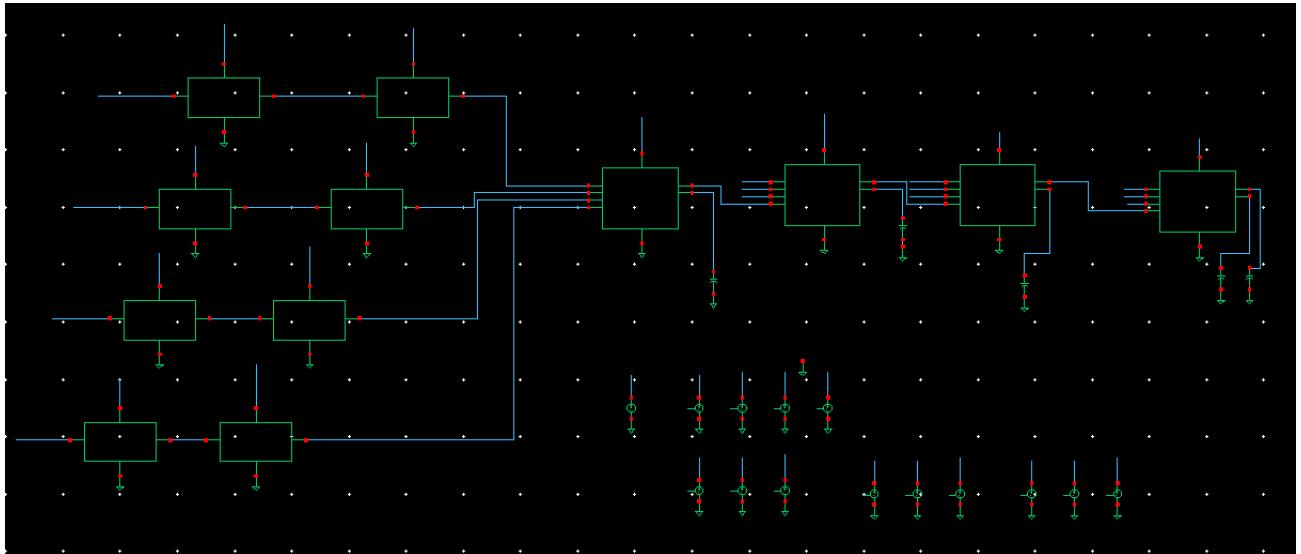
e) FA3 test bench



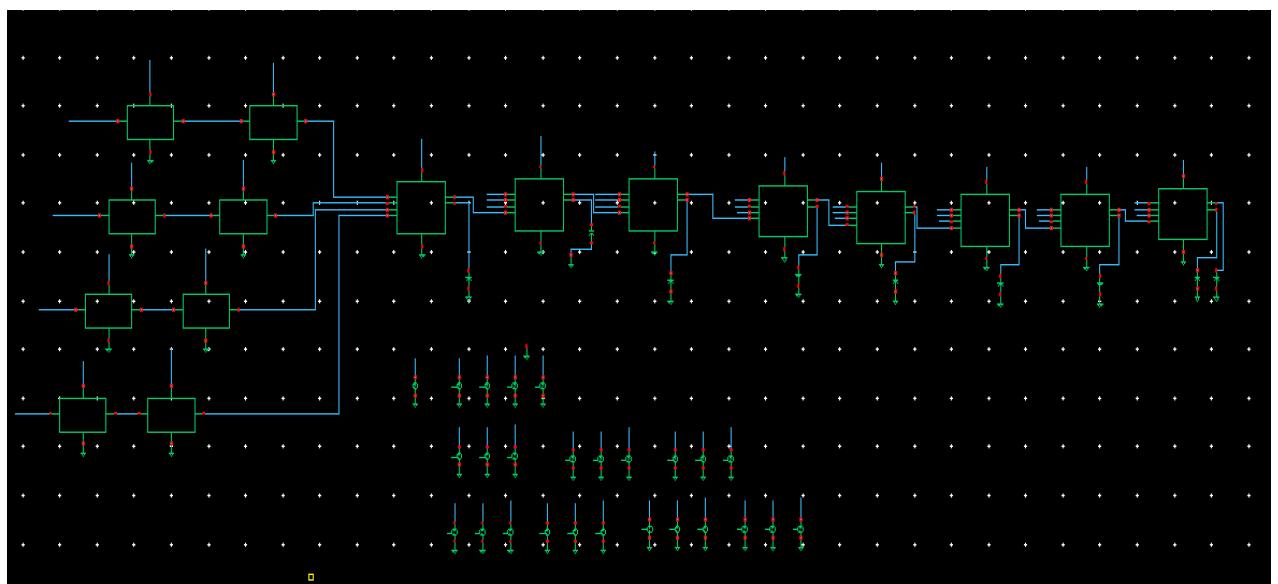
f) 2-bit FA3



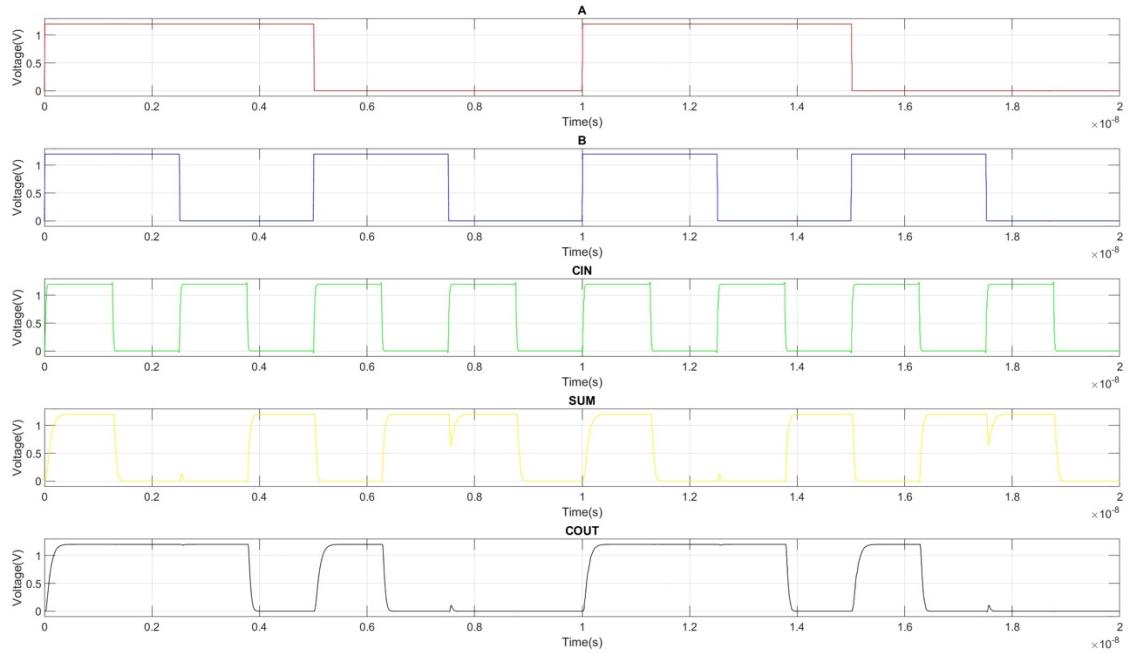
g) 4-bit FA3



h) 8-bit FA3

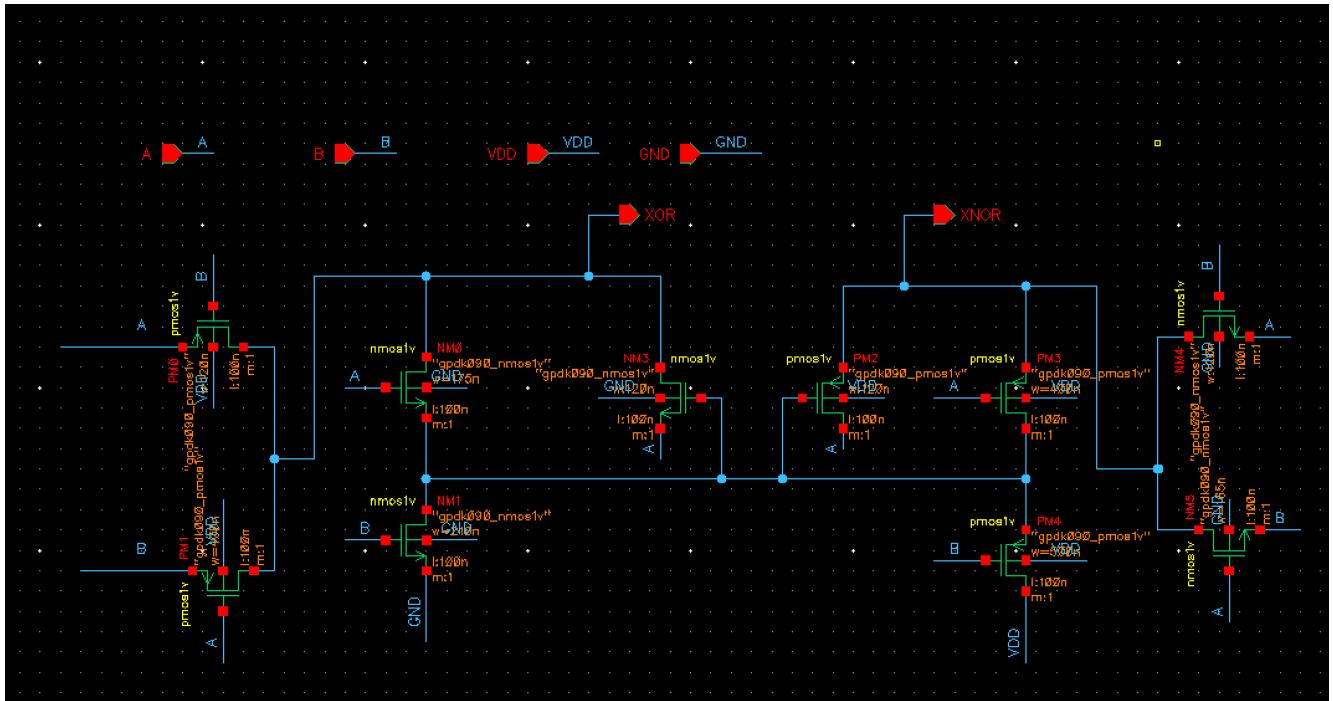


i) FA3 waveforms

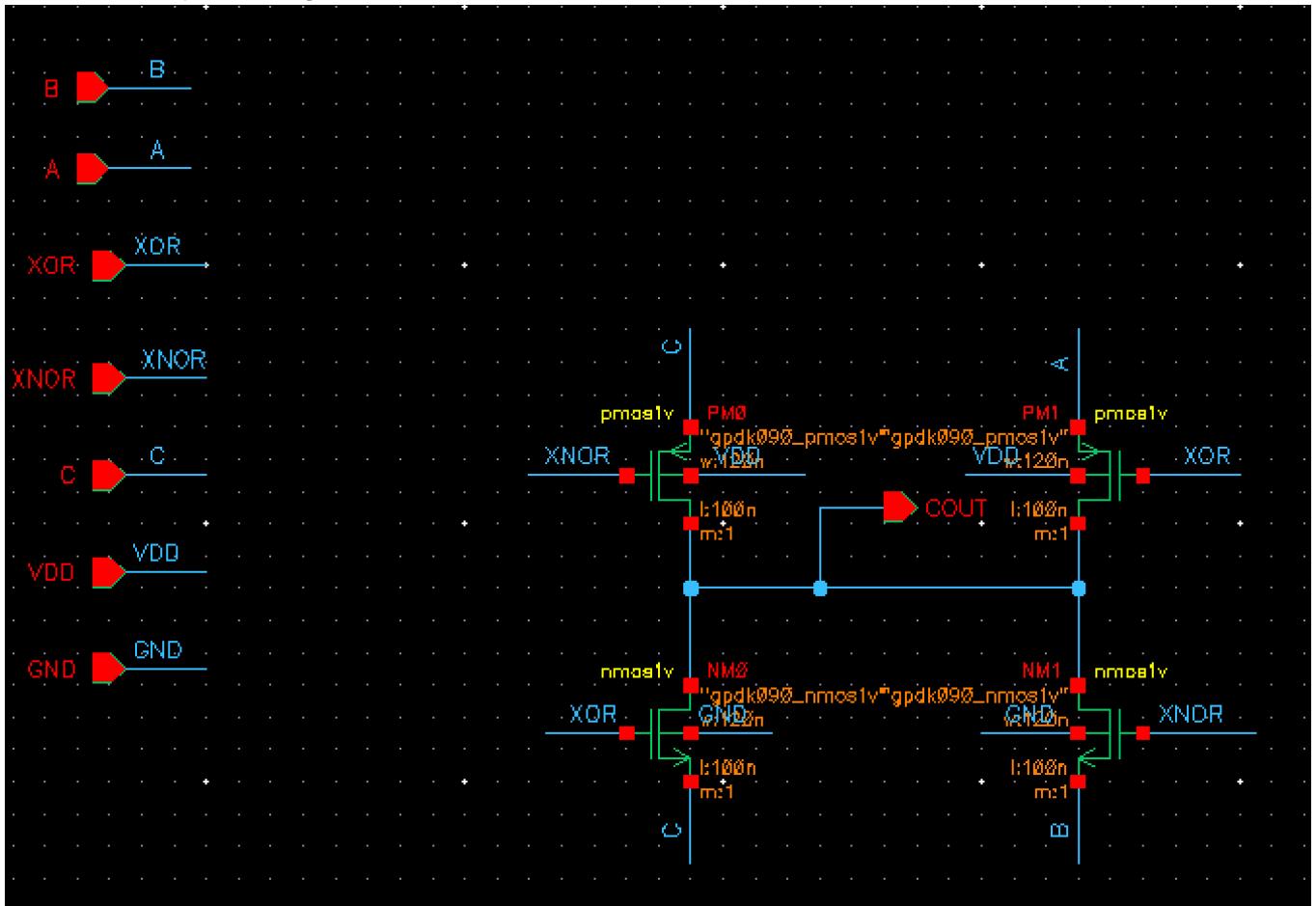


4. Full Adder 4 (Design-4)

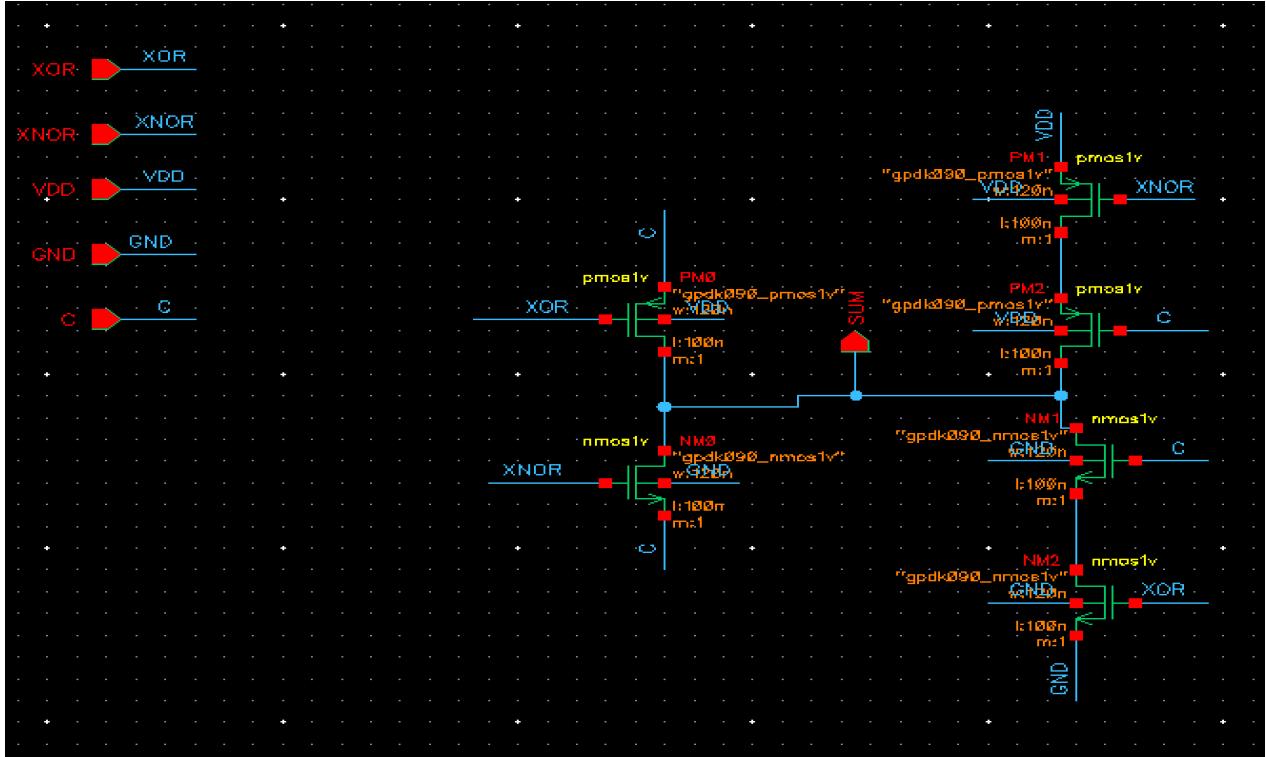
a) XOR-XNOR circuit



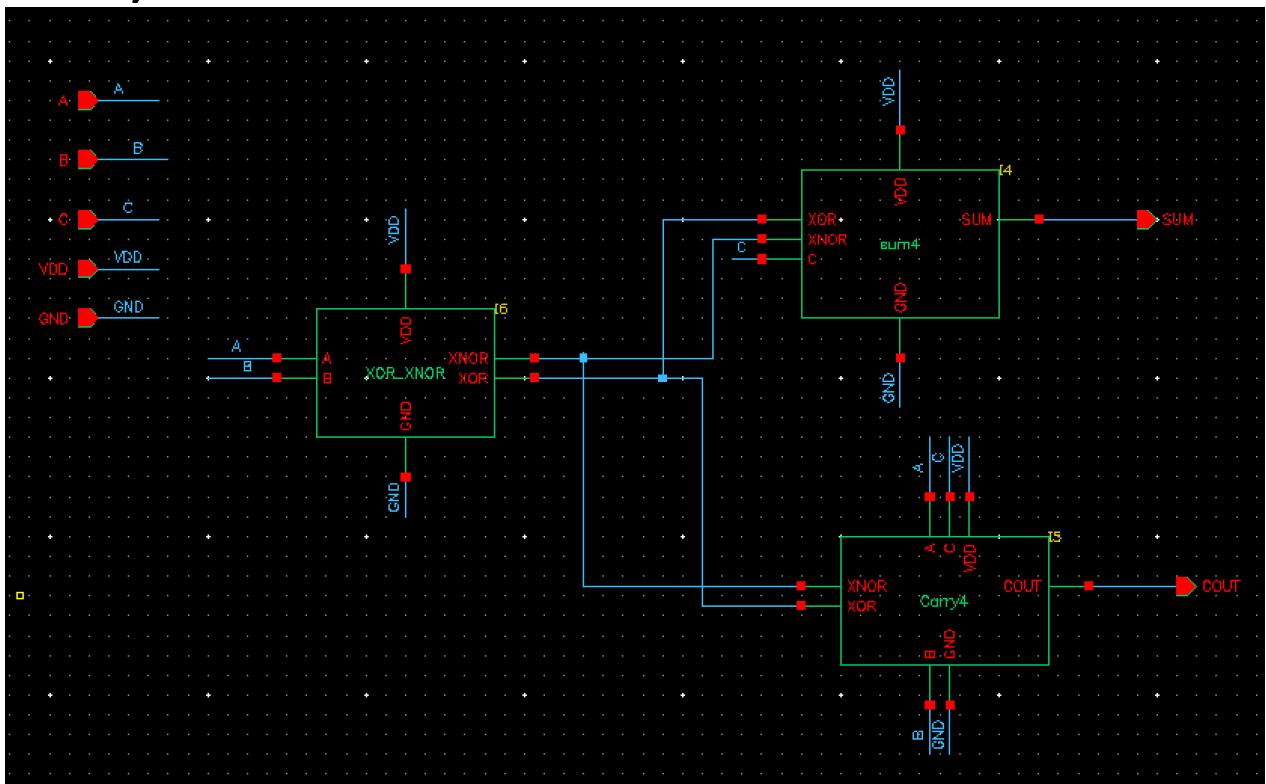
b) Carry module of FA4



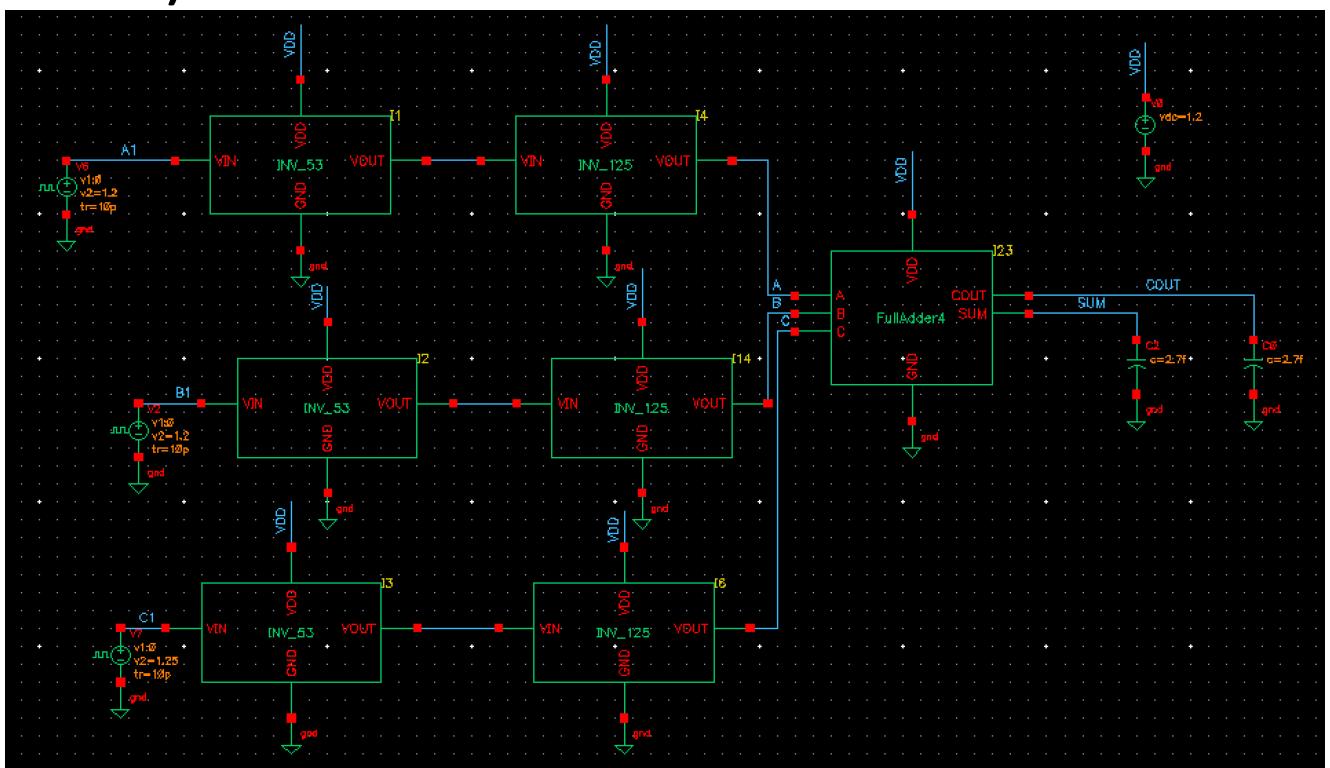
c) Sum module of FA4



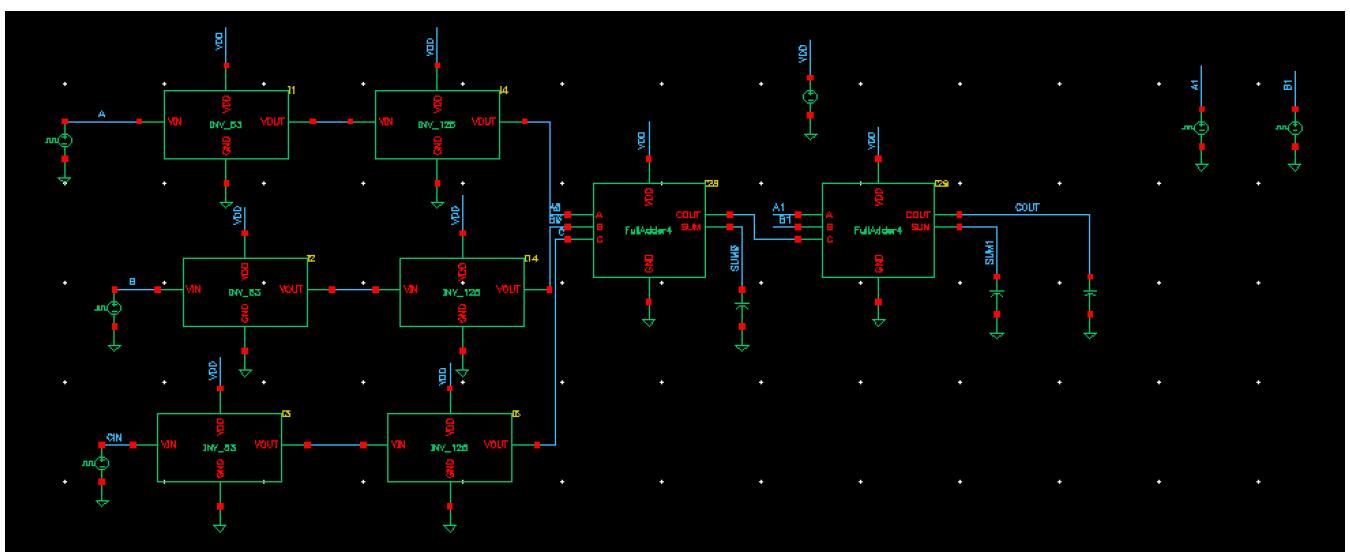
d) FA4 circuit



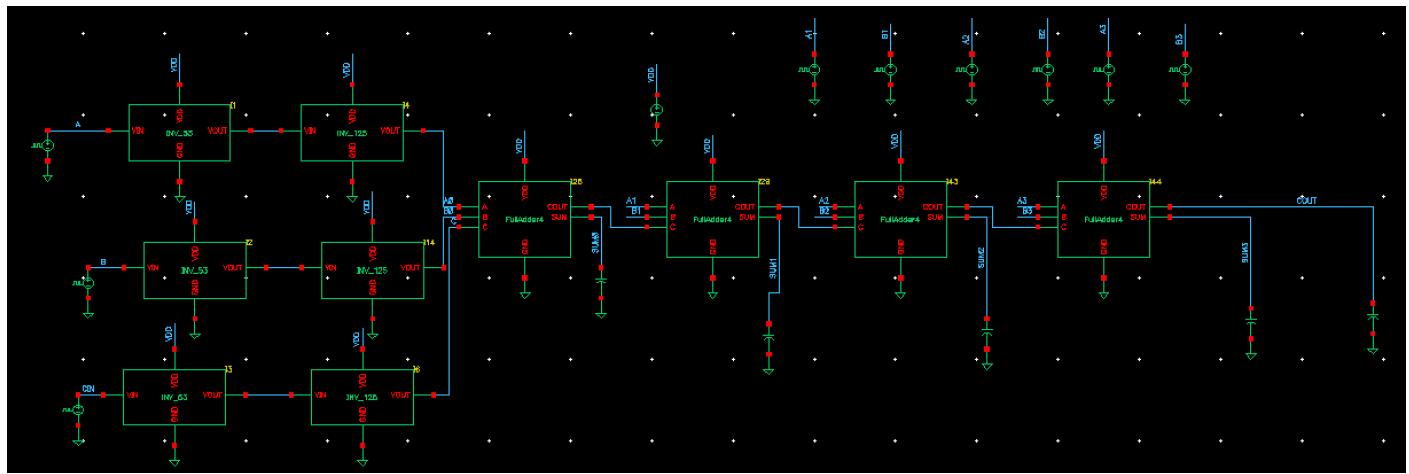
e) FA4 test bench



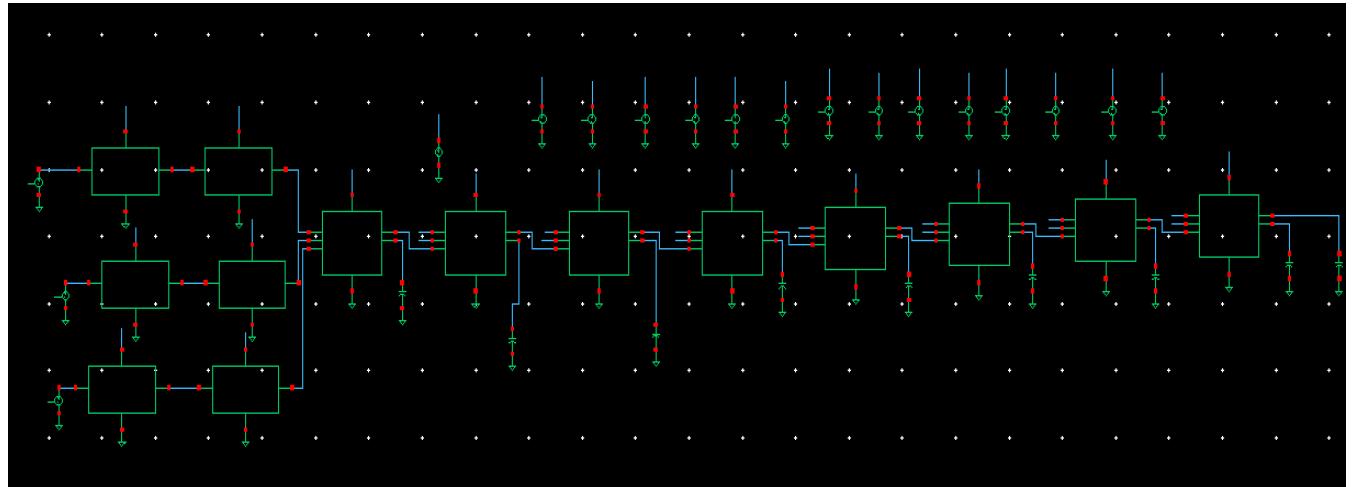
f) 2-bit FA4



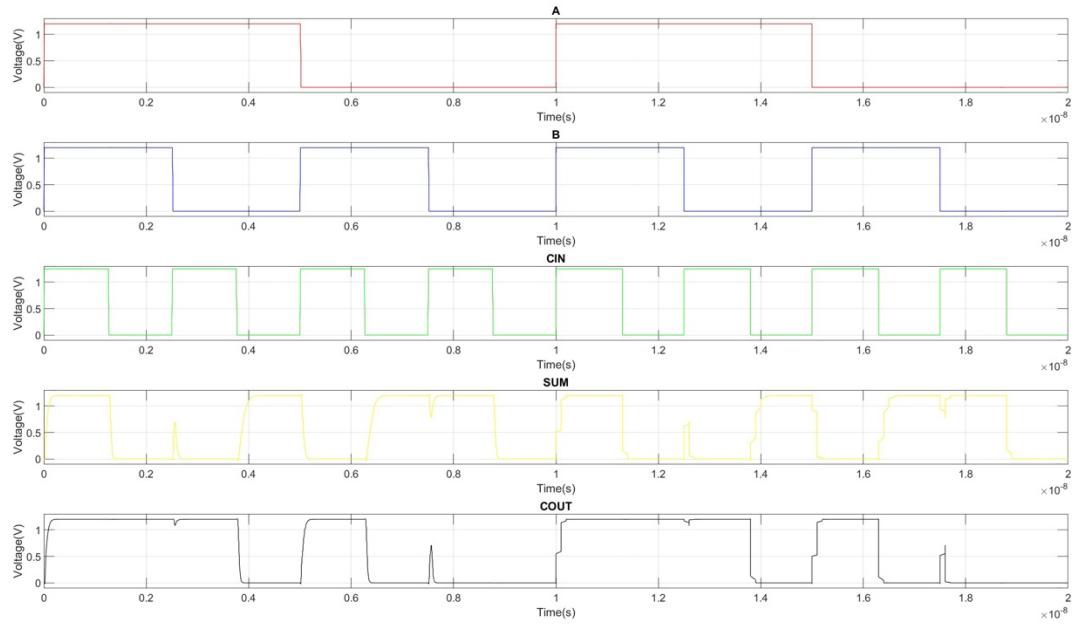
g) 4-bit FA4



h) 8-bit FA4

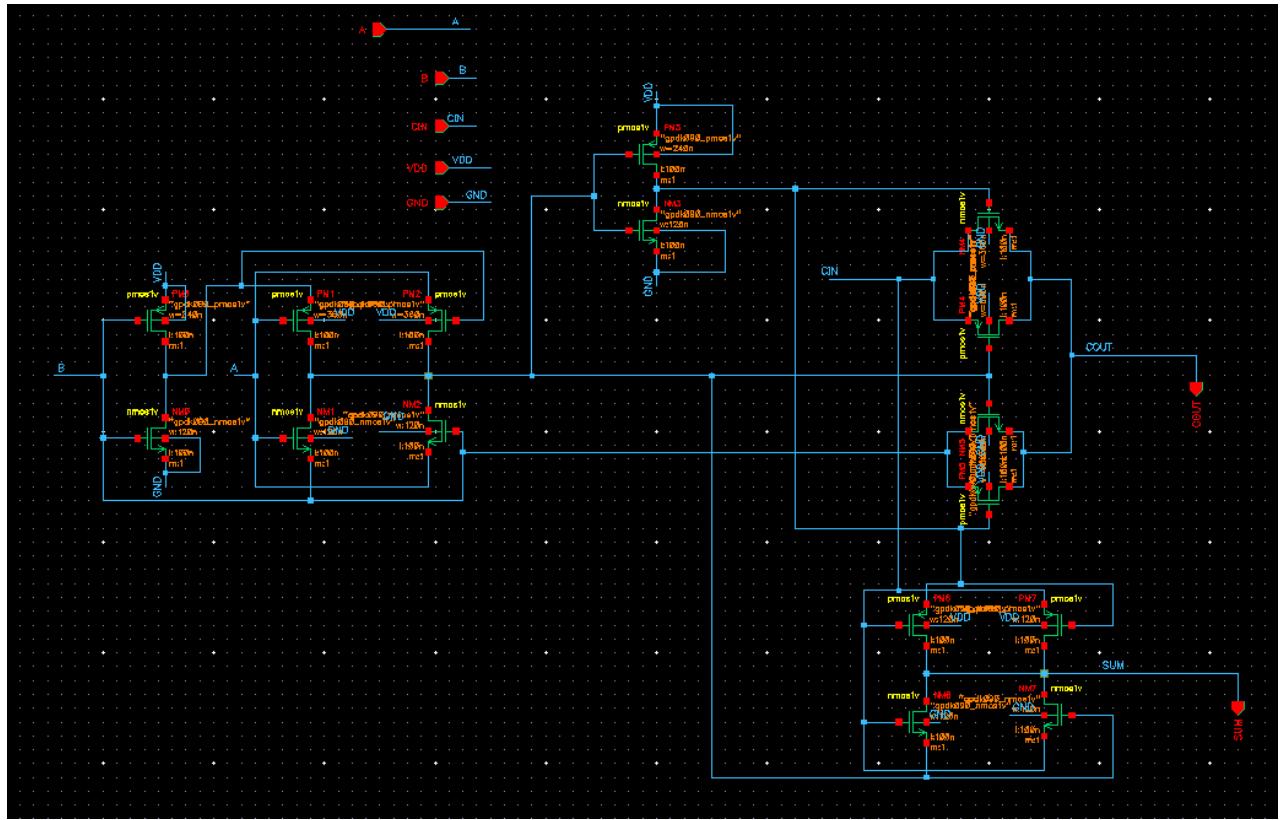


i) FA4 waveforms

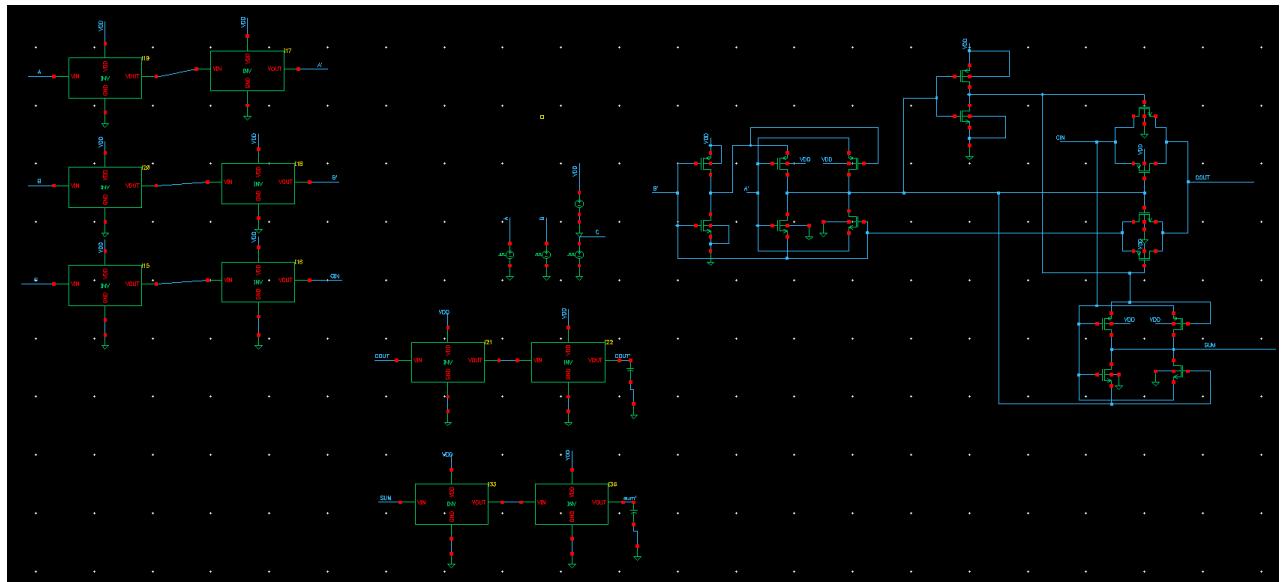


5. Bhattacharyya (Design-5)

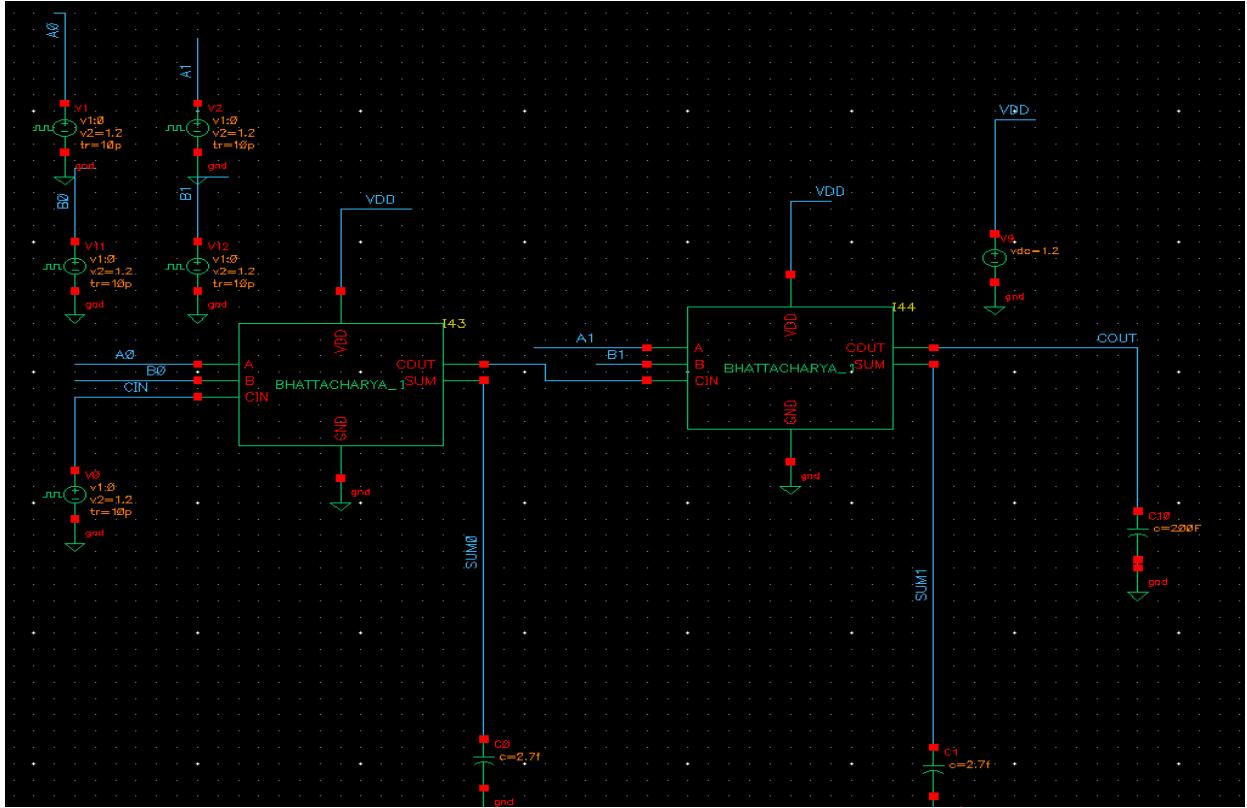
a) Bhattacharyya FA



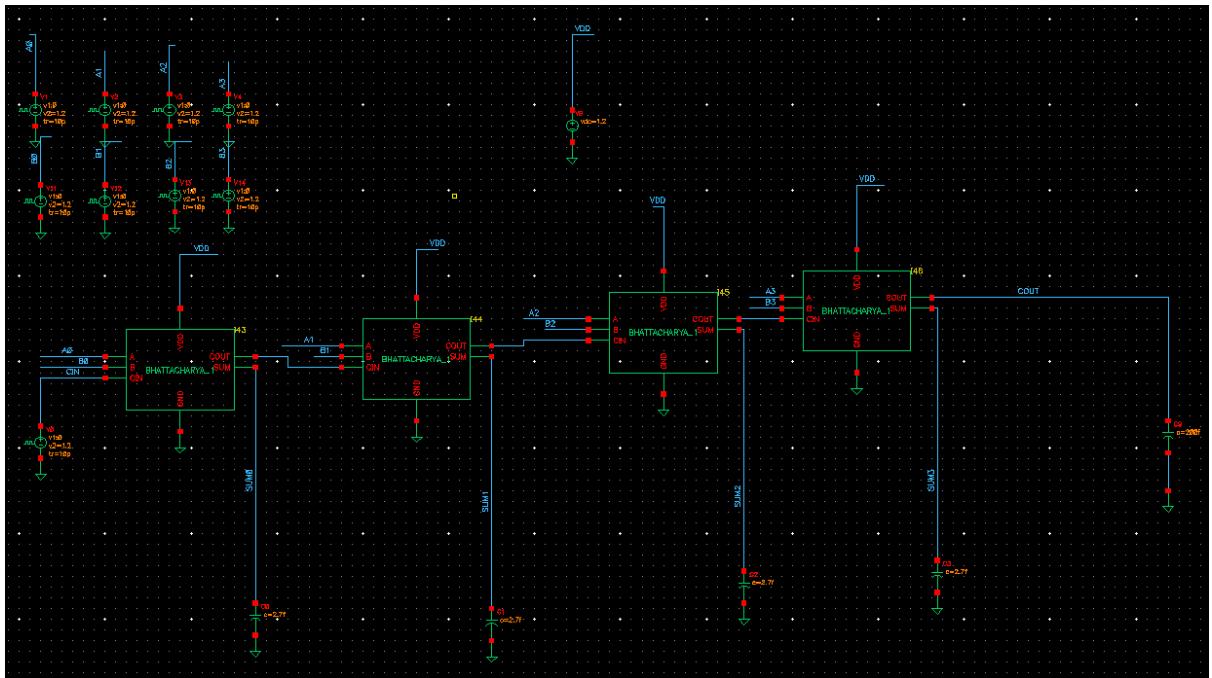
b) Bhattacharyya FA test bench



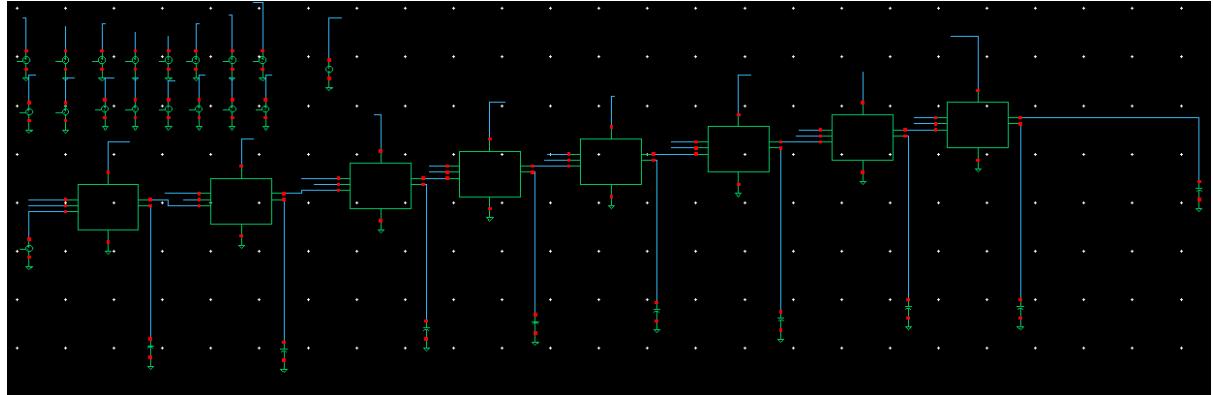
c) 2-bit Bhattacharyya FA



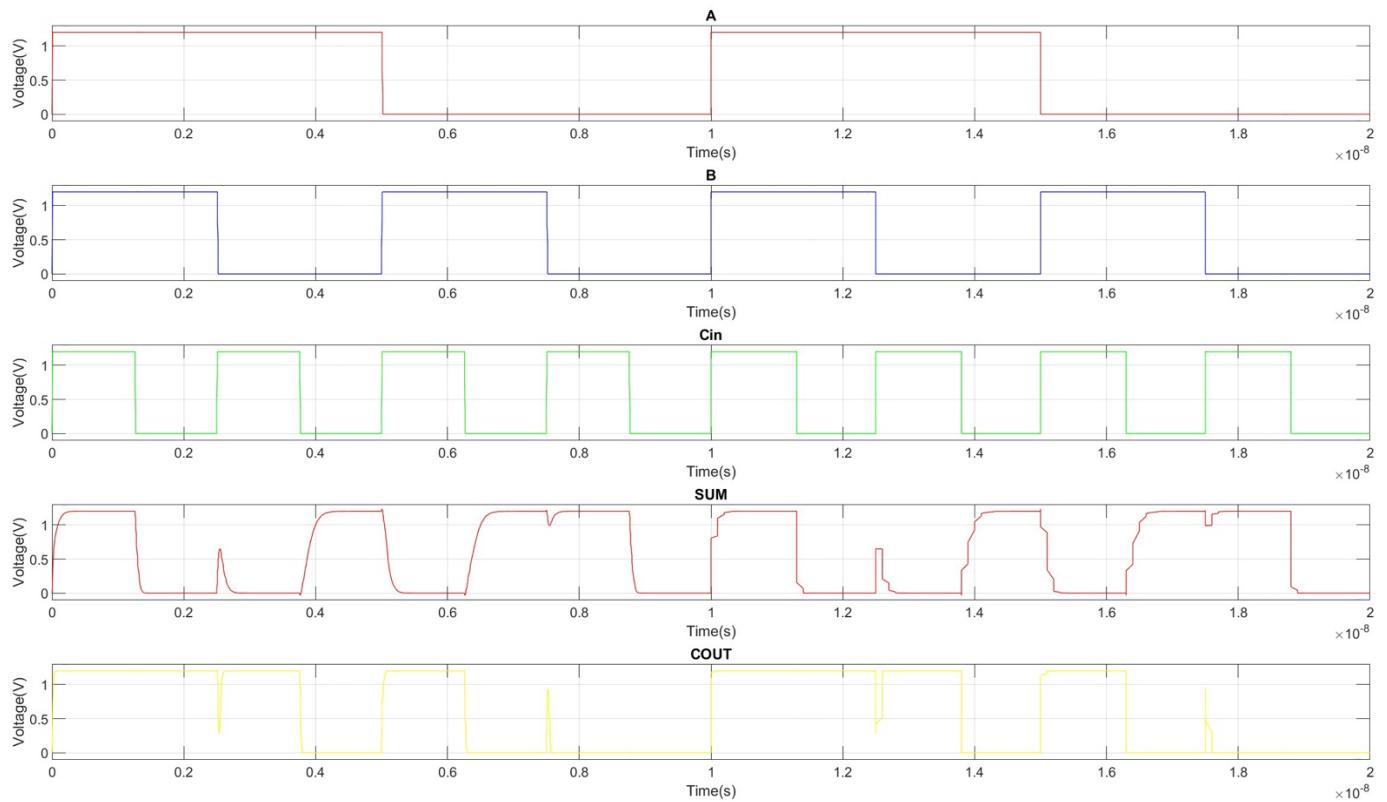
d) 4-bit Bhattacharyya FA



e) 8-bit Bhattacharyya FA



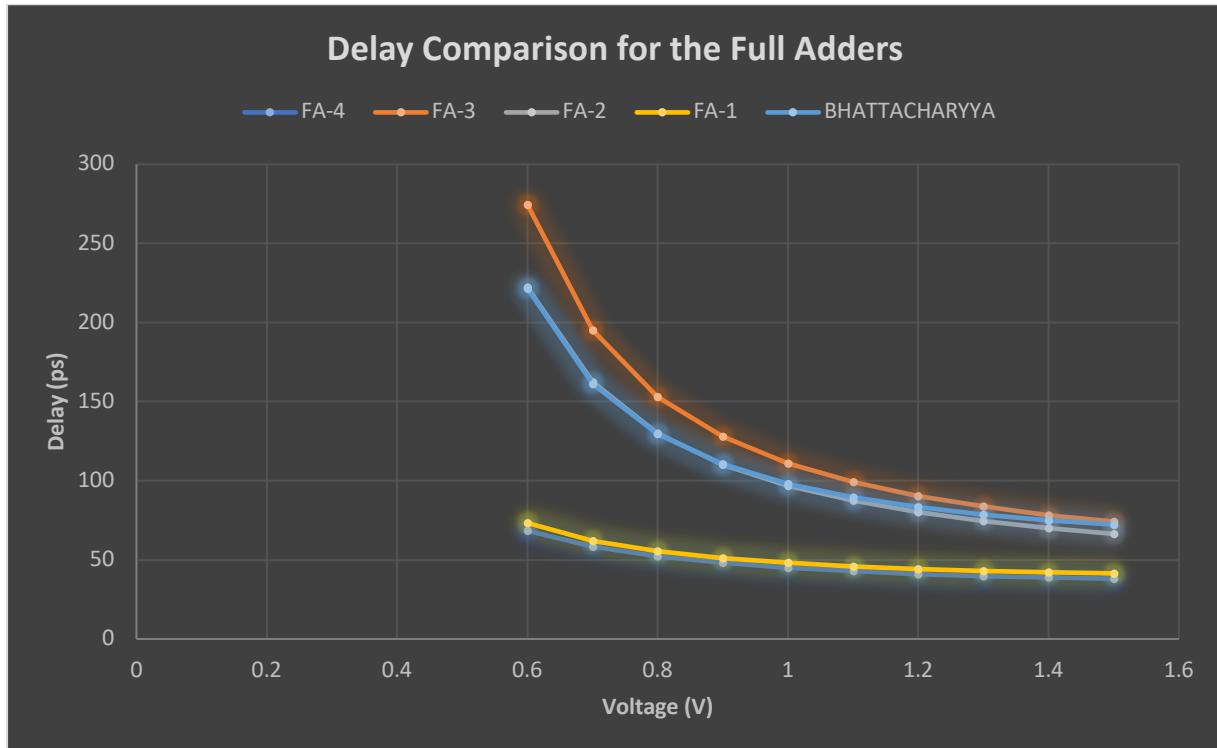
f) Bhattacharyya FA waveforms



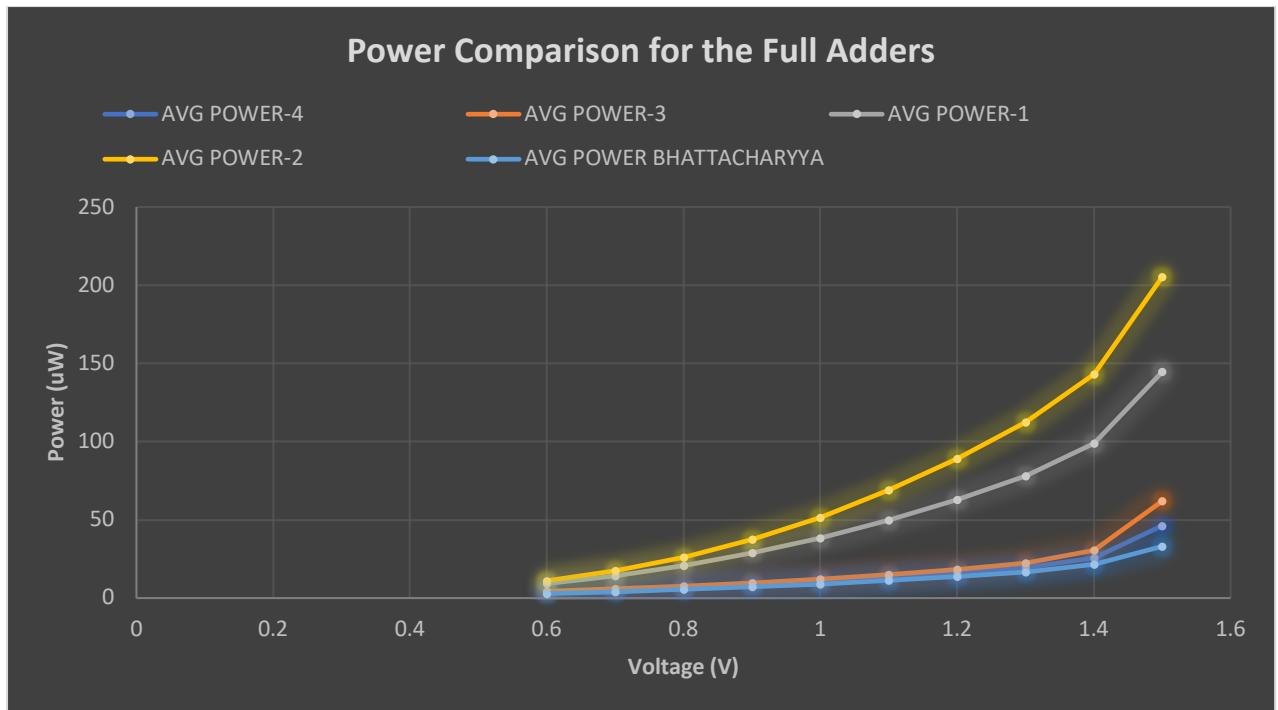
Simulation Results:

Voltage Variation Comparisons:

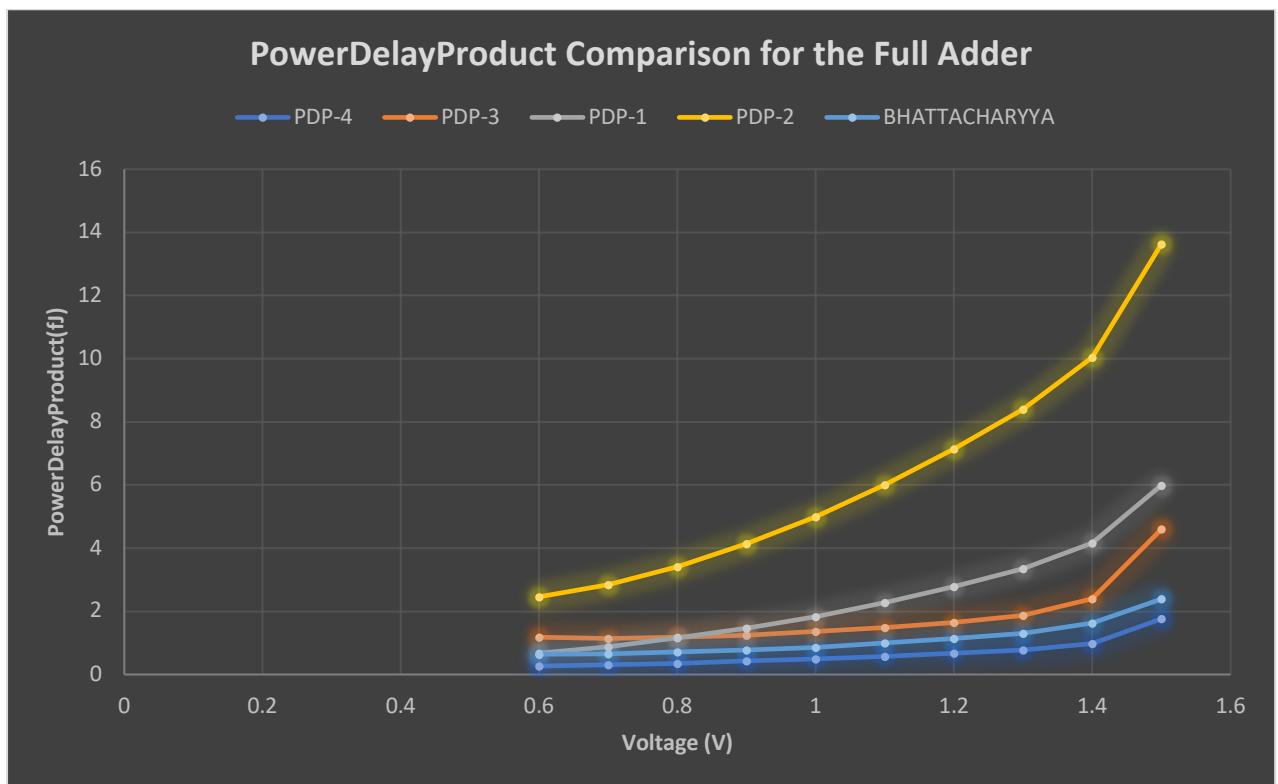
1. Delay comparison between the proposed FAs and Bhattacharyya's FA



2. Power comparison between the proposed FAs and Bhattacharyya's FA

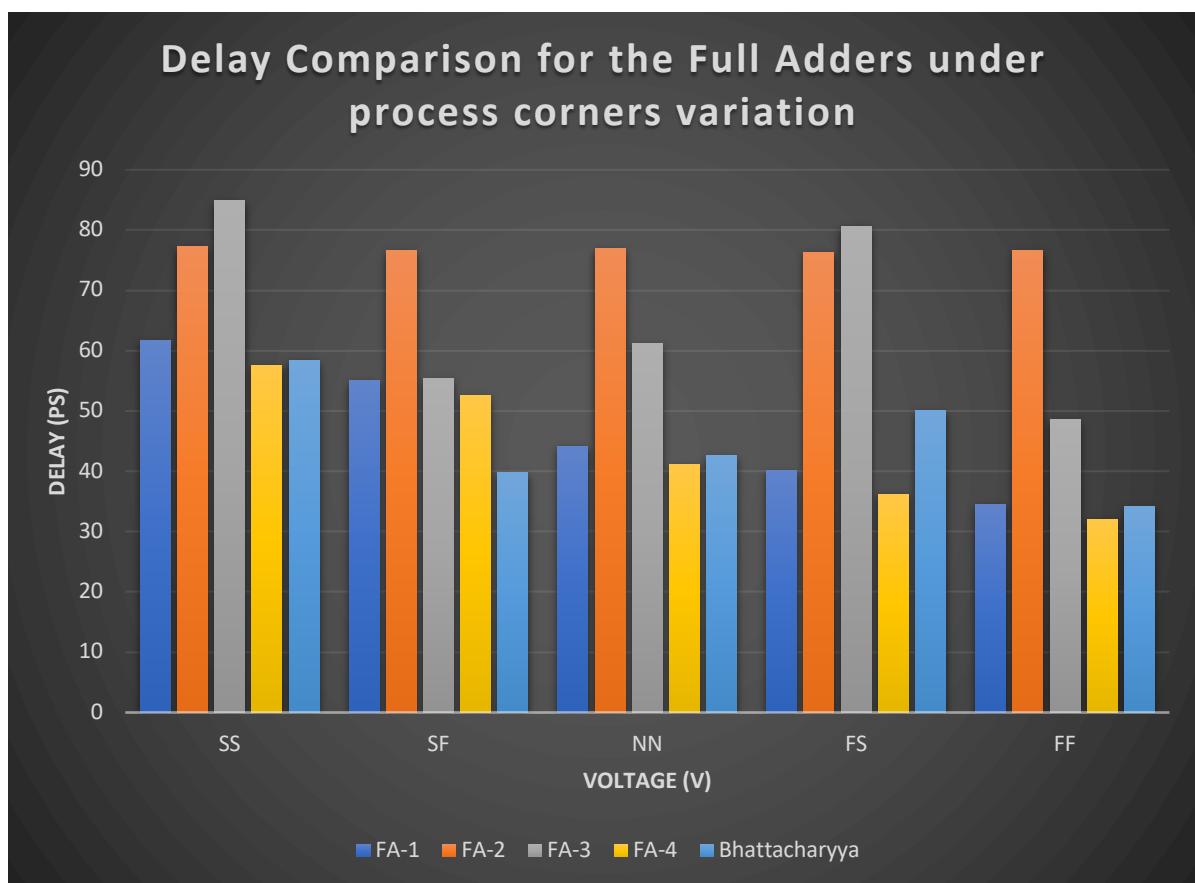


3. Power Delay Product comparison between the proposed FAs and Bhattacharyya's FA

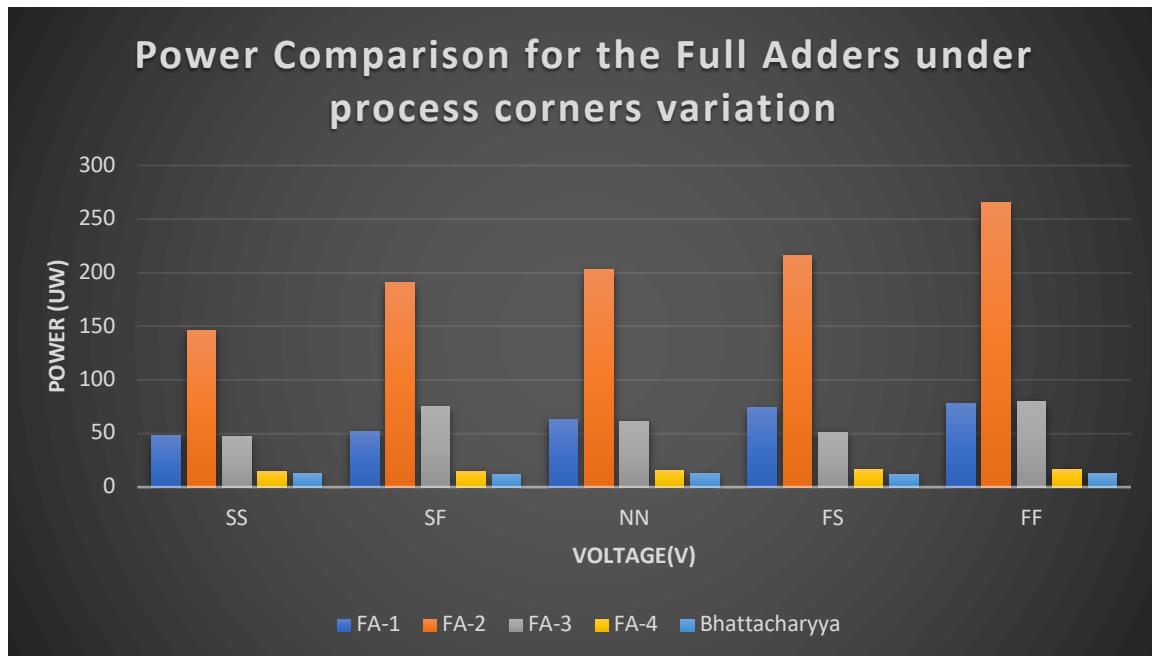


Process Corners variation Comparisons:

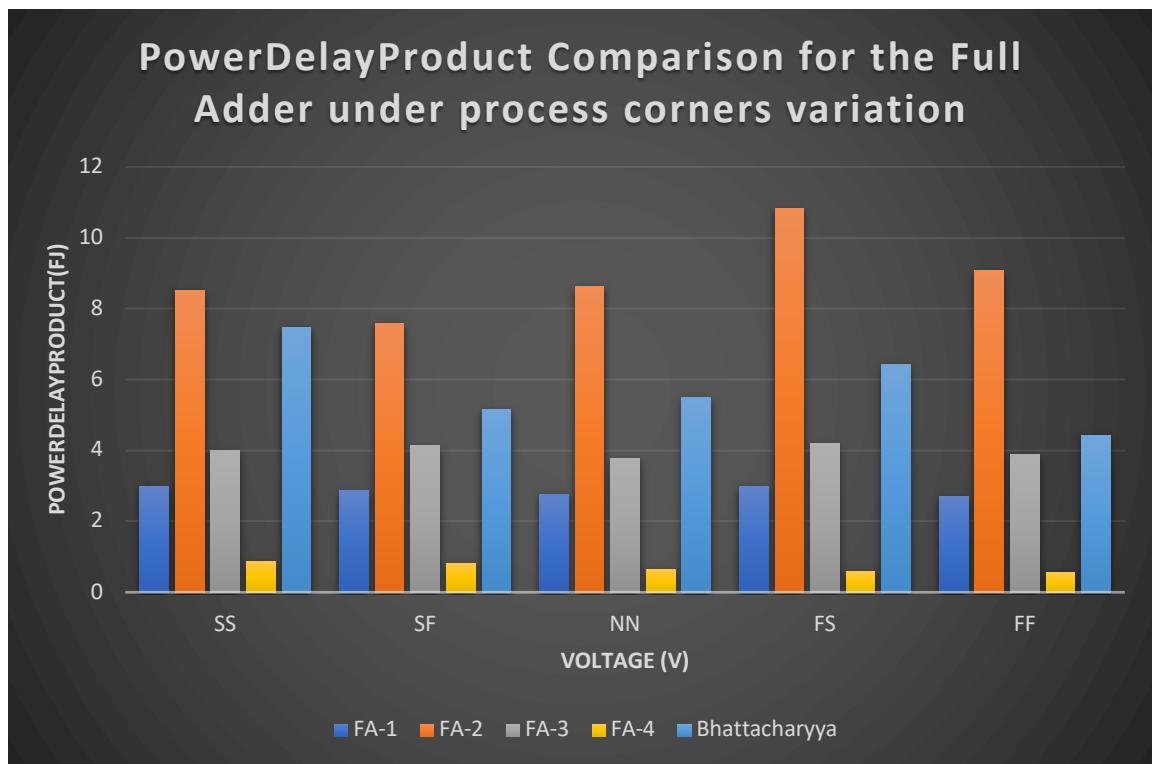
4. Delay comparison of different Full Adders for under process corners variations



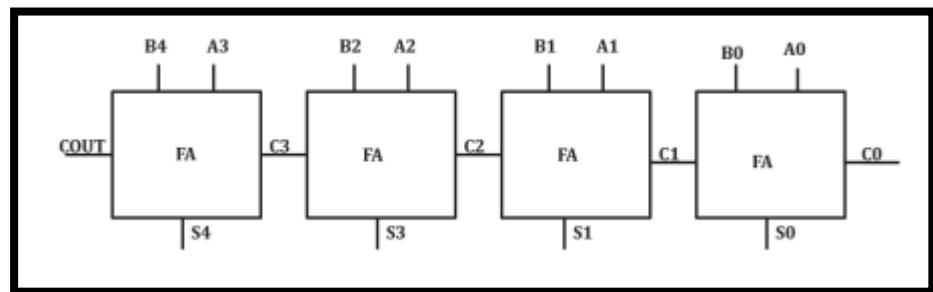
5. Power comparison of different Full Adders for under process corners variations



6. Power Delay Product comparison of different Full Adders for under process corners variations

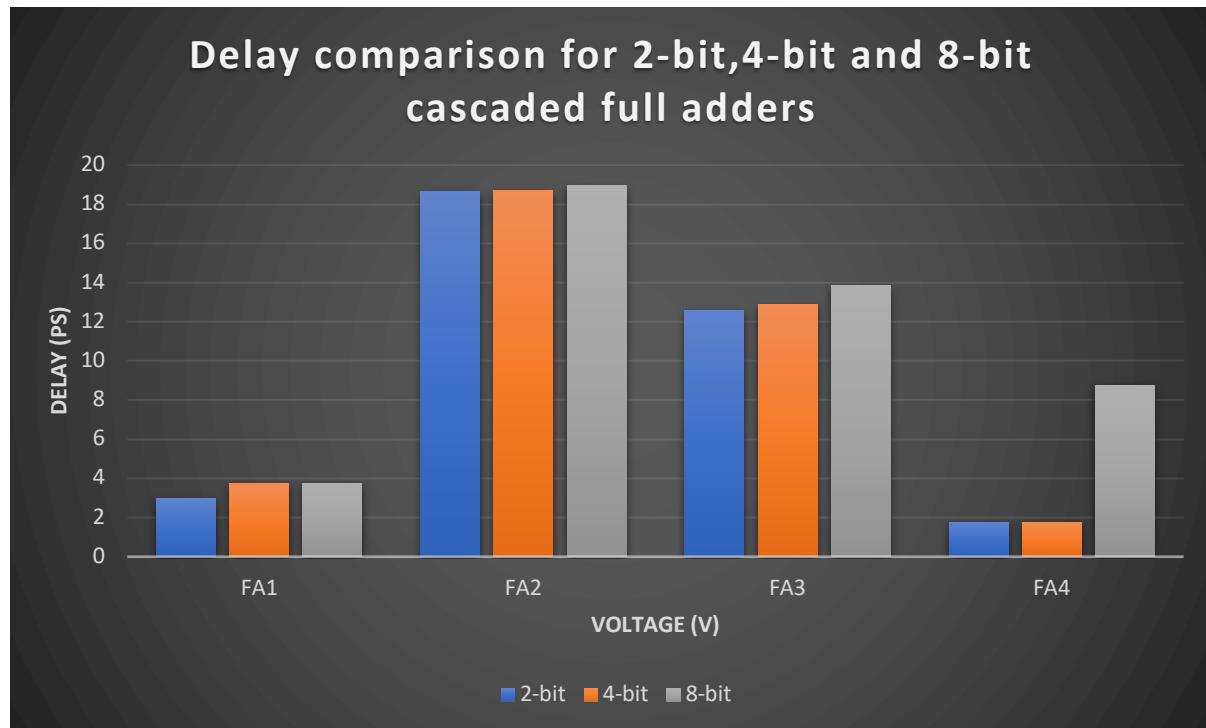


N-Bit Cascaded Full Adder (CFA)

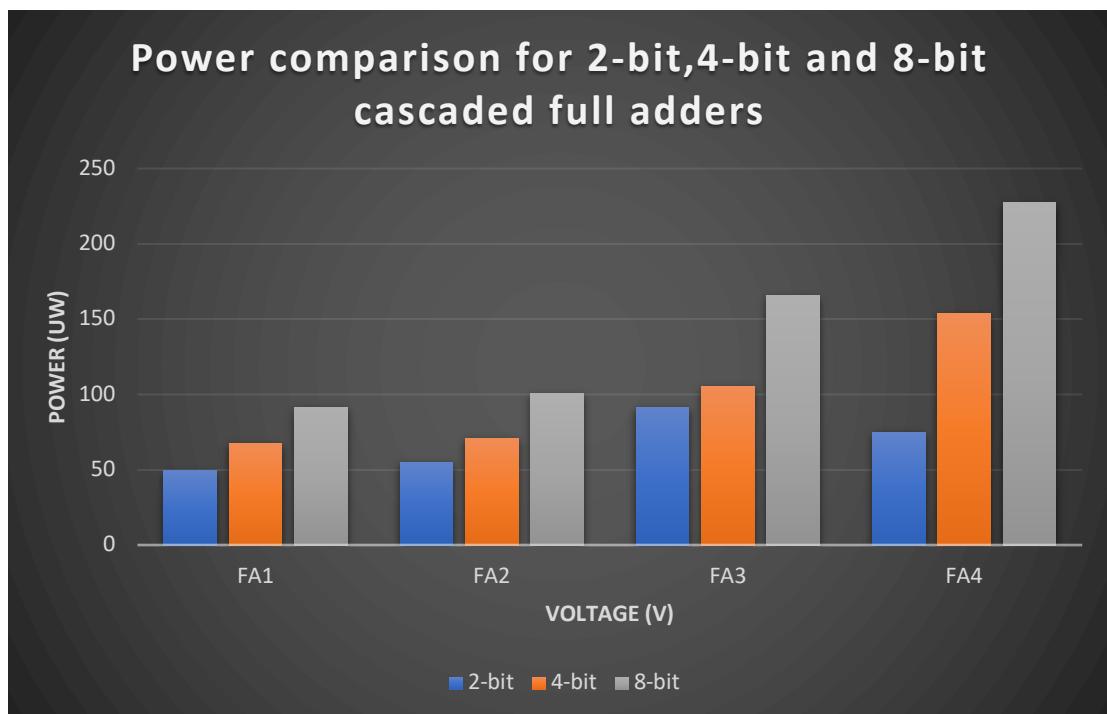


Block diagram of n-bit CFA

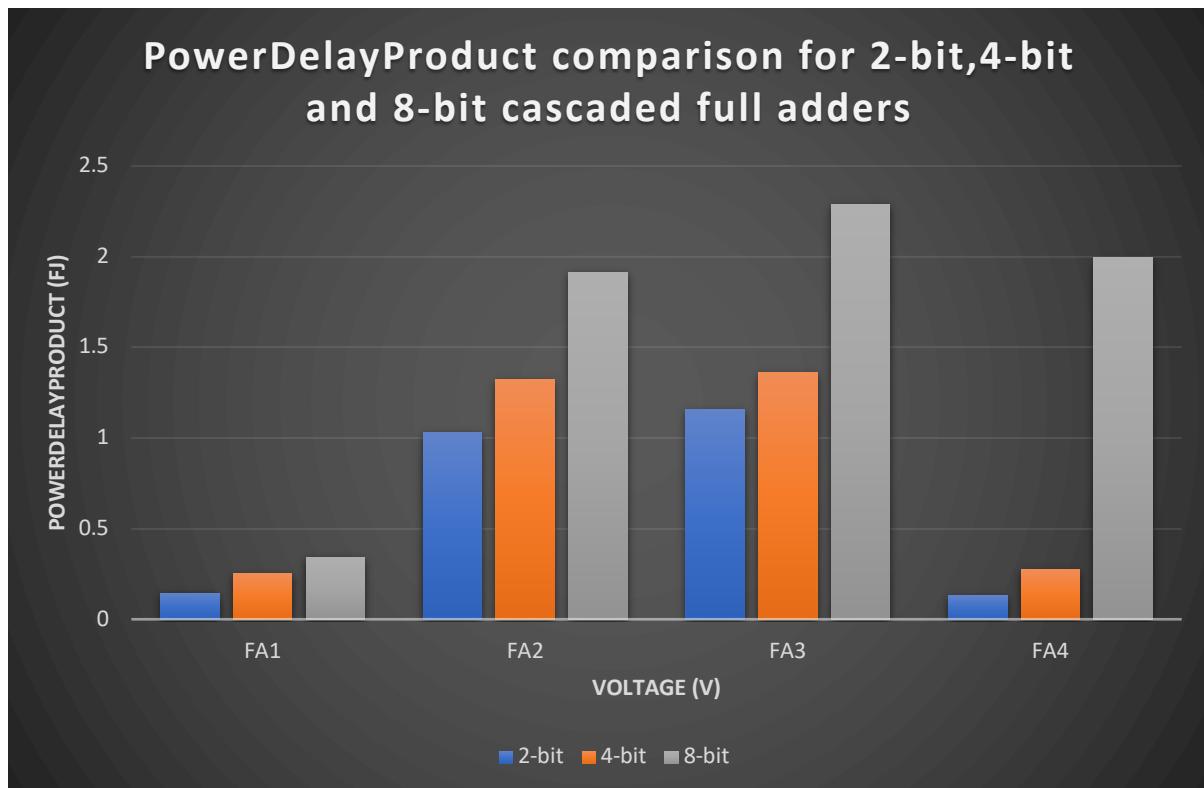
1. Delay comparison between 2-, 4-, 8- bit CFA



2. Power comparison between 2-, 4-, 8- bit CFA



3. Power Delay Product comparison between 2-, 4-, 8- bit CFA



Observations and Conclusion:

- 4 full adders have been designed using hybrid model using proposed 10T XOR-XNOR circuit
- This XOR- XNOR circuit produces both the outputs simultaneously.
- Out of all the 4 adders, full adder circuit 4 which uses CMOS logic style sum and carry circuits has been found to give the best performance
- All the full adders have been evaluated for various supply voltages from 0.6 V to 1.5 V and also at all the process corners
- The circuits have also been evaluated by cascading them to form 2-bit, 4-bit and 8-bit adders.
- Full Adder 4 is found to has the least power in 1-bit adder with power of 28.53 uW
- Full Adder 4 is found to have the best performance in 2-bit adder with PDP of 0.135 fJ

Full Adder 4 is found to have the least delay in 4-bit adder with delay of 1.8 ps

THANK YOU!!