VL 731 VLSI Arch Design
Project Proposal

Group members:

1. Divyansh Singhal, IMT2021522, Divyansh.Singhal@iiitb.ac.in
2. Daksh Sharma, IMT2021533, Daksh.Sharma533@iiitb.ac.in
3. Yash Gupta, IMT2021514, Yash.Gupta514@iiitb.ac.in
4. Chinmay Sultania, IMT2021540, Chinmay.Sultania@iiitb.ac.in

Paper Topic:

A Fully Digital SRAM-Based Four-Layer In-Memory Computing Unit Achieving Multiplication Operations and Results Store

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10109679

The paper presents several key outcomes:

1. The document presents a study on a Fully Digital SRAM-Based Four-Layer In-Memory Computing Unit (IMCU) for efficient computation.
2. The proposed IMC architecture combines data operations and processing in a memory array, reducing data transfer, lowering energy consumption, and improving computational efficiency.
3. The study demonstrates the implementation of a 4-kb SRAM-IMC macro chip using the SMIC 55-nm technology, achieving energy efficiency of 51.4 TOPS/W and a throughput of 234.3 GOPS/mm2.
4. The proposed multiplication–accumulation architecture is applied to a neural network, achieving 98.7% accuracy with the Mixed National Institute of Standards and Technology database (MNIST) dataset.
5. The study compares the proposed IMC architecture with the existing von Neumann architecture, demonstrating a significant improvement in energy efficiency and throughput.