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Experiment - 5

Aim :- Introduction to 8086 microprocessor.

Theory :-

8086 is a 16-bit microprocessor. It has 20 address lines and 16 data lines. So, it can access upto 1 MB of memory.

Architecture of 8086 microprocessor :-

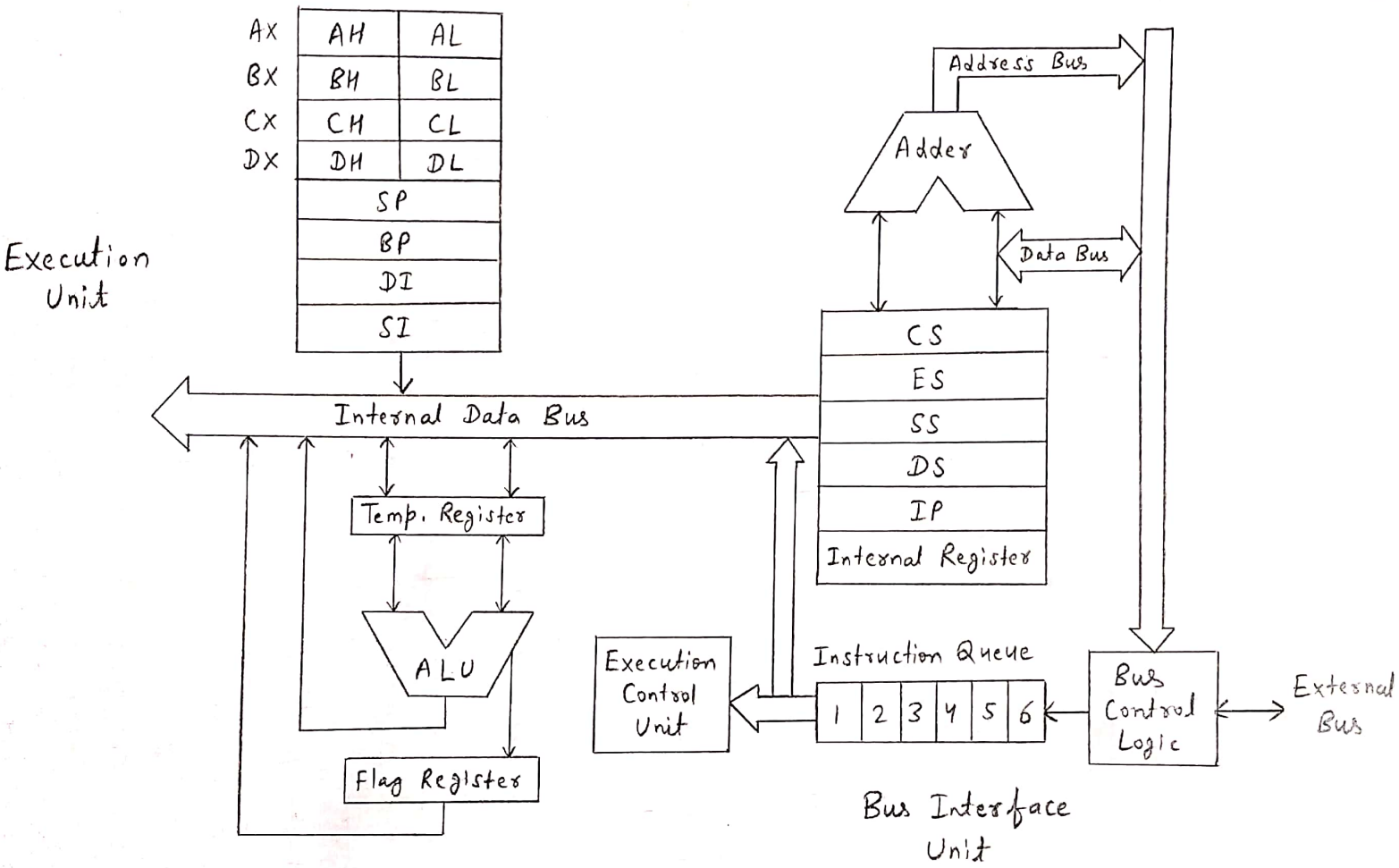
The internal architecture of Intel 8086 is divided into two units - Bus Interface Unit (BIU) and Execution Unit (EU).

The Bus Interface Unit :-

The BIU handles all data and addresses on the buses for the execution unit such as it sends out addresses, fetches instructions from memory, reads data from ports and memory as well as writes data to ports and memory. In BIU, there are so many functional groups or parts.

Instruction Queue :-

To increase the execution speed, BIU fetches as many as six instruction bytes ahead to time from memory. The pre fetched instruction bytes are held for the EU in



Architecture of 8086 Microprocessor

a first in first out group of registers called a instruction queue. When the EU is ready for its next instruction, it simply reads the instruction from this instruction queue.

Segment Registers :-
The BIU contains four 16-bit segment registers. These segment registers are used to hold the upper 16 bits of the starting address for each of the segments.

1. Code Segment (CS) :- It is used for addressing a memory location in the Code Segment of the memory, where the executable program is stored.

2. Data Segment (DS) :- The DS contains most data used by programs. Data are accessed in the Data Segment by an offset address or the content of other register that holds the offset address.

3. Stack Segment (SS) :- SS defined a section of memory to store addresses and data while a subprogram executes.

4. Extra Segment (ES) :- ES is additional data segment that is used by some of the string to hold the extra destination data.

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Instruction Pointer (IP) :- The instruction pointer (IP) holds the 16-bit address of the next code byte within this code segment.

The Execution Unit :-
The EU tells the BIU where to fetch instructions or data from, decodes instructions, and executes instructions. The functional parts of the execution unit are control circuitry or system, instruction decoder and Arithmetic Logic Unit (ALU).

Flag Register :- A 16-bit flag register is a flip flop which indicates some condition produced by the execution of an instruction or controls certain operations of the EU. It has 9 flags and they are divided into two categories - Conditional Flags and Control Flags.

Conditional Flags :- They represent result of last arithmetic or logical instructions.

1. Carry Flag (CF) :- This flag will be set to one if the arithmetic operation produces the carry in MSB position.

2. Auxiliary Flag (AF) :- If an operation generates a carry/borrow from lower nibble (D0-D3) to upper nibble (D4-D7), the AF flag is set i.e., carry given by D3 bit to D4 is AF flag.

3. Parity Flag (PF) :- If lower order 8-bits of the result contains even number of 1's, the Parity Flag is set to one and for odd number of 1's, the PF is reset.

4. Zero Flag (ZF) :- It is set to one, if the result of arithmetic or logical operation is zero else it is reset.

5. Sign Flag (SF) :- If the result of operation is negative, sign flag is set to one.

6. Overflow Flag (OF) :- An OF indicates that the result has exceeded the capacity of machine.

Control Flags :- They are intentionally set or reset to control certain operations of the processor with specific instructions put in the program from the user.

1. Trap Flag (TP) :- It allows user to execute one instruction of a program at a time for debugging. When trap flag is set, program can be run in single step mode.

2. Interrupt Flag (IF) :- If it is set, the maskable interrupt is enabled and if it is reset, the interrupt is disabled.

3. Direction Flag (DF) :- If it is set, string bytes are accessed from higher memory address to lower memory address.

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General Purpose Registers :-
The EU has four general purpose registers - AX, BX, CX and DX.

1. AX Register :- For 16-bit operations. AX is called the Accumulator register that stores operands for arithmetic operations.

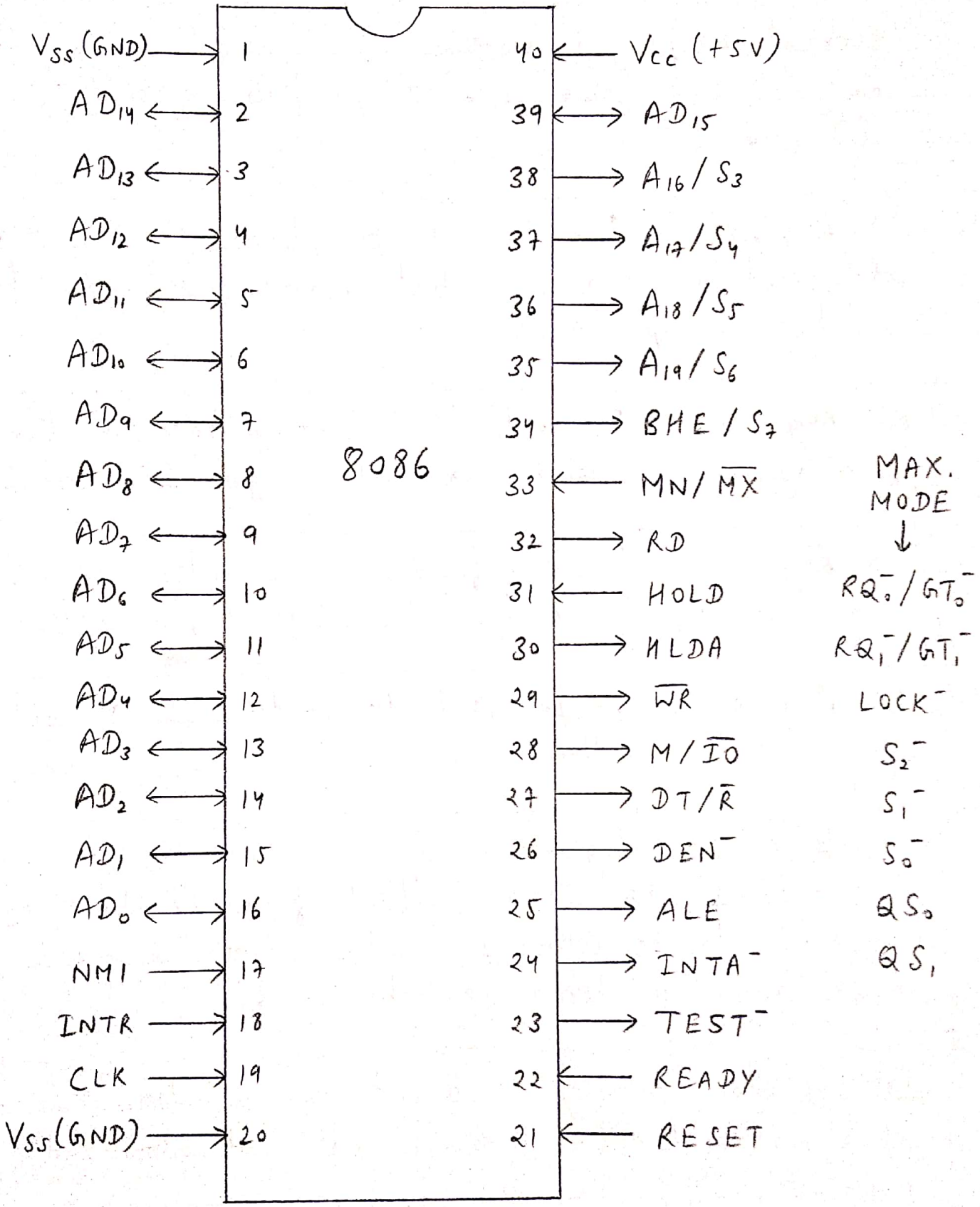
2. BX Register :- It holds the starting base location of a memory region within a data segment.

3. CX Register :- It is defined as a counter. It is primarily used in loop instruction to store loop counter.

4. DX Register :- It is used to contain I/O port address for I/O instruction.

Stack Pointer Register :-
It contains the 16-bit offset from the start of the segment to the memory location where a word was most recently stored on the stack.

The EU also contains a 16-bit source index (SI) register, base pointer (BP) registers, and Destination Index (DI) registers.



PIN DIAGRAM OF 8086

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Pin Diagram of 8086 :-
The 8086 can operate in two modes these are the minimum mode and maximum mode.

MN/MX :- It is an input pin used to select one of this mode. When it is high, the 8086 operates in minimum mode. When it is low, 8086 is configured to support multiprocessor system.

$AD_0 - AD_{15}$:- These lines are a 16-bit multiplexed address or data bus.

BHE / S7 :- It is Bus High Enable. The BHE can be used in conjunction with AD_0 to select the memory.

RD :- RD is low when the data is read from memory or I/O location.

TEST :- The 8086 enters a wait state after execution of the wait instruction until a low is seen on the test pin.

INTR :- It is a maskable interrupt input.

NMI :- It is the non maskable interrupt.

RESET :- It terminates all the activities.

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DT/R :- DT/R (Data Transmit or Receive) is an O/P signal required in system that uses the data bus transceiver.

ALE :- Address Latch Enable is used to demultiplex the AD_0 to AD_{15} lines.

M/IO :- It is an 8086 output signal to distinguish a memory access and I/O access.

WR :- It is used by the 8086 for performing write memory or write i/o operation.

INTA :- It is the interrupt acknowledgement signal.

HOLD and HLDA :- A high on the HOLD pin indicates that another master is required to take over the S/M bus.

CLK :- Clock provides the basic timing signals for the 8086 and bus controls.

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I/O Devices :-

1. 8255 (Programmable Peripheral Interface) :-
It is a programmable peripheral interface (PPI) designed to use with 8086 microprocessor. It acts as a general purpose I/O component to interface peripheral equipment's to the system bus.

2. 8253 :- (Programmable Interval Timer) :-
This chip is a programmable interval timer / counter & can be used ~~as~~ for the generation of accurate time delays under software control.

3. 8251 (USART) :-
This chip is a programmable communication interface and is used as a peripheral device.

4. 8259 (Interrupt Controller) :-
It is a device specifically designed for use in real time, interrupt driven microcomputer systems.

5. 58167 (Real Time Clock Chip) :-
The kit provides an on board RTC Chip which can be used to run the Real Time Clock on the board.

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Command Description :-

1. S (Sub_MIR) :-
Substitute - Memory (Read / Write data into / from memory).
- I/O (Read / Write data into / from Port Address).
- Register (Read / Write into / from Register).

2. M (Move) :-
Move - Block (Move a block of memory to another destination address).
- Constant (Fill a constant data byte in a memory block).

3. J (Mem_Tst) :-
Memory Test - Test a block of RAM memory for being OK.

4. E (Ex_Mon) :-
Expand Monitor - Expands the Monitor Command set for working in Assembler Mode.

5. B (Blank) :-
Blank Check - Blank check an EPROM in the ZIF socket for being Blank.

6. G (Go To) :-

Execute in - Burst (Execute a Program in Full Speed Mode)
- Sing_Stp (Execute a program in Single Step Mode).
- Break_Pt (Execute a program with Break Point).

Result :- Successfully studied the architecture, pin diagram, different chips and commands of the 8086 microprocessor.