## Experiment - 1

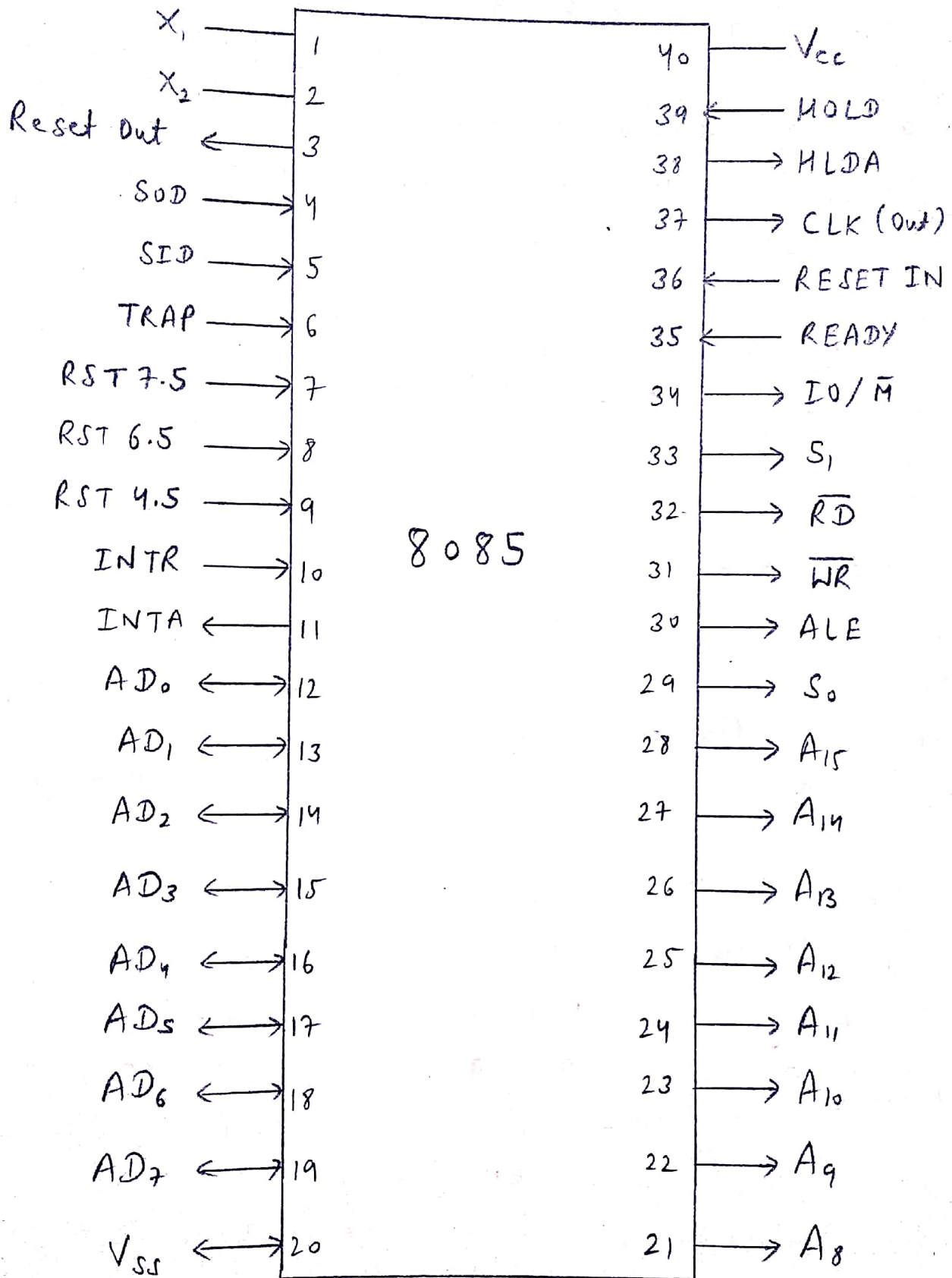**Aim :-** To study 8085 microprocessor, its architecture and function pin diagram and introduction to the 8085 kit.

**Theory :-** 8085 is an 8-bit microprocessor designed by INTEL in 1976 using NMOS technology configuration

- 8 bit data bus
- 16 bit PC
- 16 bit SP
- Six 8 bit (BC, DE, HL)
- 16 bit address bus which can address upto 64K

**Introduction to kit :-**

ET-8085 AD-LLD is a microprocessor training kit cum development kit designed around 8085 microprocessor. It has been designed to provide code in interaction with the micro-processor and various peripheral chip. The processor communicates with the outside world through $10^4$ key keyboard and LCD. System provides 16k / 32k bytes of EP ROM having monitor program and 8k bytes of RAM areas. System provides I/o through two numbers of 8225 PPI. It has 16 bit counter using 8253.
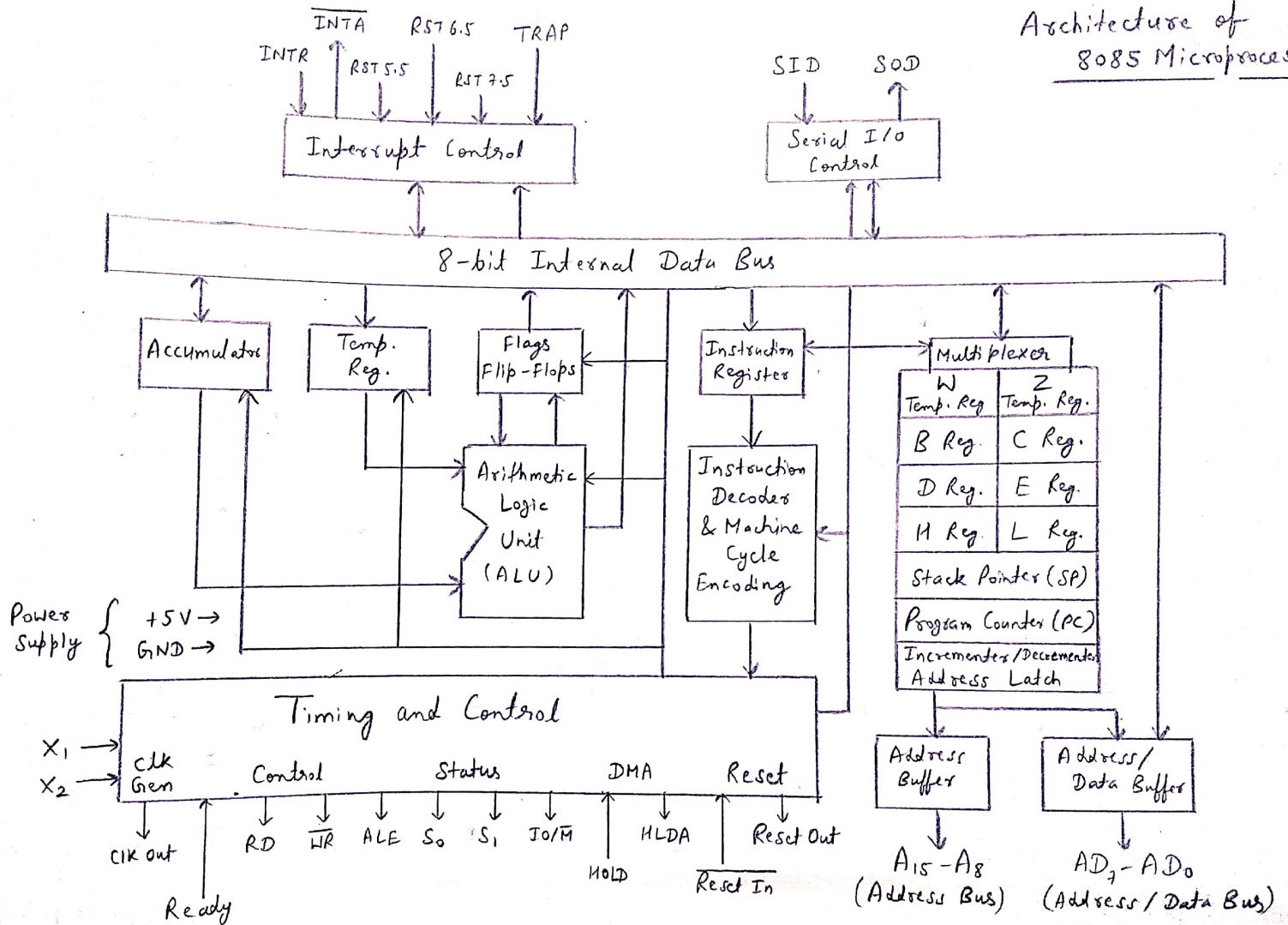
| | | | | |
|---|---|---|---|---|
| $X_1$ | — | 1 | 40 | — $V_{cc}$ |
| $X_2$ | — | 2 | 39 | ← HOLD |
| Reset Out | ← | 3 | 38 | → HLDA |
| SOD | → | 4 | 37 | → CLK (Out) |
| SID | → | 5 | 36 | ← RESET IN |
| TRAP | → | 6 | 35 | ← READY |
| RST 7.5 | → | 7 | 34 | → $IO/\bar{M}$ |
| RST 6.5 | → | 8 | 33 | → $S_1$ |
| RST 4.5 | → | 9 | 32 | → $\overline{RD}$ |
| INTR | → | 10 | 31 | → $\overline{WR}$ |
| INTA | ← | 11 | 30 | → ALE |
| $AD_0$ | ↔ | 12 | 29 | → $S_0$ |
| $AD_1$ | ↔ | 13 | 28 | → $A_{15}$ |
| $AD_2$ | ↔ | 14 | 27 | → $A_{14}$ |
| $AD_3$ | ↔ | 15 | 26 | → $A_{13}$ |
| $AD_4$ | ↔ | 16 | 25 | → $A_{12}$ |
| $AD_5$ | ↔ | 17 | 24 | → $A_{11}$ |
| $AD_6$ | ↔ | 18 | 23 | → $A_{10}$ |
| $AD_7$ | ↔ | 19 | 22 | → $A_9$ |
| $V_{SS}$ | ↔ | 20 | 21 | → $A_8$ |

8085

PIN DIAGRAM OF 8085

## List of Commands :-

| | | |
|---|---|---|
| L | - | List a memory block |
| M | - | Examine / Modify memory |
| E | - | Eenter a memory block |
| R | - | Examine / Modify Register |
| S | - | Single-step |
| G | - | Go |
| B | - | Block Move |
| I | - | Insert |
| D | - | Delete |
| N | - | Insert Data |
| O | - | Delete Data |
| F | - | File |
| H | - | Relocate |
| J | - | Memory Compare |
| K | - | String |
| P | - | Print |
| I | - | Assemble / Disassemble |

List a memory block (L) → ...
L (start address), (end address) "Shift Key" & then "y" key.

L command allows user to examine contents of a block of memory. To further see values, press <ENTER>, to exit press <ESC> key.

INTR   $\overline{INTA}$   RST 6.5   TRAP
   RST 5.5   RST 7.5

SID   SOD

Interrupt Control

Serial I/o Control

8-bit Internal Data Bus

Accumulator

Temp. Reg.

Flags Flip-Flops

Instruction Register

Multiplexer

| W Temp. Reg | Z Temp. Reg. |
|---|---|
| B Reg. | C Reg. |
| D Reg. | E Reg. |
| H Reg. | L Reg. |
| Stack Pointer (SP) | |
| Program Counter (PC) | |
| Incrementer/Decrementer Address Latch | |

Arithmetic Logic Unit (ALU)

Instruction Decoder & Machine Cycle Encoding

Power Supply { +5V →
GND →

Timing and Control

$X_1$ →
$X_2$ →
Clk Gen

Control   Status   DMA   Reset

Clk Out

Ready

RD   $\overline{WR}$   ALE   $S_0$   $S_1$   $Io/\overline{M}$   HLDA   Reset Out
                                    HOLD        $\overline{Reset In}$

Address Buffer

Address/ Data Buffer

$A_{15} - A_8$
(Address Bus)

$AD_7 - AD_0$
(Address / Data Bus)

## Examine / Modify Memory (M)
M (Start - address) <ENTER>

M command allows user to examine contents of any memory location to modify contents of RAM area.

## Enter a memory block (E)
E (Start address) <ENTER>

E command allows user to modify the contents of any memory location of RAM area.
Enter address and press <ENTER>

## Architecture :-
It is an 8-bit microprocessor designed by Intel in 1977 using NMOS technology.
It has following configurations :-
— 8 bit data bus
— 16 bit address bus which can address upto 64 kB
— A 16-bit program counter
— A 16-bit stack pointer
— Six 8-bit registers arranged in pairs BC, DE, HL.
— Requires +5 V supply to operate at 3.2 MHz single phase clock.

**Accumulator :-** It is an 8-bit register used to perform arithmetic, logical, I/o & LOAD/STORE operations. It is connected to internal data bus & ALU.

**ALU :-** As name suggest, it performs arithmetic and logical operations like addition, subtraction, AND, OR, etc on 8-bit data.

**General purpose register :-** There are 6-general purpose registers B, C, D, E, H & L, each register can hold 8-bit data.

**Flag Registers :-** 8-bit register having 5 1-bit flip flops, which holds either 0 or 1.
**Set of 5 flip flops :-** Sign (S), Zero (Z), Auxiliary carry (AC), Parity (P) and Carry (C).

**Interrupt Control :-** It control the interrupts during a process. When a microprocessor is executing a main program and whenever an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request.

**Serial I/O control :-** It controls the serial data communication by using these 2 instructions SID & SOD.

**Program Counter :-** It is a 16-bit register used to store the memory address location of the next instruction to be executed. Increments when instruction is executed.

Stack Pointer :- 16-bit register works like a stack, which is always incremented, decremented by 2 during push and pop operations.

Temporary Register :- It is an 8-bit register, which holds the temporary data of ALU operations.

Instruction Registers :- 8-bit register, when an instruction is fetched from memory then it is stored in this register.

Timing and Control Unit :- It provides timing & control signals to the micro-processor to perform operations

   Control signals - Ready, $RD$, $\overline{WR}$, ALE

   Status signals - $S_0$, $S_1$, $IO/\overline{M}$

   DMA signals - HOLD, HLDA

   Reset signals - Reset in, Reset out

## Pins of 8085 :-

→ Address Bus :- $A_{15}$-$A_{18}$ :- It carries most significant 8-bits of memory address.

→ Data Bus :- $AD_7$-$AD_0$ :- It carries rest significant 8-bits of address and data bus.

→ Control & Status signals :-

• RD :- signal indicates that the memory device is to be read.

• WR :- signal indicates that the data on data bus is to be written.

• ALE :- When ALE goes high, it indicates address bus, otherwise

**GOOD WRITE** indicates data bus when it is low.

- $IO/\overline{M}$ :- The signal is used to differentiate between I/O and memory operations.
- $S_0$ & $S_1$ :- These signals are used to identify the type of current operations.

→ Clock signals :--

- $X_1$, $X_2$ :- A crystal is connected at these 2 pins and is used to set frequency of the internal clock.
- CLK Out :- This signal is used as the system clock for devices.

→ Interrupts :-

- INTA :- Interrupt acknowledge signal.
- INTR :- This is a Maskable & non-vectored interrupt.
- TRAP :- It is non-maskable and vectored interrupt with a highest priority.
- RST 7.5 :- It is a maskable and vectored interrupt with second highest priority.
- RST 6.5 :- It is a maskable and vectored interrupt with third highest priority.
- RST 5.5 :- It is also maskable and vectored interrupt with priority higher than INTR but less than others.

→ Reset in :- Used to reset the microprocessor.

→ Reset out :- Used to reset all the connected devices.

→ Ready :- Indicates that the device is ready to send or recieve data.

→ HOLD :- Indicates that another master is requesting the use of address or data bus.

→ HLDA :- As soon as HOLD is ack., HLDA goes high, otherwise it remains low.

Power Supply – 15V, 1.5A per kit and serial I/P.
Operating Temp. – 0 – 50°C

## I/O Devices :–

→ **8255 (Programmable Peripheral Devices) :–** 8255 is a programmable peripheral devices (PPI) designed to use with 8085. This basically act as a general purpose I/o device to interface with peripheral device since the function configuration of 8255 is programmed by system software.

→ **8253 (PIT) :–** This chip is programmable interval Timer / Counter and can be used for the generation of accurate time delays under software control.

→ **8251 (USART) :–** This chip is programmable communication interface. This device accepts data character from CPU in parallel format and then converts them into serial data character for CPU.

→ **8259 (Interrupt Control) :–** 8259 is a device specially designed for use in real time ; interrupt driven microprocessor system. It manages '8' level of requests and has built in features for expandability to other 8259's.

An interface for CRT terminal or PC/AT is provided through serial interface. An additional interface is provided through 8251 USART chip.

→ <u>System Specifications</u> :-

CPU — 8 bit $\mu P$, 8085
XTAL preq. — 6.144 MHz (crystal frequency)
RAM — 8k bytes with provision for expansion
— battery backup for RAM.
EPROM — 16k / 32k bytes of EPROM.
Memory — Total on-board capacity of 64k bytes.
Timer — 10 bit programmable content using 8253.
I/O lines — 48 I/O lines with 8255
Interrupts — 8 interrupt lines through 8259
Serial Interface — RS 232 through SID & SOD lines
Other Interfaces — Additional RS 232 through R251
— A/D Controller
— D/A controller
— Relay I/P
— Opto isolated input
— Printer Input
— Real time clock
Keyboard — 101/104 key ASCII keyboard
Display — 70X21 LCD display
Bus — All data, address and Control Signals

**Result :-**

The architecture of 8085 microprocessor, pin diagram and kit of 8085 was studied. Basic occured operations were performed on 8085 kit.