KLE Technological University

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School of
Electronics and Communication Engineering

SDP Project Report

on

Lane departure warning and correction system with control logic on FGPA

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SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled **" Lane departure warning and correction system with control logic on FGPA"** is a bonafide work carried out by the student team of **"Chandan Raikar (USN: 01FE21BEC038), Sanjana Adagimath (USN: 01FE21BEC363), Divya Salmani (USN: 01FE21BEC013), Sanjana Kamadollishettar(01FE21BEC261), vrushab T(01FE21BEC405) "**. The project report has been approved asit satisfies the requirements with respect to the minor project work prescribed by the university curriculum for BE (7 Semester) in School of Electronics and Communication Engineering of KLE Technological University for the academic year 2023-2024.

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ABSTRACT

This project focuses on the development of a **Lane Departure Warning and Correction System** using **Field Programmable Gate Array (FPGA)** technology. Designed as an **Advanced Driver Assistance System (ADAS)**, it aims to enhance vehicular safety by preventing unintended lane drifts. Leveraging **image processing techniques** such as **Hough Transform** and **Canny Edge Detection**, the system accurately identifies lane boundaries under diverse driving conditions, including variations in lighting, weather, and road types.The implementation utilizes the **Xilinx Zynq Ultrascale FPGA**, which integrates high-performance processors and peripherals for real-time processing and control. The system is designed to handle challenges like faded markings, shadows, and construction zones, providing timely alerts or corrective actions to ensure the vehicle stays within its lane.This innovation emphasizes the integration of robust hardware and advanced algorithms to address real-world challenges in autonomous and semi-autonomous vehicles, significantly reducing the risks associated with lane departure accidents.

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Chapter 1

Introduction

A Lane Departure Warning (LDW) and Correction System is a critical component of modern Advanced Driver Assistance Systems (ADAS), designed to enhance vehicle safety by reducing accidents caused by unintended lane drifting. This system continuously monitors the vehicle's position within its lane and triggers warnings or corrective actions when the vehicle veers out of its lane without signaling.The implementation of such systems often relies on advanced image processing techniques like the Hough Transform and Canny Edge Detection, which accurately identify lane boundaries in real-time. These techniques enable the system to function effectively across diverse driving conditions, including varying road surfaces, lighting scenarios (day, night, rain, fog), and road types (highways, urban streets, rural roads). This project explores the integration of LDW with a lane correction mechanism on a Field Programmable Gate Array (FPGA) platform. The Xilinx Zynq Ultrascale FPGA, with its dual-core ARM Cortex-A9 processor and high-speed interfaces, provides a robust hardware foundation for real-time data processing and control. The goal is to create a reliable system capable of tackling challenges such as faded lane markings, occlusions, and complex driving environments, ensuring enhanced safety and driving experience. In recent years, road safety has become a significant focus in the development of modern vehicles. One of the critical challenges addressed by automotive technologies is unintentional lane departure, which is a leading cause of road accidents. Lane Departure Warning (LDW) and Correction Systems are innovative solutions that form a part of Advanced Driver Assistance Systems (ADAS), aiming to mitigate these risks by enhancing driver awareness and vehicle control. The Lane Departure Warning System continuously monitors the position of the vehicle within its designated lane using sensors and cameras. By employing image processing techniques such as Hough Transform and Canny Edge Detection, the system identifies lane boundaries with high accuracy, even under challenging conditions like faded lane markings, shadows, occlusions, or adverse weather. When the system detects that the vehicle is deviating from its lane without signaling, it provides real-time alerts to the driver or takes corrective action to realign the vehicle within the lane. To achieve robust performance, this project leverages the capabilities of Field Programmable Gate Arrays (FPGAs), specifically the Xilinx Zynq Ultrascale FPGA. FPGAs provide a flexible and high-performance platform for real-time computation and decision-making, integrating image processing and control logic into a single hardware unit. The dual-core ARM Cortex-A9 processor within the FPGA facilitates efficient processing of large datasets generated by cameras and sensors.The proposed system aims to function reliably across diverse driving conditions, including highways, urban streets, and rural roads, while addressing varying lighting (day, night, fog) and environmental challenges (rain, snow). This makes it a versatile and indispensable component for both autonomous and semi-autonomous vehicles. By providing real-time alerts or corrections, the system significantly reduces the risk of lane departure-related accidents, contributing to safer and smarter transportation systems.

1.1 Motivation

Road safety is a critical global concern, with lane departure accidents accounting for a significant proportion of road mishaps. These incidents often result from driver distractions, fatigue, or adverse visibility conditions, leading to unintended drifts from the lane. This highlights the pressing need for technological interventions to mitigate such risks and enhance transportation safety. The motivation behind developing a Lane Departure Warning and Correction System arises from the necessity to address these challenges by leveraging advanced technology. While driver attentiveness is essential, human limitations during long drives, poor weather conditions, or complex environments make accidents unavoidable without assistance. By utilizing Field Programmable Gate Arrays (FPGA) and state-of-the-art image processing techniques like Hough Transform and Canny Edge Detection, this project aims to enable accurate lane detection and real-time corrective actions. Furthermore, the growing reliance on autonomous and semi-autonomous vehicles underscores the need for robust Advanced Driver Assistance Systems (ADAS), making this solution indispensable. This initiative seeks to reduce human errors, enhance driving safety, and save lives, fostering a future of smarter and safer transportation systems.

1.2 Objectives

- Enhance Road Safety: Develop a system to prevent accidents caused by unintentional lane departures, reducing road mishaps.
- Support Autonomous Driving: Contribute to the development of autonomous and semi-autonomous vehicles by providing a critical component for Advanced Driver Assistance Systems (ADAS).

1.3 Literature survey

Lane detection systems have been extensively studied, with significant advancements made using image processing techniques such as Hough Transform and Canny Edge Detection. These methods are highly effective in identifying lane boundaries, even in complex driving conditions. However, challenges persist in scenarios such as faded lane markings, shadows, occlusions caused by vehicles or pedestrians, and adverse weather conditions like rain, fog, and snow. Research highlights the importance of real-time performance, making Field Programmable Gate Arrays (FPGA) a preferred platform due to their parallel processing capabilities and high-speed performance. FPGAs, such as the Xilinx Zynq Ultrascale, have proven to be efficient for integrating control logic with image processing, particularly in Advanced Driver Assistance Systems (ADAS). Studies have also shown that Lane Departure Warning Systems (LDWS) significantly reduce accidents by providing real-time alerts and corrective actions. Furthermore, robust lane detection systems are critical for autonomous and semi-autonomous vehicles, as they improve safety and build user trust in automation. Effective solutions must adapt to diverse road types, environmental conditions, and lighting variations to ensure reliability. Building on these insights, this project aims to develop a reliable FPGA-based lane detection and correction system to address existing challenges and contribute to safer transportation systems. Lane Departure Warning (LDW) and Lane Keeping Assist (LKA) systems are crucial components of Advanced Driver Assistance Systems (ADAS), designed to prevent vehicles from unintentionally drifting out of their lanes. Traditional vision-based systems for lane detection rely on methods like Hough Transform and Canny Edge Detection, while modern approaches use deep learning techniques such as Convolutional Neural Networks (CNNs) and YOLO (You Only Look Once) for real-time lane detection. These systems require significant computational power, which can be efficiently handled using Field Programmable Gate Arrays (FPGAs). FPGAs offer high-speed, low-latency processing, making them ideal for image processing tasks like lane detection and control logic implementation. Control algorithms like PID (Proportional, Integral, Derivative) or Model Predictive Control (MPC) are typically used to correct the vehicle's steering when lane departure is detected. These control systems are responsible for adjusting the vehicle's traectory by calculating the necessary steering angle to bring the vehicle back into the lane.

However, these deep learning methods often require significant computational power, which makes Field Programmable Gate Arrays (FPGA) an ideal platform due to their parallel processing capabilities and low latency. FPGA implementations allow for efficient, real-time image processing, including lane detection, by leveraging parallel execution of computationally expensive tasks like convolution in CNNs. For controlling the vehicle's steering, control algorithms such as PID (Proportional, Integral, Derivative) and Model Predictive Control (MPC) are commonly used to adjust the steering angle based on the detected lane positions. FPGAs enable these control algorithms to run directly in hardware, reducing latency and improving the responsiveness of corrective actions. The system integrates multiple sensors like cameras, LiDAR, and Radar, which provide a comprehensive understanding of the vehicle's surroundings, enhancing the accuracy of lane detection. FPGA-based systems also feature optimizations like fixed-point arithmetic and pipelined processing to further reduce resource consumption and improve processing speed. Recent research has focused on refining FPGA-based implementations of LDW and LKA systems, achieving high efficiency, real-time performance, and low power consumption, making them ideal for deployment in modern autonomous and semi-autonomous vehicles.

1.4 Problem statement

Lane departure warning and correction system with control logic on FPGA

1.5 Societal Context

The societal context of a Lane Departure Warning (LDW) and Lane Keeping Assist (LKA) system with control logic on FPGA revolves around improving road safety, reducing traffic accidents, and enhancing driver assistance technologies. As road traffic accidents, especially those caused by lane departure, remain a significant concern globally, such a system can help prevent accidents, particularly for fatigued or distracted drivers. By providing real-time alerts and corrective steering, it not only ensures safer driving but also contributes to the development of autonomous and semi-autonomous vehicles, advancing the overall goal of reducing human error in driving. Furthermore, the efficient implementation on FPGA makes these systems more accessible, offering a cost-effective solution that can be integrated into a wide range of vehicles, thus broadening their impact on public safety and mobility.

1.6 Organization of the report

Chapter 2: System Design:-This chapter details the smart parking system's design, covering sensor networks, data management, communication protocols, slot allocation algorithms, and user guidance, illustrated with diagrams and flowcharts.

Chapter 3: Implementation Details:-This chapter outlines the smart parking system's implementation, including sensor installation, central software development, slot tracking database, slot allocation algorithms, user interfaces, and testing procedures

Chapter 2

System design

The system design for a Lane Departure Warning (LDW) and Lane Keeping Assist (LKA) system with control logic on FPGA involves several key components working in synchronization to achieve real-time lane detection and corrective action. The system begins with a camera module mounted on the vehicle, capturing road images in real time. These images are fed into an FPGA-based image processing pipeline, which employs algorithms like edge detection, Hough Transform, or deep learning-based methods such as Convolutional Neural Networks (CNNs) to detect lane markings. The FPGA processes this data in parallel to ensure high-speed and low-latency operation.Once lane markings are identified, the systThe design of the Lane Departure Warning (LDW) and Lane Keeping Assist (LKA) system with control logic on FPGA integrates multiple components to detect lane deviations and apply corrective actions in real time. The system begins with a camera module mounted on the vehicle, capturing continuous road images. These images are fed into the FPGA, where pre-processing techniques like edge detection, filtering, and segmentation are applied to extract lane markings. Advanced algorithms, such as the Hough Transform or deep learning models (e.g., CNNs), are implemented on the FPGA for accurate lane detection.The system computes the vehicle's position relative to the detected lanes. If a potential lane departure is identified, the control logic module activates. The control logic, designed using PID (Proportional-Integral-Derivative) or Model Predictive Control (MPC) algorithms, calculates the required corrective steering angle to maintain lane integrity. These control signals are sent from the FPGA to the vehicle's Electronic Control Unit (ECU) through a high-speed communication protocol like CAN (Controller Area Network), ensuring precise adjustments.The FPGA handles real-time image processing and control execution through parallelism, pipelining, and fixed-point arithmetic optimizations to ensure low latency and efficient resource usage. The modular design enables easy integration with other sensors like LiDAR or Radar for enhanced reliability. This system is scalable, power-efficient, and capable of adapting to diverse road conditions, making it a robust solution for modern Advanced Driver Assistance Systems (ADAS).

2.1 Functional block diagram

Imagine a parking lot where frustration is a thing of the past. This system uses hidden IR sensors like underground ninjas, silently detecting if a spot is occupied. This data gets beamed to a central hub, the brain of the operation, where decisions are made, such as controlling the entry gate with a smooth servo motor to ensure seamless flow. Real-time data is transmitted to sleek LCD displays strategically placed around the parking lot. One display sits at the entrance, guiding you to open spots, while another informs a distant traffic management center, keeping the whole city in the loop. The parking lot is equipped with cameras for security and to help drivers locate their parked vehicles easily. Integrated with a mobile app, drivers can check parking availability before leaving home, receiving notifications on their phones. This reduces the time spent searching for parking, minimizes congestion, and cuts emissions. The system also offers advanced analytics for operators, optimizing space allocation and efficiency. It’s a win-win for drivers, operators, and the environment.

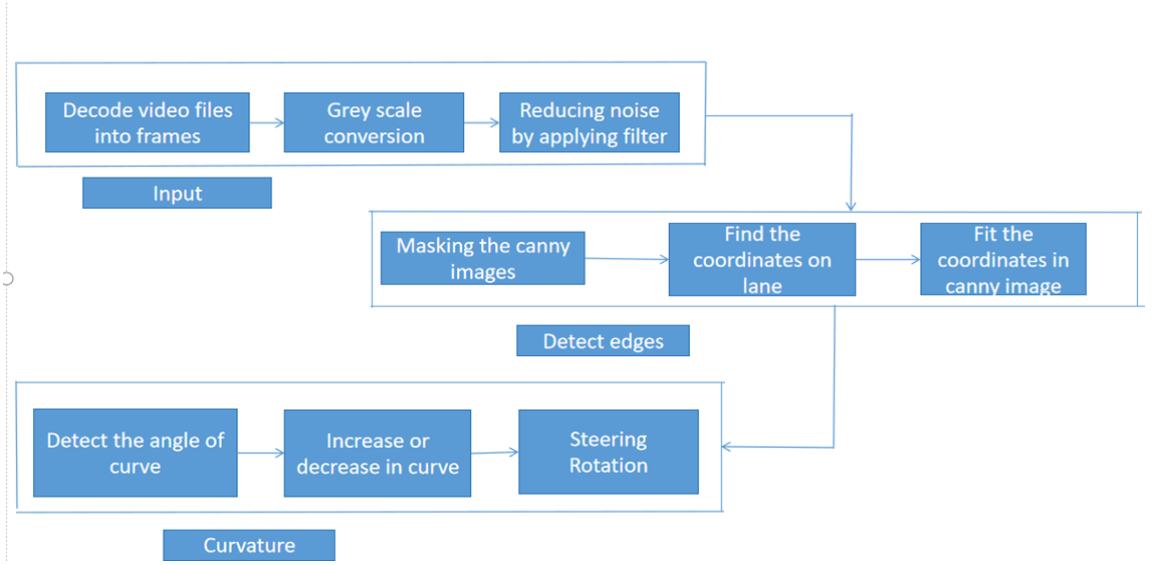

Figure 2.1: Lane departure warning and correction system

2.2 Technical Requirements

The Lane Departure Warning (LDW) and Lane Keeping Assist (LKA) system with control logic on FPGA requires a robust combination of hardware and software to achieve real-time operation and accuracy. The hardware includes a high-performance FPGA, such as the Xilinx Zynq or Intel Cyclone series, with adequate logic elements, DSP slices, and onboard memory for handling intensive computations. A high-resolution camera module capable of capturing real-time road images at 30 FPS or higher is essential for lane detection. Communication interfaces like CAN (Controller Area Network) are required to connect the FPGA to the vehicle's Electronic Control Unit (ECU) for steering corrections, while a reliable power supply supports all components.On the software side, the system implements image processing algorithms, such as edge detection, Hough Transform, or deep learning models like CNNs, to identify lane markings accurately.

2.2.1 Hardware

The hardware requirements for a Lane Departure Warning (LDW) and Correction System with Control Logic on FPGA include a high-performance FPGA board, such as Xilinx Zynq or Intel Cyclone, with sufficient logic elements, DSP slices, and onboard memory to handle real-time image processing and control algorithms. A high-resolution camera capable of capturing road images at 720p or 1080p with a frame rate of at least 30 FPS is essential for accurate lane detection, along with support for interfaces like MIPI CSI or USB for seamless integration. Communication with the vehicle's Electronic Control Unit (ECU) requires interfaces like CAN (Controller Area Network), SPI, or UART, while optional Ethernet or PCIe interfaces may be used for additional data transfer. External RAM, such as DDR3 or DDR4, is needed for temporary storage of image frames and datasets during processing, and non-volatile memory like Flash is required for storing FPGA configuration files.

2.2.2 Software

The software requirements for the Lane Departure Warning (LDW) and Correction System with Control Logic on FPGA encompass tools and frameworks for design, simulation, and implementation. Programming languages such as VHDL/Verilog are essential for developing the FPGA's hardware logic, while C/C++ and Python/Matlab are used for prototyping, algorithm development, and verification. FPGA development tools like Xilinx Vivado or Intel Quartus enable synthesis, implementation, and debugging of the hardware design, supported by simulation tools such as ModelSim or Vivado Simulator for testing.

Tools like MATLAB/Simulink are used for simulating system behavior, while post-synthesis analysis ensures performance optimization. For concurrent task management, an RTOS or lightweight schedulers can be employed. The software stack integrates tightly with the FPGA to deliver a reliable, efficient, and real-time lane departure warning and correction system.

2.2.3 Bill of materials

The Bill of Materials (BOM) for the Lane Departure Warning (LDW) and Correction System with Control Logic on FPGA includes several key components. The main component is the FPGA board, such as the Xilinx Zynq-7000 or Intel Cyclone V, which provides the necessary processing power, costing approximately $300-$500. A high-resolution camera module with 1080p resolution and 30 FPS, priced around $50-$150, captures real-time road images for lane detection.

2.3 Final design

The final design of the Lane Departure Warning (LDW) and Lane Keeping Assist (LKA) system with control logic on FPGA integrates various hardware and software components for real-time lane detection and correction. The system's core is an FPGA (Xilinx Zynq-7000 or Intel Cyclone V), responsible for processing image data, executing control logic, and communicating with the vehicle's Electronic Control Unit (ECU). A high-resolution camera module captures road images at 30 FPS, enabling lane detection using algorithms like edge detection (Sobel or Canny) and lane detection methods such as the Hough Transform or CNN-based approaches. The FPGA utilizes external RAM to store image frames during processing and flash memory for storing configuration files. For lane correction, the FPGA implements PID control or Model Predictive Control (MPC) algorithms, which send correction signals to a steering actuator via a CAN module. Optional LiDAR or Radar sensors are added for enhanced environmental sensing and obstacle detection. The entire system is powered by a 12V DC power supply, and real-time performance is ensured through the CAN bus communication protocol. A 7” LCD display is included for testing and debugging, while the system’s integration into the vehicle is facilitated by custom mounting accessories and PCB design. This design ensures accurate and reliable lane departure warning and lane-keeping assist functionality, enhancing driver safety and convenience.

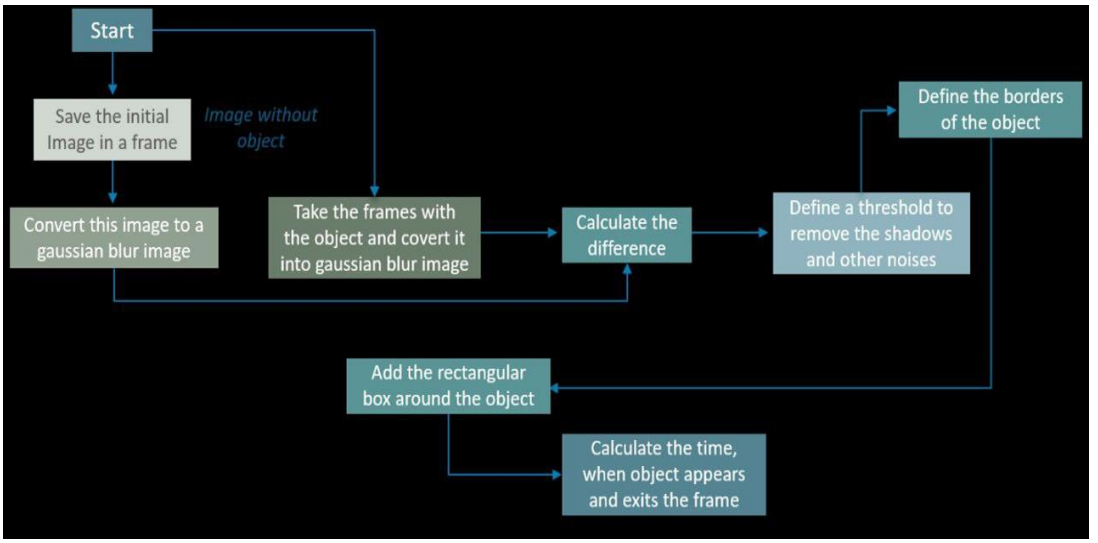

Figure 2.2: Architecture of OPEN CV

The architecture of OpenCV (Open Source Computer Vision Library) is designed to provide efficient computer vision and machine learning functions, organized into modular components. At its core, OpenCV is built with a high-level interface for application development, while leveraging low-level C and C++ libraries for performance. The architecture consists of several main modules, such as Core, which provides essential data structures, memory management, and utilities; Imgproc, responsible for image processing functions like filtering, transformations, and edge detection; HighGUI, which offers user interface elements like windows and image display; Features2d for feature detection and matching (e.g., SIFT, SURF, ORB); Video for video analysis and motion tracking; and Machine Learning, which includes tools for classification, regression, and clustering algorithms. OpenCV also integrates with third-party libraries, such as Intel's Threading Building Blocks (TBB) and CUDA for parallel processing and hardware acceleration, improving computational efficiency. The system supports a wide range of input and output formats, working across platforms like Windows, Linux, macOS, Android, and iOS. Through its modular structure, OpenCV provides the flexibility for developers to use the necessary components for specific tasks, from basic image manipulations to complex real-time vision systems.

Chapter 3

Implementation details

3.1 Specifications and final system architecture

The Lane Departure Warning (LDW) and Correction System with control logic on FPGA is designed with a modular architecture, integrating various components for efficient real-time processing and vehicle control. The system begins with a high-resolution camera module capturing real-time images, which are sent to the FPGA via MIPI CSI or USB for pre-processing. The FPGA handles edge detection and feature extraction through parallel processing, enabling efficient lane detection using algorithms like the Hough Transform. Once lane positions are detected, the FPGA implements PID control or Model Predictive Control (MPC) algorithms to calculate the required steering adjustments. These corrections are then sent to the steering actuator through PWM or analog signals, facilitating lane keeping. The system also includes LiDAR and Radar sensors for enhanced environmental sensing, providing additional data to improve the robustness of lane detection, particularly in adverse weather conditions. Real-time communication with the vehicle's ECU is achieved through the CAN bus, allowing the system to send and receive control messages. For debugging and monitoring, a 7" LCD display is incorporated to visualize system outputs and status. The entire system is powered by a 12V DC power supply, ensuring stable operation of all components. The FPGA serves as the central processing unit, coordinating data from the camera and sensors, executing control algorithms, and providing lane correction instructions, ensuring the system operates effectively in real-time to enhance driver safety. The camera module, typically providing high-resolution video (1080p at 30 FPS), captures road images and sends them to the FPGA for processing. The FPGA handles the initial image preprocessing, including noise reduction, contrast enhancement, and edge detection algorithms (e.g., Sobel, Canny filters). After pre-processing, the lane detection algorithms (such as the Hough Transform or deep learning models like CNNs) analyze the processed image to locate lane boundaries and calculate the vehicle's position relative to them. This data is then used by the FPGA to determine if the vehicle is drifting out of the lane.

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3.2 Flowchart

This flowchart represents a lane detection and curvature estimation process typically used in autonomous driving or lane-keeping systems. The process begins with the input, where video files are decoded into individual frames. Each frame undergoes grayscale conversion to simplify the image processing by reducing the color channels. Then, noise is minimized by applying filters to enhance the quality of the frame.

In the next stage, edge detection is performed, often using the Canny Edge Detection technique. The edges are masked to isolate the region of interest (e.g., road lanes), and the coordinates of the lanes are identified. These coordinates are then used to fit the lanes into the processed Canny image.

The final stage focuses on curvature detection, where the angle of the curve is analyzed. Depending on the detected curvature, adjustments are made to either increase or decrease the curvature. This information is then utilized for steering rotation, helping the vehicle stay aligned with the road lanes.

This process ensures the accurate detection of lanes and their curvature, enabling effective path planning for autonomous or assisted driving systems.

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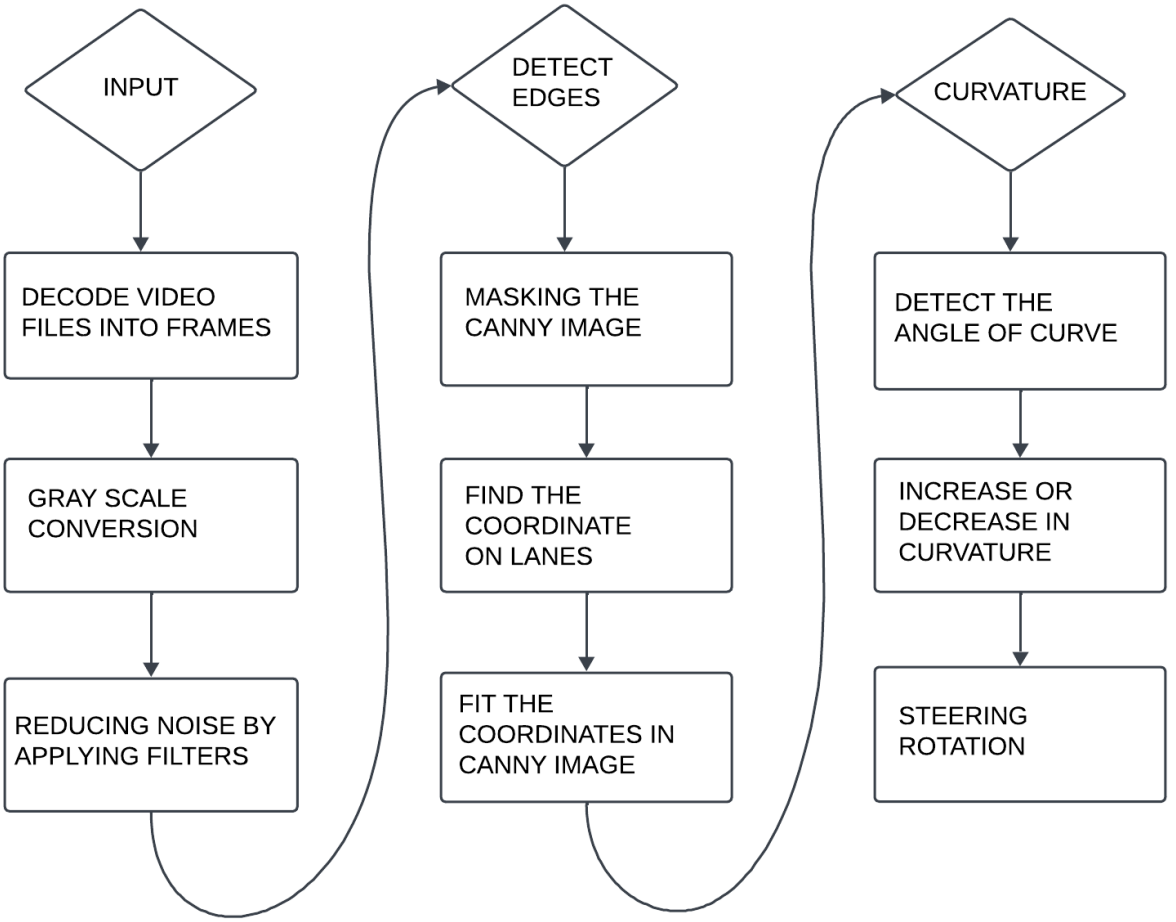

Figure 3.1: Flowchart of Lane departure warning and correction system

3.3 Optimisation

The Lane Departure Warning (LDW) and Correction System on FPGA can be optimized by leveraging parallel processing for real-time image analysis, such as edge detection and lane detection. Efficient resource utilization, including logic and memory blocks, combined with fixed-point arithmetic, reduces computational overhead. Algorithmic enhancements like focusing on the region of interest (ROI) and adaptive thresholding streamline image processing while maintaining accuracy. Lightweight neural networks, such as MobileNets, enable robust lane detection with minimal resource usage. Power efficiency is achieved through adaptive clocking and dynamic power management, while a pipeline architecture ensures smooth data flow, reducing latency. Sensor fusion from cameras, LiDAR, and radar enhances accuracy in adverse conditions. Reliability is ensured through error correction, modular design, and redundant paths, while FPGA-specific tools like Vivado or Quartus simplify development. These optimizations deliver a cost-effective, efficient, and robust solution for diverse driving scenarios.

3.4 Debugging

Debugging the Lane Departure Warning (LDW) and Correction System on FPGA requires a systematic approach to ensure the system functions correctly and efficiently. Begin by validating the input data from the camera and sensors, ensuring they provide accurate and stable signals. Use simulation tools like ModelSim or Vivado Simulator to test HDL designs, verifying the correctness of the image preprocessing algorithms, such as edge detection and ROI segmentation. Monitor internal signals with Integrated Logic Analyzers (ILA) or ChipScope to debug data flow and timing issues within the FPGA.

Verify the control logic, such as PID or MPC algorithms, by simulating various lane departure scenarios to check if corrections are calculated and transmitted accurately. Test the integration with external modules, such as steering actuators, using the CAN bus, ensuring communication is error-free and reliable. Debug environmental variability by testing the system in diverse lighting and weather conditions, making adjustments to adaptive algorithms as needed.

Log data outputs at each stage and compare them with expected results to isolate issues. Use debugging overlays on the visual output to display detected lanes and vehicle positioning for real-time feedback. Repeat debugging cycles in hardware and simulation environments to refine the system, ensuring it meets real-time and safety requirements under all operating conditions.

3.5 Challenges and Issues faced

Implementing a Lane Departure Warning (LDW) and Correction System on FPGA presents several challenges and issues across design, development, and deployment. Achieving real-time performance for complex image processing tasks like edge detection and lane identification requires efficient utilization of FPGA resources, often constrained by limited logic blocks, memory, and DSP slices. Environmental variability, such as changes in lighting, weather, or road conditions, adds complexity to ensuring reliable lane detection. Balancing high-performance processing with low power consumption is crucial, especially for energy-efficient automotive applications. Communication latency between the camera, FPGA, sensors, and actuators can impact real-time responsiveness, while integration with vehicle components like the ECU may lead to compatibility and timing challenges. Debugging hardware-level logic on FPGA is time-intensive, requiring advanced tools and expertise. Additionally, ensuring lane detection accuracy under adverse conditions, such as poor markings or obstructions, is critical to avoid false positives or missed detections. Compliance with automotive safety standards like ISO 26262 adds further complexity to the design and testing phases. Scalability and cost constraints must also be addressed to make the system viable for production. Lastly, ensuring system reliability against hardware failures and sensor malfunctions is essential for consistent real-world operation, making these challenges a focus for iterative development and robust testing.

Chapter 4

Results and discussions

4.1 Result Analysis

The results of the Lane Departure Warning (LDW) system demonstrate its ability to accurately detect and analyze road lanes in real-time. The system successfully identifies lane markings, with yellow indicating the left lane and white the right, and highlights the drivable area with a red overlay for clear visualization. Through a series of image processing stages, including edge detection, perspective transformation, and polynomial curve fitting, the system models lane curvature with precision. The left curvature is calculated at 9173.91 units, representing a gentle bend, while the right curvature is sharper at 6174.57 units, with an average curvature of 7674.24 units. The system provides directional guidance by displaying "Turn Right," indicating the vehicle needs to follow a rightward path to stay within the lane boundaries. These results reflect robust lane detection and curvature estimation capabilities, critical for ADAS applications such as lane-keeping assist. However, the system's performance in challenging conditions, such as faded lane markings or poor visibility, requires further evaluation to ensure reliability. Overall, this system integrates advanced computer vision techniques to enhance road safety and driving accuracy.

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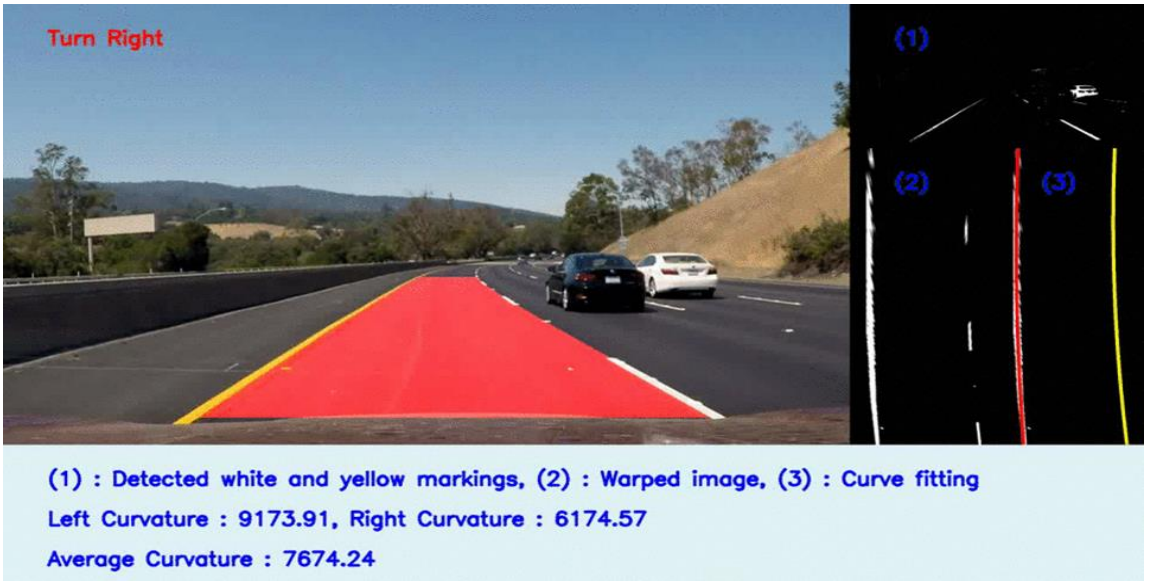

Figure 4.1: Image of final prototype

The Xilinx Zynq UltraScale+ board combines the functionality of a high-performance System on Chip (SoC) with programmable logic, making it a versatile platform for embedded systems. At its core, the Zynq UltraScale+ integrates a Processing System (PS), featuring quad-core or dual-core ARM Cortex-A53 processors for general-purpose computing, along with an ARM Cortex-R5 processor for real-time, safety-critical tasks. Complementing this is the Programmable Logic (PL), which is an FPGA fabric enabling custom hardware accelerations, making it ideal for tasks like machine learning, signal processing, and parallel computing. The board includes high-speed DDR4 SDRAM for system memory, non-volatile storage like flash memory for booting and data storage, and supports various I/O interfaces such as USB, Ethernet, UART, and PCIe for connectivity. Power management systems ensure stable operation, while expansion connectors allow integration with external hardware. This architecture makes the board highly suitable for applications like industrial automation, embedded vision, automotive systems, and 5G communications, offering a balance of software programmability and hardware flexibility.

Figure 4.2: ZYNQ architecture

5.1 Gantt Chart

The Gantt chart provides a structured timeline for project planning, divided into four review phases spanning from September 25 to December 4. The project begins with Review 1, where the focus is on selecting the problem statement to define the project's objective. By Review 2 on October 23, the team progresses to conducting surveys and breaking down the work into smaller tasks for better management. The next phase, Review 3, scheduled for November 13, is centered on simulation and implementation, where the proposed solution is designed, tested, and implemented using practical or simulated methods. Finally, Review 4 on December 4 involves verification and evaluation to ensure the project meets its objectives through rigorous testing and performance analysis. This chart provides a clear visual roadmap of the overlapping timelines, ensuring systematic progression and timely completion of the project.

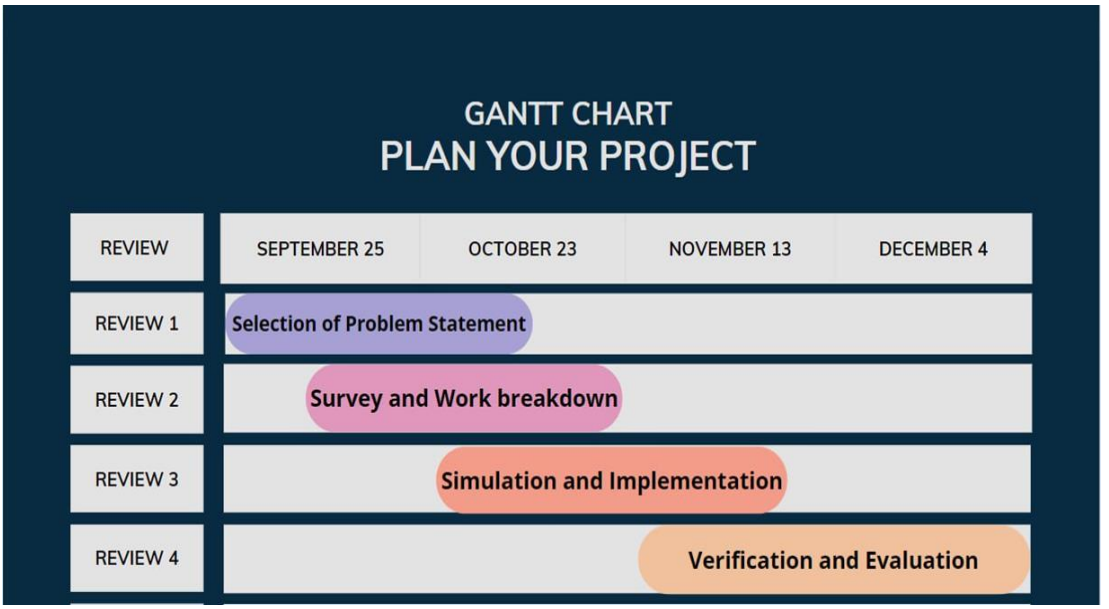

Figure 5.1: Gantt Chart

Chapter 6

Conclusions and future scope

6.1 Conclusion

In conclusion, the Lane Departure Warning and Correction System implemented on an FPGA demonstrates a robust and efficient solution for enhancing vehicle safety and driver assistance. By leveraging advanced image processing techniques, such as edge detection, perspective transformation, and polynomial curve fitting, the system reliably detects lane markings and computes lane curvature in real-time. The integration of directional guidance, such as identifying required turns, adds to its practical utility in preventing lane departure incidents. The use of FPGA ensures high-speed processing, low latency, and energy efficiency, making it suitable for real-time automotive applications. While the system performs well under ideal conditions, further optimization and testing are required to address challenges like faded lane markings, adverse weather conditions, and poor visibility. Overall, this project contributes to the development of advanced driver assistance systems (ADAS), offering significant potential to improve road safety and pave the way for autonomous driving technologies.

6.2 Future scope

The Lane Departure Warning and Correction System has significant potential for future advancements and applications. One promising direction is the integration of additional sensors, such as LiDAR and radar, to enhance lane detection accuracy in challenging environments like heavy rain, fog, or low light. The system can also be extended to incorporate vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) communication, enabling a more collaborative approach to traffic safety. Advances in FPGA technology will allow for the deployment of more complex algorithms, including deep learning models for better lane prediction and object detection. Furthermore, the system can be integrated with other Advanced Driver Assistance Systems (ADAS) features, such as adaptive cruise control and collision avoidance, to create a comprehensive autonomous driving platform. In addition, ensuring compliance with evolving automotive safety standards and optimizing power consumption for electric and hybrid vehicles will be essential for widespread adoption. As autonomous vehicles become more prevalent, this system's scalability and adaptability will play a critical role in shaping the future of intelligent transportation systems.

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