1)

a) Node degree – Node degree is referred as the number of links from the particular node either to the interconnection or the associated hardware in the topology.

b) Network diameter – In terms of interconnection networks, the network diameter is defined as the maximum routing distance possible in a network. Or it can also be termed as the minimum distance between the farthest nodes in a network.

c) Bisection bandwidth – It is the minimum bandwidth of all the links crossing a network which is split onto two roughly equal halves.

d) Static (direct) networks – A static or a direct network is referred as the network in which all the endpoint nodes sit inside the network topology itself.

e) Dynamic networks - A dynamic or an indirect network is referred as the network in which the endpoint sits outside the network topology.

f) Non-blocking network – In this type of network topology, it is possible for the network continues to operate even when there are packets from different sources to different destinations using the same link. Crossbar network topology is an example of a non-blocking network.

g) Multi-stage network – Splitting a large switch into several smaller stages of switches which are connected in a way such that a single pass allows any destination to be reached from any source point. Such networks are referred as the multi-stage networks or even multistage switch fabrics.

h) Crossbar switches – Crossbar switches is a centralized switched network technique in which a single switch can interconnect a set of devices when the number of devices is less than or equal to the number of switch ports.

i) Shared media networks – One of the simplistic network techniques to connect multiple devices by sharing the same networking medium between the connected devices.

j) Switched Networks – Instead of sharing the entire media at once with all the connected devices, switched network devices work by switching the media between the nodes. They usually create a point-to-point link between the active switch components and hence dynamically establish communication channels.

k) Network flow control – To ensure reliable delivery of packets there are certain responsibilities beyond the packet transport. One of them is to ensure that the packet isn't garbled or lost in transit and other is to ensure that the sender doesn't send the packets faster than anticipated by the consumer – this is known as the network flow control. This can be achieved by a simple handshaking or even a credit-based flow control.

l) Network topology – Network topology specifies the way switches are wired and also affects the routing, throughput, reliability, latency, etc of the entire network chain.

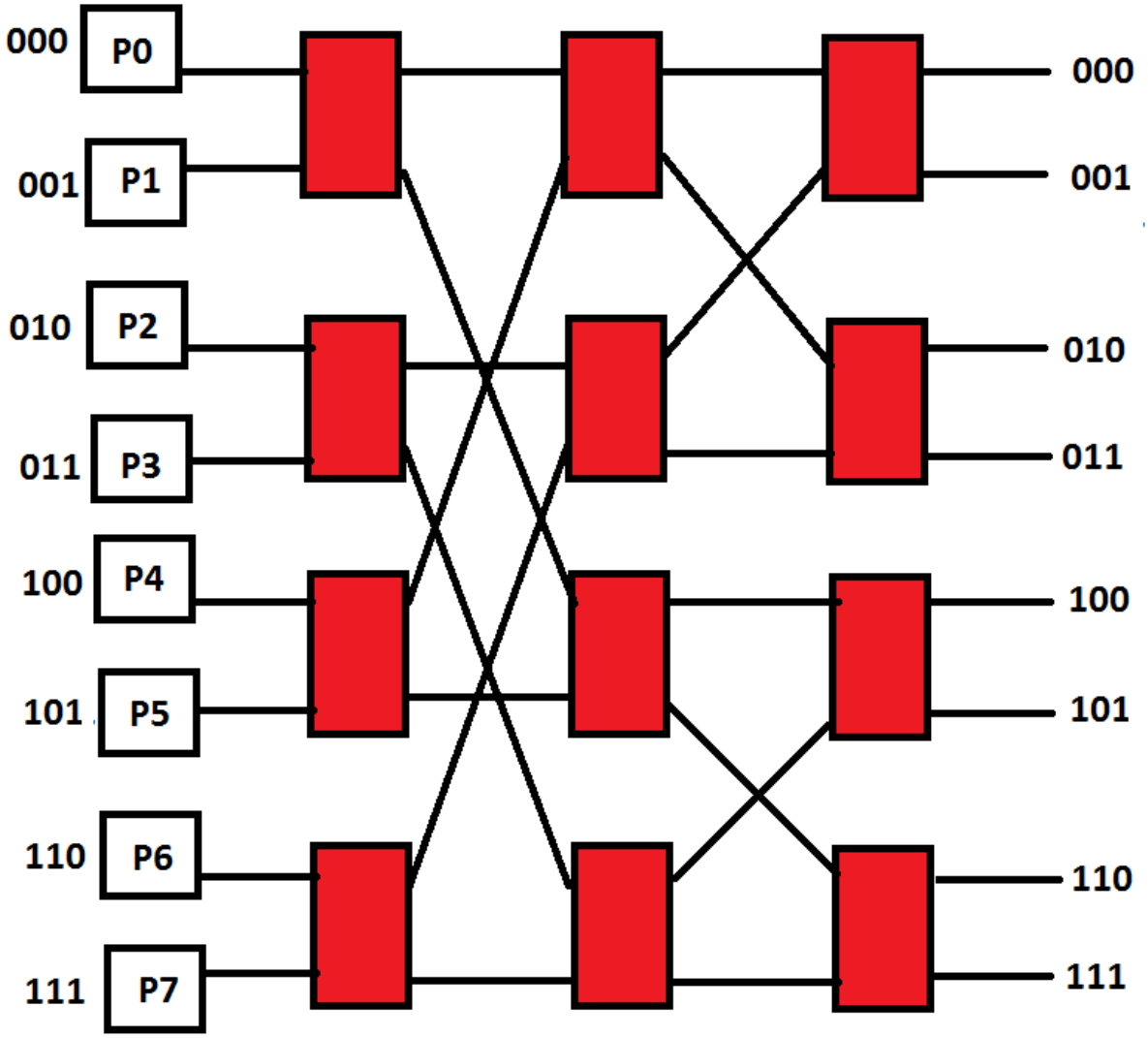
m) Routing – Routing refers to the way of transmitting the packet from the source to the final destination of the packet. This could be either static or dynamic in nature.

n) Arbitration – Most of the interconnection networks contain many shared paths, hence it is possible that among different shared paths, different devices may request some shared resources at the same time. The arbitration function is required to resolved when this happens i.e. this function decides the outcome when different devices request same shared paths at same time.

o) Switching fabric – In case of the switched networks, the switch components establish connection between the source and the destination point. These passive and active components together are known as the network switch fabric.

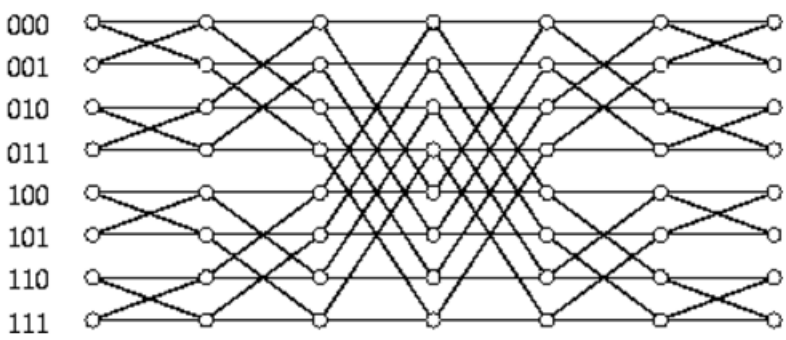
2)

a) Omega Network -



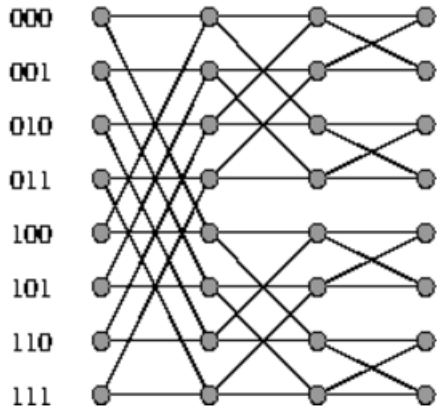
Simple routing scheme – The switches can be activated based on the destination of the packet. This type of routing algorithm is known as the destination tag routing. The upper most bit (most significant bit) can be used to decide which output to be selected for each stage of the network.

Benes Network -



Simple routing scheme – One of the routing techniques for Benes network is the use of looping algorithm. The looping algorithm decomposes the given permutation into sub-permutations which could be routed independently in their own subnetworks.

Butterfly Network -



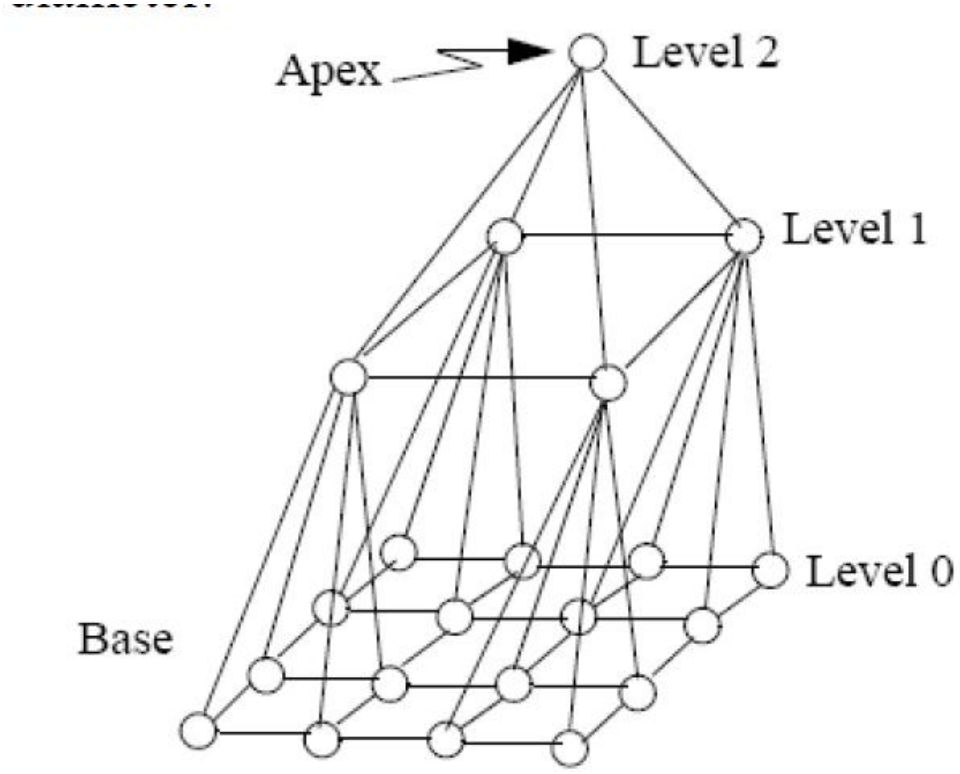
Simple routing – The routing algorithm used could be the “greedy butterfly algorithm”. In this each packet is constrained to follow its own greedy path thus leading to a unique path from level 0 onwards.

b) In a non-blocking interconnection every node is connected to all the other nodes. – In this type of network topology, it is possible for the network continues to operate even when there are packets from different sources to different destinations using the same link. The best way to design a non-blocking interconnection is using the “Crossbar network”. It is good for a small number of nodes since every node would be connected to others. This type of connection has low latency and high throughput. The only downside of such a network is that it is not scalable and grows at the rate of $O(n^2)$. Other non-blocking networks could be Clos network which makes use of large switches in middle of two other switch stages to establish alternative paths through the middle stage switches. Hence, the main factor behind designing a non-blocking interconnection is to make sure that the network paths aren’t blocked when paths from different sources to different destinations share the same link.

c) Major components of switch microarchitecture include the following –
i) Internal crossbar – The main reason behind using an internal crossbar in a switching network is to ensure a high performance non-blocking connectivity within the switch which allows concurrent connections between multiple input-output port pairs.
ii) Queues (FIFOs) – First in, first out buffers are used for buffering the blocked packets. These queues are usually implemented as dynamically allocatable multi-queues (DAMQs) which provides more flexibility and high capacity. Such queues can be used either at the input, output or within the switch as well to allow functions like input buffered switch, output buffered switch or centrally buffered switch. Combinations of input and output can also be used.
iii) Routing Control unit – Routing refers to the way of transmitting the packet from the source to the final destination of the packet. Routing is usually implemented as a finite-state machine or by using a forwarding table mechanism within the routing control unit of the switch. In FSM technique the routing information is present in the packet header which is used by the state to determine the next state of the routing algorithm. In the forwarding table technique the routing information present in

the packet header acts like an address to index the table which contains the allowed switch output ports as per the routing algorithm. Hybrid of these two techniques also exists where some logic is implemented as a forwarding table and rest is implemented as an FSM.
iv) Arbitration Unit - Most of the interconnection networks contain many shared paths, hence it is possible that among different shared paths, different devices may request some shared resources at the same time. The arbitration function is required to resolved when this happens i.e. this function decides the outcome when different devices request same shared paths at same time. Switch arbitration can be either centralized or even distributed. In centralized approach all the requests and status information needs to be transmitted to the arbitration unit which then decodes the outcome. For distributed units the arbitration logic is distributed across the switch and thus arbitration may be performed multiple times on the same packet. Usually, a hierarchical approach is used wherein some of the arbitration is done locally on every input stage and later arbitration is done globally to process the request of each of the incoming local arbiter.
v) Link Flow Control – The link control is responsible for decoding and generating the sequence of bits when the packet arrives at the switch input port. It is also responsible for deserialising the data to adapt them to the width of the internal switch data path and also extracts packet information from the headers.

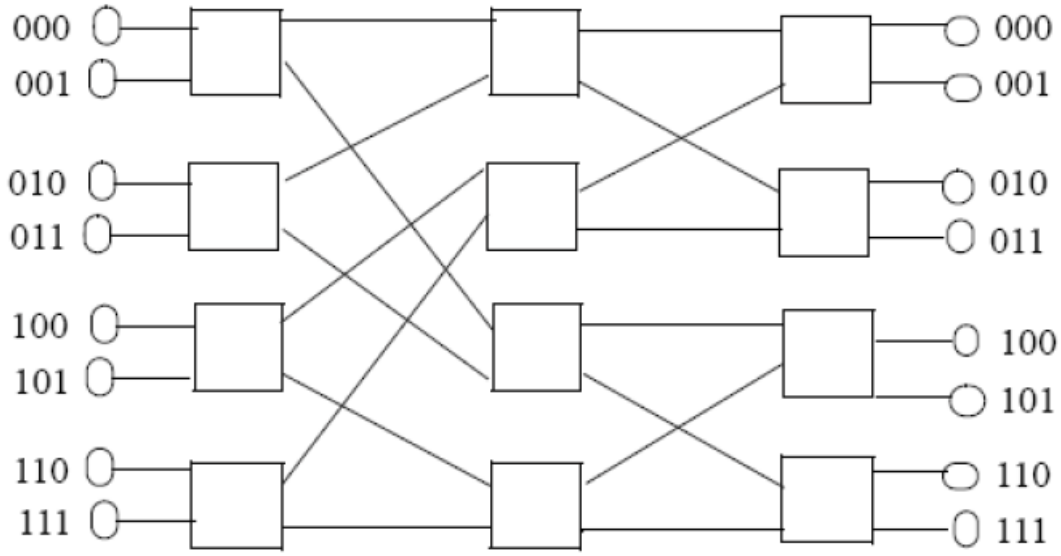
3) The following static network is shown –



Number of nodes -
Level 0 – 16
Level 1 – 4
Level 2 – 1
Total = 21 nodes.

Degree – Maximum = 7 Minimum = 3 {7, 3}
Diameter – 2 (there would be two hops required for pyramid interconnection with k = 4)

4) The interconnection shown –



Kind – It is a multistage interconnection network similar to Omega network
Routing – Destination based packet routing. The packets can be routed based on the destination of the packet starting from the most significant bit and choosing the lower link if the bit is 1 and upper link otherwise.
Blocking/non-blocking properties – It is a blocking network since a request from incoming port 000 to destination port 111 would be blocked if there is a request from source 011 to destination 110 as there is a single path only.
Inter-stage connection scheme – Stage 0 uses perfect shuffle exchange. Stage 1 uses a mix of upper and lower broadcast.
Clearly the network has three (3) stages.
The number of switches in the network are 12 with 8 nodes.

5)
i) Multirate Clos Networks – The paper in general talks about the Clos networks and how the discovery of such networks made by Charles Clos is still used in the modern day technology. The paper describes how Clos results have been generalized to systems that support connections with varying bandwidth requirements. Paper tries to present theories on the efforts made by the researchers to have a non-blocking multirate switching systems. The author initially describes the time-sharing switching systems and how Clos theory could be applied to make them non-blocking. From there author moves to a more advanced technique known as the Asynchronous transfer mode (ATM) which makes use of the virtual circuit identifier. The author also talks about the concept of wide-sense non-blocking network where blocking in the network can be avoided through judicious selection of routes. This lead to the research of a more sophisticated algorithm known as the Quota Scheme which basically implied that the large connections can use any of the middle-stage switch, while routing small connections only through a subset of them. But this added to the cost of the network and it was later realised that the benefits attained were quite less. In order to have a non-

blocking network a new technique was devised which is known as the rearrangeably non-blocking networks where a link from one input to output can be made by reconfiguring the network. The author also touches upon the problem of routing in multicast networks. Routes in multicast switches form trees rooted at the inputs from which they originate. As a result of this a non-blocking large multicast network is impractically expensive. The author also talks about the reroutably nonblocking multicast network where any existing connection can be extended if it can be rerouted. One approach mentioned in the paper is to cascade two clos networks, connecting the outputs of the first to the inputs of the second. The first network is used for routing purposes and the second one completes the multicast connections. The paper ends with the author highlighting some of the practical concerns with these approaches. The author describes the problem of deciding when a set of connections can be multiplexed together for higher benefits. The author also highlights the fact that the average rate (instead of the peak rate) should be chosen as the connection rate for practical reasons. The author finally concludes the paper talking about the cost of different configurations keeping in mind the cost of crosspoint counts for the non-blocking networks.

ii) Circuit design of Clos-based on-chip interconnection networks

The main focus of study in this paper is related to the high performance circuit design of multi-stage non-blocking networks other than the trivial crossbars networks. The paper provides a comprehensive study of different multi-stage interconnection networks like the Benes, Clos, crossbars and even does a comparison between these topologies. The main focus is on the practical usage of these topologies in a network on a chip system. Author initially presents a deep study of the work related to the design of crossbars and benes/clos networks. Most of the designs are Matrix/Mux based designs using the CMOS standard cell ASIC technology. Though one of the main factors which limit the research in this area is due to the fact that there is lack of appropriate wire models hence it's very inaccurate to conduct circuit level simulations for the design. The paper also talk about the non-blocking implementations of the above mentioned Benes/Clos network designs. These are mainly used in multicore systems to ensure coherency in the memory sub-system. The author tries to compare the different techniques based on transistor count, power and area of the network topology. Paper also details the design flow used in the circuit design of the Benes and Clos networks. It also presents the schematic and layout designs of the logic unit and gives details about the number of logic units and reconfigurable switches. The design was carried out using two approaches one used transmission gates and the other used NMOS based gates. The experimental results shows that the timing delay of the NMOS-based Benes network was about 10 times the delay as compared to the transmission gate based design. Though the area consumed by the transmission gates design was more as compared to the NMOS-based design. But the power consumptions of the NMOS based design was significantly more than the transmission based design. All the different design approaches and experimental study concluded that the transmission gate based design have much better timing and power performance than the NMOS based designs though the transistor count is a bit more for transmission based designs. These results also confirmed that the Clos network is a better alternative than Benes/crossbars in large scale networks. The author ends the paper giving some insights to the possible future work related to the network performance of Benes/Clos based designs under real-life applications.