MIPS64 Reference

Load/store instructions

LD, LW, LH, LB SD, SW, SH, SB L.S, L.D, S.S, S.D LWU, LHU, LBU

Arithmetic & logical

DADD, DADDI, DADDIU // 32-bit variants still supported (ADD, ADDI, ADDIU) DSUB, DSUBU SLT, SLTI, SLTU, SLTIU DMUL, DDIV, DDIVU

Shift & rotate

DSLL, DSLL32, DSLLV
DSRA, DSRA32, DSRAV
DSRL, DSRL32, DSRLV
DROTR, DROTR32, DROTRV

Branch & jump

J, JAL, JALR BEQ, BNE, BLT, BLE, BGT, BGE

Load a 64-bit immediate

LUI, AUI, DAHI, DATI

Floating-Point Compare

C.EQ.S, C.NE.S, C.LT.S, C.LE.S, C.GT.S, C.GE.S C.EQ.D, C.NE.D, C.LT.D, C.LE.D, C.GT.D, C.GE.D BC1T, BC1F

Floating-Point move between GPR and FPR

DMTC1, DMFC1

Integer/Floating-Point conversion

CVT.D.S, CVT.D.W, CVT.D.L CVT.S.D, CVT.S.W, CVT.S.L CVT.L.S, CVT.L.D CVT.W.S, CVT.W.D (W: 32-bit int) (L: 64-bit int) (S: 32-bit FP) (D: 64-bit FP)

Floating-point operations

ADD.S, ADD.D, ADD.PS

MUL.S, MUL.D, MUL.PS

MOV.S, MOV.D, MOV.PS

SUB.S, SUB.D, SUB.PS

DIV.S, DIV.D, DIV.PS

Pair of Singles (PS) support

CVT.PS.S F0, F1, F2 // Merge two SPs into one PS
PLL.PS F0, F1, F2 PLU.PS F0, F1, F2 // Merge two SP into one PS
PUL.PS F0, F1, F2 PUU.PS F0, F1, F2 // Merge two SP into one PS
CVT.S.PL F0, F1 // Extract a SP from a PS