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Design and Implementation of Low Power 16-Bit ALU using MGDI Technique

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Abstract: Rapid development in portable digital applications, demands for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts. The wish to improve the performance of logic circuits, once based on traditional CMOS technology, resulted in the development of many logic design techniques during the last two decades.MGDI (Modified Gate Diffusion Input) is a technique of low power digital combinational design; Compared to other currently used logic design styles, allows less power consumption and reduced propagation delay with minimum number of transistors.In this paper a 16 – bit Arithmetic Logic Unit using MGDI Technique is presentedand also compared with CMOS logic. The Arithmetic and Logical functions that are realized in ALU are Addition,Subtraction,Increment, Decrement operations, AND, OR, XOR, and XNOR. The simulation tool used is Tanner EDA 32 nm Technology.

Keywords: CMOS (Complementary Metal Oxide Semiconductor), ALU (Arithmetic Logical Unit), GDI (Gate Diffusion Input), MGDI (Modified Gate Diffusion Input).

I. INTRODUCTION

Very large scale integration (VLSI)technology has developed to the point where millions of transistor can be implemented on a single chip. Complementary metal Oxide semiconductor (CMOS) has been the backbone in mixed signal because it reduces powerand providing good mix component for analog and digital design. A processor is a main part of any digital system such that ALU (Arithmetic and Logic Unit) is a fundamental building block of the processor circuit which performs arithmetic and logical operations. The power consumed by the ALU has a direct impact in the power dissipated from the processor. Hence, therequired design is to implement the ALU in a fashion where the performance of the processor is improved and also with less power consumption. Improving the performance of circuits based on CMOS logic by the introduction of many logic styles like Pass Transistor logic, Transmission Gate logic, Double Pass Transistor logic and also many other hybrid logics. Improving the performance of circuits based on CMOS logic by the introduction of many logic styles like Pass Transistor logic, Transmission Gate logic, Double Pass Transistor logic and also many other hybrid logics, It has many advantages over CMOS i.e., high speed, low powerdissipation and lower interconnection effects. GDI Technique can overcome certain drawbacks of CMOS LogicA wide range of complex logic functions in which PTL was used, can be replaced by GDI Technique and this makes the circuit simple.

Easier design of fast, low power circuits with less number of transistors are enabled using GDI Technique.An Arithmetic Logic Unit with low power dissipation, lesser transistor count and lesser propagation delay can contribute much to the modern era.In this paper a 16 - bit ALU is designed using GDI Technique and its power dissipation and transistor count is compared with the CMOS logic. The sub blocks used are multiplexers, adders and gates. The basic logic gates AND, OR, XOR, XNOR and combinational circuits like half adder, full adder, multiplexer etc are designed and compared with the existing logic styles, CMOS and Transmission Gate , in terms of power dissipation and transistor count. The paper progresses as follows: Section 2 provides some background work on CMOS logics in general and Arithmetic logic unit. In the next, a proposedGDI is described in Section 3 and the next section, called section 4, Describes ALU using Modified GDI Technology and Its Architecture. In Section 5 the simulation results are shown and last of all this paper is concluded in section 6.

II. CMOS LOGIC TECHNOLOGY

One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation.This allows integrating many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance.

A. Components Design With Cmos Logic

The various components are designed using complementary metal oxide logic (CMOS logic) are Inverter, AND, OR, MUX etc are given below

1. CMOS Inverter

The basic CMOS Inverter as shown in the figure 1 below. When a low voltage (0 V) is applied at the input, the top transistor (P-type) is conducting (switch closed) while the bottom transistor behaves like an open circuit. Therefore, the supply voltage (5 V) appears at the output.

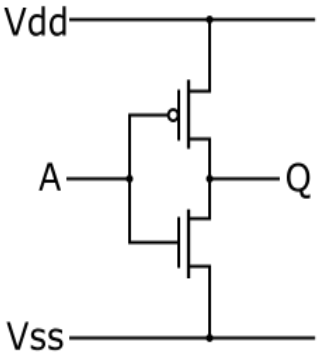


Fig 1. CMOS Inverter

Conversely, when a high voltage (5 V) is applied at the input, the bottom transistor (N-type) is conducting (switch closed) while the top transistor behaves like an open circuit.Hence, the output voltage is low (0 V). The output is the opposite of the input – this gate inverts the input.

2. CMOS AND Logic

Two PMOS gates are connected in parallel and two NMOS gates are connected in series such that these modules are connected together and in between these two modules we can take output as NAND by providing input to the NMOS and PMOS transistors and it will feed to normal inverter which can give results as AND Gate. The Basic CMOS AND gate is shown in figure below

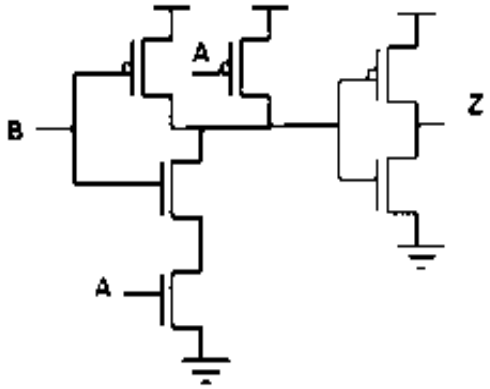


Fig 2. CMOS AND gate

3. CMOS OR Logic:

Two PMOS gates are connected in series and Two NMOS gates are connected in Parallel such that these modules are connected together and in between these two modules we can take output as NOR by providing input to the NMOS and PMOS transistors and it will feed to normal inverter which can give results as OR Gate.

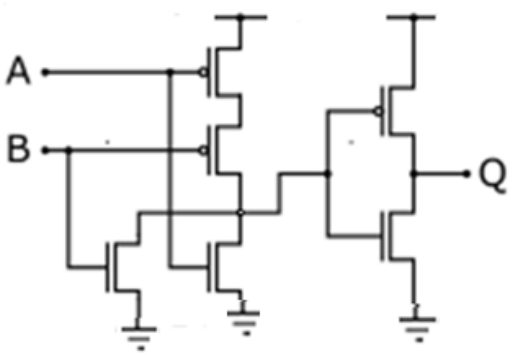


Fig 3. CMOS OR Gate

4. CMOS Mux Design

A multiplexer is used to select the input as output from many inputs based on the selection input In 2 to 1 MUX we have 2 inputs an one section line which is used to select the input to output. The cmos design of Multiplexer is given below

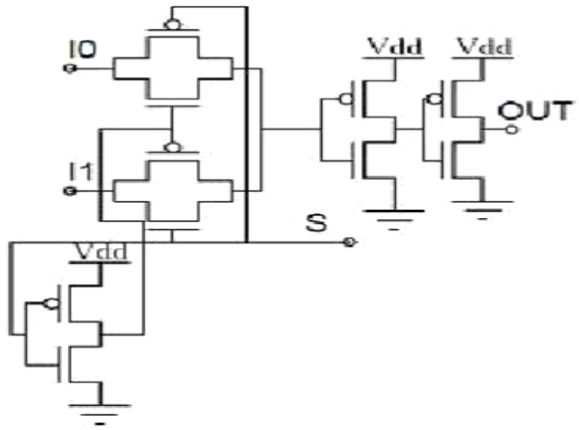


Fig 4. Basic CMOS MUX Design

B. CMOS Based Full Adder

The 1-bit full adder circuit is one of the most important components of any digital system applications. The power-delay product is a measurement of the energy expanded per operational cycle of an arithmetic circuit.

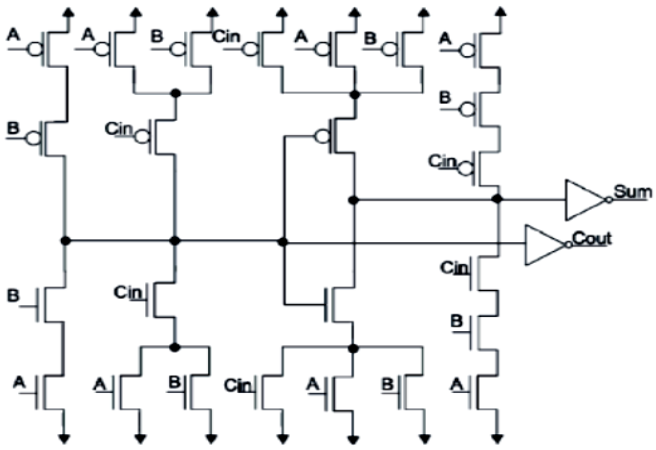


Fig 5. CMOS FULL ADDER

C. Arithmatic And Logic Unit (ALU)

The arithmetic logic unit (ALU) is the brain of the computer, the device that performs the arithmetic operations like addition and subtraction or logical operations like AND and OR. This section constructs an ALU from four hardware building blocks (AND and OR gates, inverters, and multiplexors) and illustrates how combinational logic works. In the next section, we will see how addition can be sped up through more clever designs.

1. 1 bit ALU

An arithmetic-logic unit (ALU) is the part of a ComputerProcessor (CPU) that carries out arithmetic and logic operations on the operands in Computer instruction wordsIn some processors, the ALU is divided into two units, an arithmetic unit (AU) and a logic unit (LU).The logical operations are easiest, because they map directly onto the hardware components in Figure below.

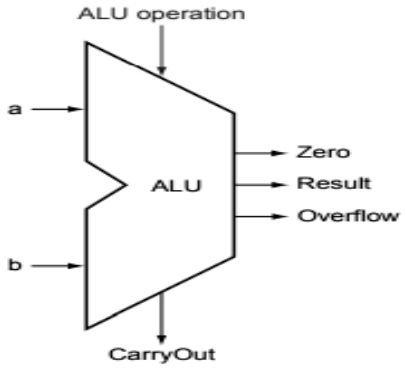


Fig 6. Symbol of ALU

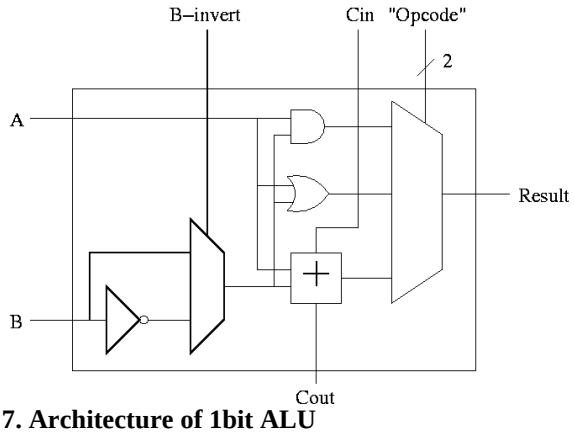


Fig 7. Architecture of 1bit ALU

ALU is a core part of computer or digital processor that executes arithmetic and logical operation, such as increment,decrement, addition and subtraction as an arithmetic operationAND, OR, XOR, XNOR as a logical operation. ALU isbuild by using FA and multiplexer.

III. EXISTING GDI TECHNOLOGY

The GDI cell is similar to a CMOS inverter structure. In a CMOS inverter the source of the PMOS is connected to VDD and the source of NMOS is grounded. But in a GDI cell this might not necessarily occur.There are some important differences between the two. The three inputs in GDI are namely

1. G- common inputs to the gate of NMOS and PMOS
2. N- input to the source/drain of NMOS
3. P- input to the source/drain of PMOS Bulks of both NMOS and PMOS are connected to N or P

Basic GDI cell is given below in figure 8

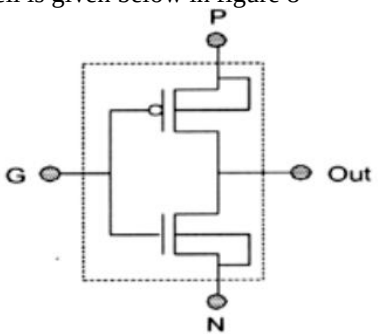


Fig 8. Basic GDI Cell

Table 1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6–12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method.

Table .1 Various Logic Functions Of GDI Cell for Different Input Configurations

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

The circuits required to design Arithmetic and Logic unit are

A. GDI Based Multiplexer:

Multiplexer will acts as a digital switch. Selection line plays a major role to select particular input. If the number of input lines is "2n" and selection lines will be "n"selectionlines. With the "n" selection line the particular "2n" input line will be selected. Figure 9 shows the implementation of 2x1 multiplexer.

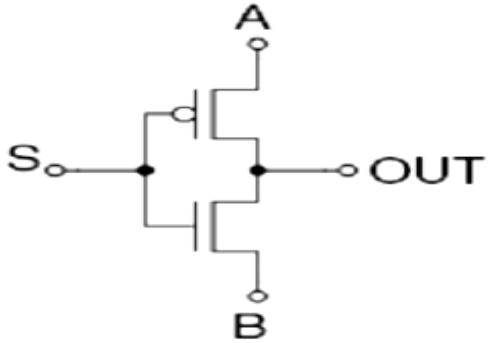


Fig 9. GDI Multiplexer

B. GDI Based XOR

XOR gate is the main building block of the full adder and also which gives the sum output of the full adder. The number of transistors taken to design the XOR gate is four.

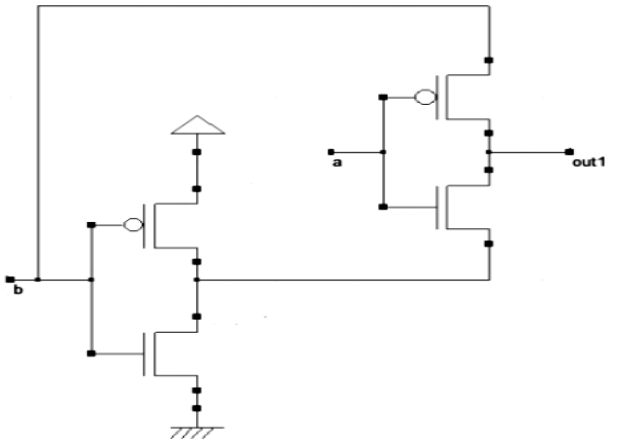


Fig 10. GDI based EXOR gate

C. GDI Based Full Adder

FA is basic functional module for designing ALU. 11T used for design of FA, this modern design of FA is minimize the power and reduced the delay. FA depicts in Fig. 11, circuit is operating at power supply (VDD) 0.9V. Inputs A apply to the gate terminal of PMOS_1 and NMOS_1, drain terminal of PMOS_2. Inputs B apply to the gate terminal of PMOS_2 and PMOS_2, drain terminal of NMOS_1. When source voltage (VS) is greater than threshold voltage (VTH) transistor is ON and pass the signal from gate terminal to drain terminal meanspass the gate voltage (VG) to drain terminal.

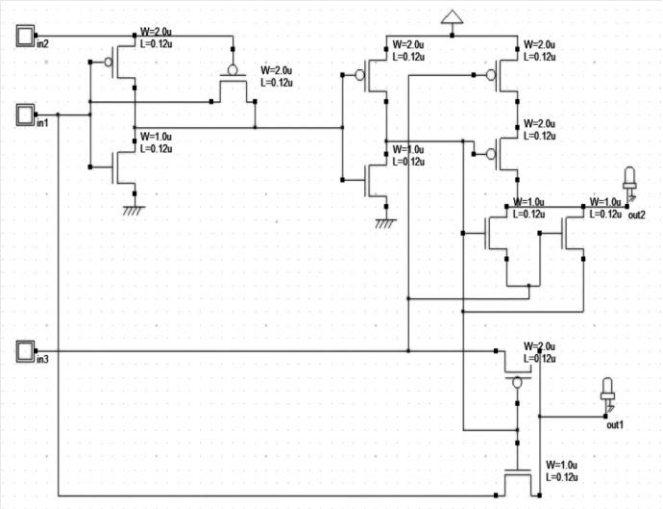


Fig 11. GDI Full Adder Using 11 T

IV. PROPOSED MODIFIED GDI TECHNOLOGY

This modified gate diffusion input (Mod-GDI) logic style allows reducing power consumption, delay and area of digital circuits. Fig below shows basic Mod-GDI cell. In contrast with basic GDI cell, Modified GDI cell contains

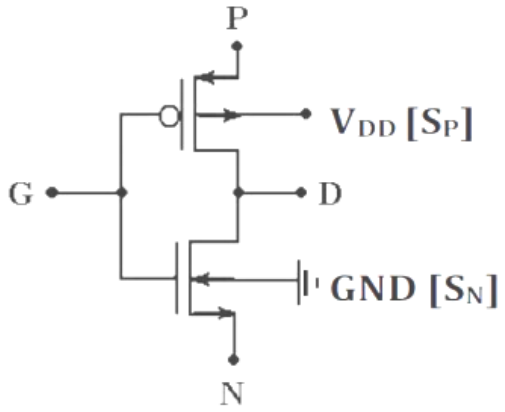


Fig 12. Modified GDI cell

A. MGDI Based XOR:

Conventional XOR gate can be fabricated using GDI logic needs more than 3 transistors. But here is new design of a XOR gate with 3 transistors as shown in figure 13 below,

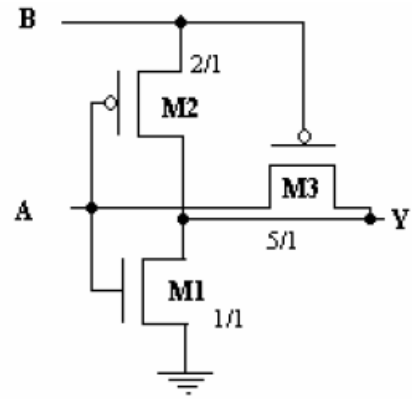


Fig 13. XOR with 3T

By using this 3 Transistor XOR we can minimize the no of transistors of a full adder.

B. MGDI Based FULL ADDER:

In the GDI Technology It requires 11 Transistors to design a full adder But in the MGDI we can design an XOR gate with 3 transistors instead of 4 so that we can able to design a Full Adder with minimum transistors (8) than GDI based Full adder

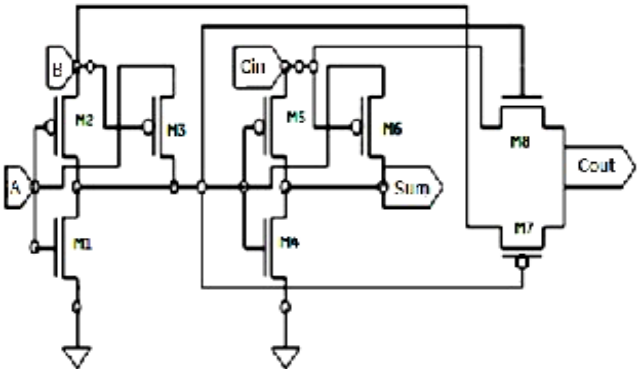


Fig 14. Full adder With 8 Transistors

C. 16 bit ALU using MGDI Technology

ALU is a core part of computer or digital processor that executes arithmetic and logical operation, such as increment, decrement, addition and subtraction as an arithmetic operation & AND, OR, XOR, XNOR as a logical operation. ALU is build by using FA and multiplexer.

Table 2 TRUTH TABLE OF ALU

S_2	S_1	S_0	OPERATION
0	0	0	OR
0	0	1	XNOR
0	1	0	XOR
0	1	1	AND
1	0	0	INCREMENT
1	0	1	ADDITION
1	1	0	DECREMENT
1	1	1	SUBTRACTION

FA is mainstays of ALU, 16-bit ALU is design using 16-bitripple carry adder (RCA). RCA is responsible for arithmeticoperation of ALU. Other modules needed for designing ALUare 2 is to 1 multiplexer and 4 is to 1 multiplexer. Logicaloperation executes by using multiplexer. Fig. 7 depicts the 1-bit ALU, 1 bit ALU design using one 4 is to 1 multiplexer and one2 is to 1 multiplexer and FA.

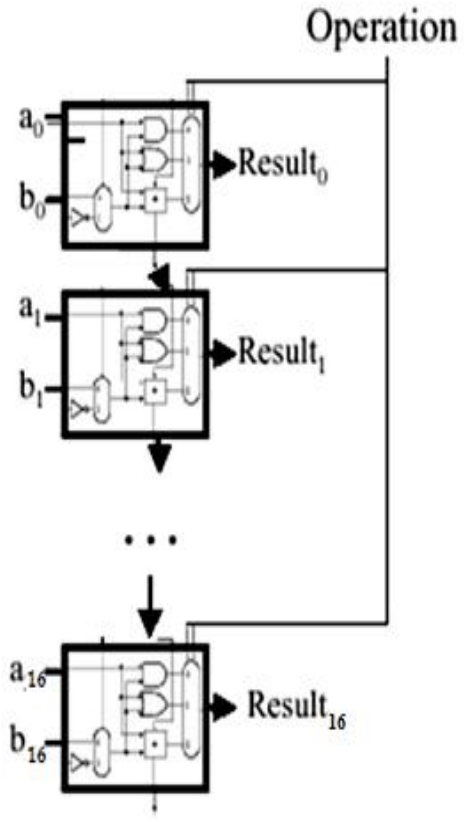
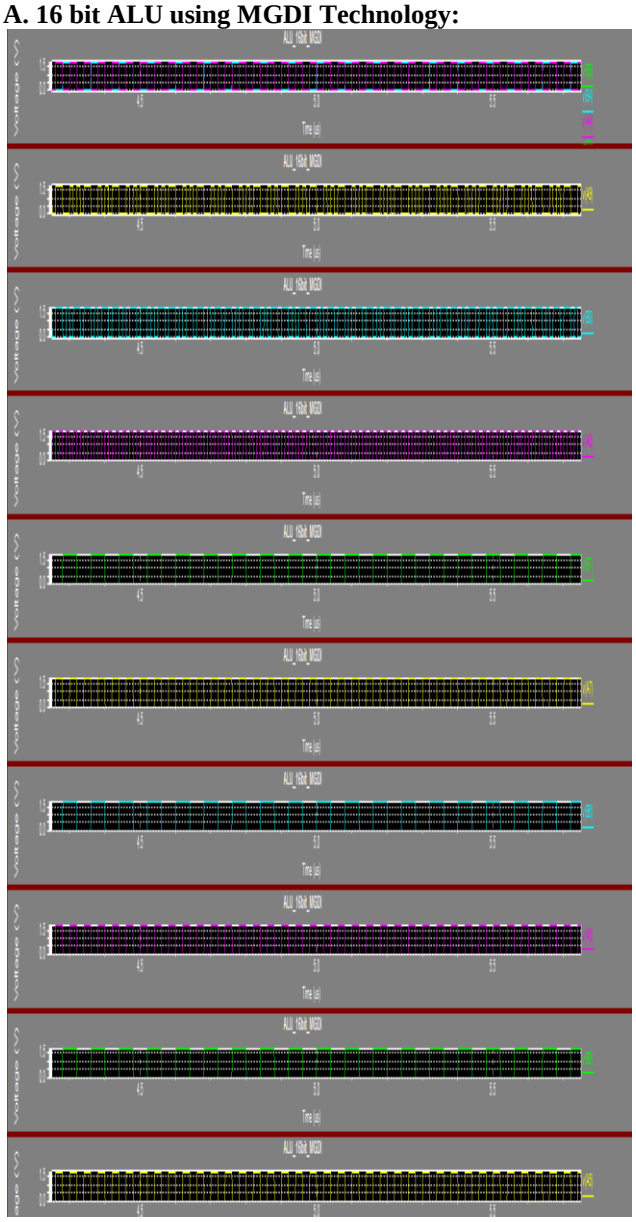


Fig 15. 16-bit ALU Design

V. SIMULATION RESULTS

A. 16 bit ALU using MGDI Technology:



B. DELAY:

```
tdelay = -9.0405e-009
   Trigger = 8.0722e-008
   Target  = 7.1682e-008
```

C. AREA:

```
Device and node counts:
            MOSFETs - 1200              MOSFET geometries - 10
               BJTs - 0                            JFETs - 0
            MESFETs - 0                            Diodes - 0
         Capacitors - 0                         Resistors - 0
          Inductors - 0                  Mutual inductors - 0
Transmission lines - 0        Coupled transmission lines - 0
   Voltage sources - 37                 Current sources - 0
               VCVS - 0                             VCCS - 0
               CCVS - 0                             CCCS - 0
  V-control switch - 0                 I-control switch - 0
     Macro devices - 0        External C model instances - 0
       HDL devices - 0
        Subcircuits - 0             Subcircuit instances - 320
 Independent nodes - 5376                 Boundary nodes - 38
       Total nodes - 5414
```

D. POWER:

```
Power Results
V0 from time 0 to 1e-005
Average power consumed -> 2.334785e-002 watts
Max power 5.950067e-002 at time 9.56003e-006
Min power 8.724368e-006 at time 8.95793e-006

V34 from time 0 to 1e-005
Average power consumed -> 7.134871e-002 watts
Max power 1.260565e-001 at time 4.011e-006
Min power 0.000000e+000 at time 0

V35 from time 0 to 1e-005
Average power consumed -> 7.174606e-003 watts
Max power 3.753088e-002 at time 5.88039e-006
Min power 0.000000e+000 at time 0

V36 from time 0 to 1e-005
Average power consumed -> 1.191443e-002 watts
Max power 2.954534e-002 at time 5.631e-006
Min power 0.000000e+000 at time 0
```

E. COMPARISON RESULTS:

Table 3. Results of different technologies with parameters

Parameter\Type	CMOS	GDI	MGDI
No. of Transistors	2752	1264	1200
Power (watts)	10.768	27.121	17.835
Delay (ns)	2.556	2.559	9.040

VI. CONCLUSION

MGDI (modified Gate diffusion input) is a technique of low power digital combinational design This technique as compare to other currently used logic design styles(GDI and CMOS technologies), allows less power consumption and reduced propagation delay with minimum number of transistors. In this paper presented with 16 – bit Arithmetic Logic Unit using modified Gate Diffusion Input (MGDI) Technique and also number of transistors is reduced than existing Systems.

VII. REFERENCES

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