 (+91) 9284502604

Divyesh Unadkat

Education

Ph.D. in Computer Science and Engineering (pursuing), 2015–Present
Indian Institute of Technology Bombay, Mumbai.
CPI: 9.48/10

B.E. in Computer Engineering, *Dharmsinh Desai University*, Nadiad. 2006–2010
Aggregate: 80.12 %

Experience

Researcher, *Tata Research Development and Design Centre*, Pune. **Jun'10–Present**

Intern, *Tata Research Development and Design Centre*, Pune. **Dec'09–Apr'10**

Technical Skills

Programming: C, C++, Java, Python, LaTeX

Compilers: LLVM, Clang, GNU tool chain (GCC, GDB, Make)

Research Tools: Z3, CBMC, Daikon, CPAChecker, InvGen

Development Tools: Emacs, Vim, Eclipse

Version Control: Git, CVS

Publications

[1] Supartik Chakraborty, Ashutosh Gupta, and Divyesh Unadkat. Diffy: Inductive reasoning of array programs using difference invariants. In *Proceedings of the 32nd International Conference on Computer-Aided Verification (CAV)*, pages 1320–1341, 2021.

[2] Mohammad Afzal, Supratik Chakraborty, Avriti Chauhan, Bharti Chimdyalwar, Priyanka Darke, Ashutosh Gupta, Shrawan Kumar, Charles Babu M, Divyesh Unadkat, and R. Venkatesh. Veriabs : Verification by abstraction and test generation (competition contribution). In *Proceedings of the 26th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, pages 383–387, 2020.

[3] Supartik Chakraborty, Ashutosh Gupta, and Divyesh Unadkat. Verifying array manipulating programs with full-program induction. In *Proceedings of the 26th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, pages 22–39, 2020.

[4] Supratik Chakraborty, Ashutosh Gupta, and Divyesh Unadkat. Verifying array manipulating programs by tiling. In *Proceedings of the 24th International Static Analysis Symposium (SAS)*, pages 428–449, 2017.

[5] Anand Yeolekar and Divyesh Unadkat. Assertion checking using dynamic inference. In *Proceedings of the 9th Haifa Verification Conference (HVC)*, pages 199–213, 2013.

[6] Anand Yeolekar, Divyesh Unadkat, Vivek Agarwal, Shrawan Kumar, and R Venkatesh. Scaling model checking for test generation using dynamic inference. In *Proceedings of the 6th International Conference on Software Testing, Verification and Validation (ICST)*, pages 184–191, 2013.

Presentations & Posters

Verifying Array Manipulating Programs with Full-Program Induction: 26th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), Online Presentation, March 2021.

Verifying Array Manipulating Programs with Full-Program Induction: Software Engineering Research India (SERI), (Online Presentation), **IIIT Hyderabad**, July 2020.

Technical Poster: Verifying Array Programs with Full-Program Induction: 4th Indian SAT+SMT School, **IIT Bombay**, December 2019

Executive Poster: Verifying Array Programs by Tiling: TCS Anvetion Workshop, **IITM Research Park, Chennai**, 2018

Verifying Array Manipulating Programs by Tiling: 24th International Static Analysis Symposium, SAS, **New York, USA**, August 2017.

Competition Talk: Verifying Array Manipulating Programs by Tiling: Research and Innovation Symposium in Computing, RISC, **IIT Bombay**, April 2017.

Competition Talk: Towards Precise Software Verification: Research and Innovation Symposium in Computing, RISC, **IIT Bombay**, April 2016.

Assertion Checking using Dynamic Inference: 9th Haifa Verification Conference, **Haifa, Israel**, November 2013.

Awards

Award: Best Verification Tool

Institution: International Software Verification Competition (SV-COMP)

Description: VERIABS stood first in the ReachSafety category at SV-COMP 2020. As a part of its team, I designed and developed an induction-based verification techniques for Arrays sub-category, and implemented them in tools VAJRA and TILER as well as integrated them with VERIABS [2].

Award: Most Admired Sprint Thesis Talk

Institution: Indian Institute of Technology Bombay, Mumbai

Description: Runner-up, Senior Researcher Sprint Talks, RISC 2017, IIT Bombay.

Award: Best Speaker in Sprint Thesis Talk

Institution: Indian Institute of Technology Bombay, Mumbai

Description: Winner, Early Researcher Sprint Talks, RISC 2016, IIT Bombay.

Award: Eklavya Gold Medal

Institution: Dharmsinh Desai University, Nadiad

Description: Highest aggregate marks in first four semesters, CE 2008, DDU Nadiad.

Contact

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Links

Webpage: https://divyeshunadkat.github.io/

dblp: http://dblp.uni-trier.de/pers/hd/u/Unadkat:Divyesh

LinkedIn: https://www.linkedin.com/in/divyeshunadkat/

GitHub: https://github.com/divyeshunadkat/