

EDUCATION	Ph.D. in ESE, University of Pennsylvania <i>Aug'16-Jul'18, Aug'21-Present</i> Advisor: Prof. André DeHon Research Interests: FPGA design methodology, Tools/CAD for FPGAs, Hardware Acceleration
	B.S. in ECE, Carnegie Mellon University <i>Aug'12-Dec'15</i> Recipient of David Tuma Project Award – Best ECE Capstone Project Award Graduated with University Honors
ACADEMIC RESEARCH	Software-like Incremental Refinement on FPGA [1] <i>Feb'23-Present</i> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> Proposed a fast incremental refinement strategy for FPGA designs that resembles SW compilation Designed a runtime bottleneck identification for HLS dataflow designs using FIFO full/empty counters Created a multi-clock system with a NoC (400MHz) and compute kernels (200–400MHz) Accelerated design tuning time by $1.3\text{--}2.7\times$ while improving application latency by $2.2\text{--}12.7\times$
	Network-on-a-Chip (NoC) on FPGA [2] <i>Sep'22-Jan'23</i> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> Designed a novel asymmetric Butterfly Fat Tree NoC in Verilog that excels in unbalanced traffic Analyzed throughput and worst case latency in realistic graph workloads and synthetic traffic patterns Achieved up to 76% more throughput than existing Butterfly Fat Tree NoC with the similar resource usage
	Parallel FPGA Compilation using Hierarchical Partial Reconfiguration [4] <i>Jan'22-Aug'22</i> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> Open-sourced the Makefile/Python/Tcl based FPGA's parallel compilation framework (link) Provided flexibility in sizes of compile slots for parallel FPGA compilations, utilizing Xilinx Nested DFX Only 2–5 min to compile realistic benchmarks, from HLS to bitstream ($2.2\text{--}5.3\times$ speedup over Xilinx Vitis)
	Accelerating FPGA Compilation using NoC and Partial Reconfiguration [6][7] <i>May'17-Aug'18</i> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> Designed packet parser, reassembly buffer, and FIFO modules in Verilog for the NoC interface Analyzed Xilinx Vivado's compile speed with case studies and revealed the limitations of the vendor tool Showed $4.5\times$ speedup in PnR time over Xilinx Vivado's compilation with a divide-and-conquer approach
	Detecting Voltage Anomalies in Scan-Testing Environment on FPGA <i>Dec'14-Oct'15</i> Advisor: Prof. Shawn Blanton, CMU <ul style="list-style-type: none"> Implemented a synthesizable, fine-grained voltage sensor on FPGA using carry chains and latches Analyzed voltage activities for three different ISCAS'89 circuits in at-speed scan testing environment
INDUSTRY EXPERIENCE	AMD, San Jose, CA, USA <i>(incoming) May'24-Aug'24</i> <i>(incoming) FPGA Architecture Intern</i>
	AnaPass, South Korea <i>Jul'20-Jul'21</i> <i>SoC Engineer (in fulfilment of military service)</i> <ul style="list-style-type: none"> RTL verification of Timing Controller IP for Samsung Tablet display
	Korea Advanced Institute of Science and Technology (KAIST), South Korea <i>Aug'18-Jul'20</i> <i>Research Engineer (in fulfilment of military service)</i> <ul style="list-style-type: none"> Projects on Radar-based fall detector, FPGA-based beamforming system, IQ imbalance calibration
	CoMira Solutions, Pittsburgh, PA, USA <i>Jun'14-Aug'14</i> <i>Hardware Engineering Intern</i> <ul style="list-style-type: none"> Optimized hardware implementation of CRC in area and timing using a table-based approach
	HW/SW co-design for VGG16, University of Pennsylvania <i>Nov'21-Dec'21</i> <ul style="list-style-type: none"> Designed a systolic array based FPGA acceleration kernel for 2D convolution function using HLS Integrated multiple FPGA kernels (on AWS EC2 F1) with PyTorch using C++ extension Demonstrated $11\text{--}14.8\times$ performance improvement over the SW baseline of 2D convolution (report link)

PUBLICATIONS	[1]	REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs D. Park , A. DeHon ACM Int. Symp. on Field-Programmable Gate Arrays (FPGA), 2024 – (acceptance rate: 22.5%)	
	[2]	Asymmetry in Butterfly Fat Tree FPGA NoC D. Park , Z. Yao, Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2023	
	[3]	ExHiPR: Extended High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, D. Park , Z. Niu, A. Hota, A. DeHon ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2023	
	[4]	Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration D. Park , Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2022 – (acceptance rate: 25.2%)	
	[5]	HiPR: High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, A. Hota, D. Park , A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2022 (<i>Best Paper Candidate</i> : 7.0%)	
	[6]	Reducing FPGA Compile Time with Separate Compilation for FPGA Building Blocks Y. Xiao, D. Park , A. Butt, H. Giesen, Z. Han, R. Ding, N. Magnezi, R. Rubin, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2019 – (acceptance rate: 25.0%)	
	[7]	Case for Fast FPGA Compilation using Partial Reconfiguration D. Park , Y. Xiao, N. Magnezi, A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2018	
TALKS	•	REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs – at AMD – FPGA Architecture team, San Jose, CA, USA (<i>slides</i>) – at Altera – FPGA Architecture team, San Jose, CA, USA (<i>slides</i>) – at FPGA 2024, Monterey, CA, USA (<i>talk video, slides</i>)	<i>Mar'24</i> <i>Mar'24</i> <i>Mar'24</i>
	•	Asymmetry in Butterfly Fat Tree FPGA NoC – at FPT 2023, Yokohama, Japan (virtual) (<i>talk video, slides</i>)	<i>Dec'23</i>
	•	Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration – at FPT 2022, Hong Kong (<i>talk video, slides</i>) – at ESE PhD seminar, University of Pennsylvania, Philadelphia, PA, USA (<i>slides</i>)	<i>Dec'22</i> <i>Oct'22</i>
	•	High-level Partial Reconfiguration for Fast Incremental FPGA Compilation – at FPL 2022, Belfast, Northern Ireland (<i>slides</i>)	<i>Aug'22</i>
	•	Case for Fast FPGA Compilation using Partial Reconfiguration – at FPL 2018, Dublin, Ireland (<i>slides</i>)	<i>Aug'18</i>
	•	Student Recognition Award, University of Pennsylvania	<i>Apr'23</i>
	•	Best Presentation Award, Penn ESE PhD seminar (F2022-S2023)	<i>Apr'23</i>
AWARDS/ SERVICE	•	Samsung Electronics Global Fellowship with post-graduation employment offer	<i>Oct'22</i>
	•	Best Paper Candidate , FPL2022	<i>Aug'22</i>
	•	PhD Fellowship, University of Pennsylvania	<i>Aug'16</i>
	•	Best ECE Capstone Project Award (Project: Neural Networks on FPGA), CMU	<i>May'16</i>
	•	University Honors, CMU	<i>May'16</i>
	•	Penn ESE PhD students seminar organizer	<i>Feb'23-Dec'23</i>
	•	Judge, Research Experience for Undergraduates, University of Pennsylvania	<i>Aug'23</i>
TEACHING ASSISTANT	•	SoC Architecture (ESE5320), University of Pennsylvania – Co-authored homework labs on multi-core, SIMD, HW acceleration, HLS, Xilinx Vitis – Held C/exam review sessions and weekly office hours for the graduate level course (20-40 students) – TA rating for Fall 2022: 3.74/4, the highest of all 7 offerings of the course's history	<i>Fall 2021, Fall 2022</i>
	•	Mathematical Foundations of Electrical Engineering (18-202), CMU	<i>Fall 2014</i>
	•	Structure and Design of Digital Systems (18-240), CMU	<i>Spring 2014</i>
	•	Hardware Verilog, Vivado, Vitis HLS, Quartus, HDL Simulation tools, OpenCL	
	•	Software C++, Python, PyTorch, scikit-learn, Tcl, Shell scripting	
SKILLS			