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EDUCATION	Ph.D. in ESE, University of Pennsylvania Advisor: Prof. André DeHon Research Interests: Tools for FPGAs, FPGA design methodology	<i>Aug'16-Jul'18, Aug'21-Present</i>	
	B.S. in ECE, Carnegie Mellon University Recipient of David Tuma Project Award – Best ECE Capstone Project Award Graduated with University Honors	<i>Aug'12-Dec'15</i>	
ACADEMIC RESEARCH	Software-like FPGA Development [1] <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> Fast incremental refinement for FPGA designs, iterating initial design points with parallel compilations Created a multiple-clock system with a NoC (400MHz) and compute kernels (200–400MHz) Designed a runtime bottleneck identification for HLS dataflow designs using FIFO full/empty counters Utilized ML-based classifiers to reduce resource fragmentation for separate FPGA compile technique Improved application latency 2.2–12.7× while Design Space Exploration time by 1.3–2.7× 	<i>Feb'23–Present</i>	
	Network-on-a-Chip (NoC) on FPGA [2] <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> Proposed a novel asymmetric Butterfly Fat Tree NoC in Verilog that excels in unbalanced traffic Analyzed throughput and worst case latency in realistic graph workloads and synthetic traffic patterns Achieved up to 76% more throughput than existing Butterfly Fat Tree NoC with the similar resource usage 	<i>Sep'22–Jan'23</i>	
	Parallel FPGA Compilation using Hierarchical Partial Reconfiguration [4] <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> Open-sourced the Makefile/Python/Tcl based FPGA's parallel compilation framework (link) Provided flexibility in sizes of compile slots for parallel FPGA compilations, utilizing Xilinx Nested DFX Demonstrated 1.4–4.9× latency improvement for realistic HLS applications over the previous work 	<i>Jan'22–Aug'22</i>	
	Accelerating FPGA Compilation using NoC and Partial Reconfiguration [6][7] <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> Designed packet parser, reassembly buffer, and FIFO modules for NoC interface in Verilog Analyzed Xilinx Vivado's compile speed with case studies and revealed the limitations of the vendor tool Demonstrated 4.5× compile time speedup for a multi-core design on FPGA over Xilinx Vivado 	<i>May'17–Aug'18</i>	
	Detecting Voltage Anomalies in Scan-Testing Environment on FPGA <i>Advisor: Prof. Shawn Blanton, Carnegie Mellon University</i> <ul style="list-style-type: none"> Implemented a synthesizable, fine-grained voltage sensor on FPGA using carry chains and latches Analyzed voltage activities for three different ISCAS'89 circuits in at-speed scan testing environment 	<i>Dec'14–Oct'15</i>	
INDUSTRY EXPERIENCE	AnaPass, South Korea <i>SoC Engineer</i> <ul style="list-style-type: none"> RTL verification of Timing Controller IP for Samsung Tablet display 	<i>Jul'20–Jul'21</i>	
	Korea Advanced Institute of Science and Technology (KAIST), South Korea <i>Research Engineer</i> <ul style="list-style-type: none"> Projects on Radar-based fall detector, FPGA-based beamforming system, IQ imbalance calibration 	<i>Aug'18–Jul'20</i>	
	CoMira Solutions, Pittsburgh, PA <i>Hardware Engineering Intern</i> <ul style="list-style-type: none"> Optimized hardware implementation of CRC in area and timing using a lookup table-based approach 	<i>Jun'14–Aug'14</i>	
COURSE PROJECTS	HW/SW co-design for VGG16, University of Pennsylvania <ul style="list-style-type: none"> Designed a systolic array based FPGA acceleration kernel for 2D convolution function using HLS Integrated multiple FPGA kernels (on AWS EC2 F1 instance) with PyTorch using C++ extension Achieved 11–14.8× performance improvement over the SW baseline of 2D convolution function (report link) 	<i>Nov'21–Dec'21</i>	

PUBLICATIONS	[1] REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs D. Park , A. DeHon ACM Int. Symp. on Field-Programmable Gate Arrays (FPGA), 2024 – <i>to appear</i>		
	[2] Asymmetry in Butterfly Fat Tree FPGA NoC D. Park , Z. Yao, Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2023		
	[3] ExHiPR: Extended High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, D. Park , Z. Niu, A. Hota , A. DeHon ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2023		
	[4] Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration D. Park , Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2022 (acceptance rate: 25.2% = 31/123), Artifact Evaluated - Available, Functional, Reusable, Replicated		
	[5] HiPR: High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, A. Hota, D. Park , A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2022 (Best Paper Candidate : 7.0% = 9/129)		
	[6] Reducing FPGA Compile Time with Separate Compilation for FPGA Building Blocks Y. Xiao, D. Park , A. Butt, H. Giesen, Z. Han, R. Ding, N. Magnezi, R. Rubin, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2019 (acceptance rate: 25.0% = 26/104)		
	[7] Case for Fast FPGA Compilation using Partial Reconfiguration D. Park , Y. Xiao, N. Magnezi, A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2018		
TALKS	<ul style="list-style-type: none"> • Asymmetry in Butterfly Fat Tree FPGA NoC – at FPT 2023, Yokohama, Japan (<i>talk video, slides</i>) Dec'23 • Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration – at FPT 2022, Hong Kong (<i>talk video, slides</i>) Dec'22 – at ESE PhD seminar, University of Pennsylvania, Philadelphia, PA (<i>slides</i>) Oct'22 • High-level Partial Reconfiguration for Fast Incremental FPGA Compilation – at FPL 2022, Belfast, Northern Ireland (<i>slides</i>) Aug'22 • Case for Fast FPGA Compilation using Partial Reconfiguration – at FPL 2018, Dublin, Ireland (<i>slides</i>) Aug'18 		
AWARDS/ SERVICE	<ul style="list-style-type: none"> • Student Recognition Award, University of Pennsylvania Apr'23 • Best Presentation Award, Penn ESE PhD seminar (F2022-S2023) Apr'23 • Samsung Electronics Global Fellowship with post-graduation employment offer Oct'22 • Best Paper Candidate, FPL2022 Aug'22 • PhD Fellowship, University of Pennsylvania Aug'16 • Best ECE Capstone Project Award (Project: NN on FPGA), Carnegie Mellon University May'16 • University Honors, Carnegie Mellon University May'16 • Penn ESE PhD students seminar organizer Feb'23-Dec'23 • Judge, Research Experience for Undergraduates, University of Pennsylvania Aug'23 		
TEACHING ASSISTANT	<ul style="list-style-type: none"> • SoC Architecture, University of Pennsylvania Fall 2021, Fall 2022 – Co-authored homework labs on multi-core, SIMD, HW acceleration, HLS, Xilinx Vitis – Held C/exam review sessions and weekly office hours for the graduate level course (20-40 students) – High TA rating for Fall 2022: 3.74/4, the best of all 7 offerings of the course's history • Mathematical Foundations of Electrical Engineering, Carnegie Mellon University Fall 2014 • Structure and Design of Digital Systems, Carnegie Mellon University Spring 2014 		
SKILLS	Hardware	Verilog, Vivado, Vitis HLS, Quartus, HDL Simulation tools (VCS, Verdi, iverilog), OpenCL	
	Software	C++, Python, PyTorch, scikit-learn, Tcl	
RELEVANT COURSES	Computer Architecture HW/SW Co-Design for ML	Computer Organization Advanced Computer Arch. (GPU)	SoC Architecture Big Data Analytics