Dongjoon(DJ) Park

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Education

Ph.D. in **ESE**, **University of Pennsylvania** *Aug'16–Jul'18, Aug'21–Dec'24(Expected)*
Advisor: Prof. André DeHon
Thesis: Software-like Incremental Refinement on FPGA using Partial Reconfiguration

B.S. in **ECE**, **Carnegie Mellon University** *Aug'12–Dec'15*
Recipient of David Tuma Project Award – Best ECE Capstone Project Award
Graduated with University Honors

Industry Experience

AMD, San Jose, CA, USA *May'24–Present*
FPGA Architecture Intern
- Explored divide-and-conquer strategy in FPGA implementation to achieve a high clock frequency (>450MHz) for SpMV accelerator that fully utilizes HBM bandwidth of modern datacenter FPGAs
- Identified the limitations of the current FPGA toolchain (Vivado) and FPGA architecture (Alveo U280)

AnaPass, South Korea *Jul'20–Jul'21*
SoC Engineer
- RTL verification of Timing Controller IP for Samsung Tablet display

Korea Advanced Institute of Science and Technology (KAIST), South Korea *Aug'18–Jul'20*
Research Engineer

CoMira Solutions, Pittsburgh, PA, USA *Jun'14–Aug'14*
Hardware Engineering Intern

Academic Research

Software-like Incremental Refinement on FPGA [1] *Feb'23–May'24*
Advisor: Prof. André DeHon, University of Pennsylvania
- Proposed a fast incremental refinement strategy for FPGA designs that resembles SW compilation
- Designed a runtime bottleneck identification for HLS dataflow designs using FIFO full/empty counters
- Created a multi-clock system with a NoC (400MHz) and compute kernels (200–400MHz)
- Accelerated design tuning time by 1.3–2.7× while improving application latency by 2.2–12.7×

Network-on-a-Chip (NoC) on FPGA [3] *Sep'22–Jan'23*
Advisor: Prof. André DeHon, University of Pennsylvania
- Designed a novel asymmetric Butterfly Fat Tree NoC in Verilog that excels in unbalanced traffic
- Analyzed throughput and worst case latency in realistic graph workloads and synthetic traffic patterns
- Achieved up to 76% more throughput than existing Butterfly Fat Tree NoC with the similar resource usage

Parallel FPGA Compilation using Hierarchical Partial Reconfiguration [4] *Jan'22–Aug'22*
Advisor: Prof. André DeHon, University of Pennsylvania
- Open-sourced the Makefile/Python/Tcl based FPGA's parallel compilation framework (*link*)
- Provided flexibility in sizes of compile slots for parallel FPGA compilations, utilizing Xilinx Nested DFX
- Only 2–5 min to compile realistic benchmarks, from HLS to bitstream (2.2–5.3× speedup over Xilinx Vitis)

Accelerating FPGA Compilation using NoC and Partial Reconfiguration [6][7] *May'17–Aug'18*
Advisor: Prof. André DeHon, University of Pennsylvania
- Designed packet parser, reassembly buffer, and FIFO modules in Verilog for the NoC interface
- Analyzed Xilinx Vivado's compile speed with case studies and revealed the limitations of the vendor tool
- Showed 4.5× speedup in PnR time over Xilinx Vivado's compilation with a divide-and-conquer approach

Detecting Voltage Anomalies in Scan-Testing Environment on FPGA *Dec'14–Oct'15*
Advisor: Prof. Shawn Blanton, CMU
- Implemented a synthesizable, fine-grained voltage sensor on FPGA using carry chains and latches
- Analyzed voltage activities for three different ISCAS'89 circuits in at-speed scan testing environment

Course Projects

HW/SW co-design for VGG16, University of Pennsylvania *Nov'21–Dec'21*
- Designed a systolic array based FPGA acceleration kernel for 2D convolution function using HLS
- Demonstrated 11–14.8× performance improvement over the SW baseline of 2D convolution (*report link*)

Publications

[1] REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs
D. Park, A. DeHon
ACM Int. Symp. on Field-Programmable Gate Arrays (**FPGA**), 2024 – (acceptance rate: 22.5%)

[2] ExHiPR: Extended High-level Partial Reconfiguration for Fast Incremental FPGA Compilation
Y. Xiao, **D. Park**, Z. Niu, A. Hota , A. DeHon
ACM Transactions on Reconfigurable Technology and Systems (**TRETS**), 2024

[3] Asymmetry in Butterfly Fat Tree FPGA NoC
D. Park, Z. Yao, Y. Xiao, A. DeHon
IEEE Int. Conf. on Field-Programmable Technology (**FPT**), 2023

[4] Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration
D. Park, Y. Xiao, A. DeHon
IEEE Int. Conf. on Field-Programmable Technology (**FPT**), 2022 – (acceptance rate: 25.2%)

[5] HiPR: High-level Partial Reconfiguration for Fast Incremental FPGA Compilation
Y. Xiao, A. Hota, **D. Park**, A. DeHon
IEEE Int. Conf. on Field-Programmable Logic and Applications (**FPL**), 2022
(***Best Paper Candidate***: 7.0%)

[6] Reducing FPGA Compile Time with Separate Compilation for FPGA Building Blocks
Y. Xiao, **D. Park**, A. Butt, H. Giesen, Z. Han, R. Ding, N. Magnezi, R. Rubin, A. DeHon
IEEE Int. Conf. on Field-Programmable Technology (**FPT**), 2019 – (acceptance rate: 25.0%)

[7] Case for Fast FPGA Compilation using Partial Reconfiguration
D. Park, Y. Xiao, N. Magnezi, A. DeHon
IEEE Int. Conf. on Field-Programmable Logic and Applications (**FPL**), 2018

Talks

- **REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs**
  - at AMD – FPGA Architecture team, San Jose, CA, USA (*slides*) *Mar'24*
  - at Altera – FPGA Architecture team, San Jose, CA, USA (*slides*) *Mar'24*
  - at FPGA 2024, Monterey, CA, USA (*talk video*, *slides*) *Mar'24*
- **Asymmetry in Butterfly Fat Tree FPGA NoC**
  - at FPT 2023, Yokohama, Japan (virtual) (*talk video*, *slides*) *Dec'23*
- **Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration**
  - at FPT 2022, Hong Kong (*talk video*, *slides*) *Dec'22*
  - at ESE PhD seminar, University of Pennsylvania, Philadelphia, PA, USA (*slides*) *Oct'22*
- **High-level Partial Reconfiguration for Fast Incremental FPGA Compilation**
  - at FPL 2022, Belfast, Northern Ireland (*slides*) *Aug'22*
- **Case for Fast FPGA Compilation using Partial Reconfiguration**
  - at FPL 2018, Dublin, Ireland (*slides*) *Aug'18*

Awards/ Service

- AKF Scholarship (1st place), KSEA – Andrew Kim Memorial Foundation (*slides*) *Apr'24*
- Student Recognition Award, University of Pennsylvania *Apr'23*
- Best Presentation Award, Penn ESE PhD seminar (F2022–S2023) *Apr'23*
- **Samsung Electronics Global Fellowship** with post-graduation employment offer *Oct'22*
- **Best Paper Candidate**, FPL2022 *Aug'22*
- PhD Fellowship, University of Pennsylvania *Aug'16*
- **Best ECE Capstone Project Award** (Project: Neural Networks on FPGA), CMU *May'16*
- University Honors, CMU *May'16*
- Artifact Evaluation Committee for FCCM 2024
- Penn ESE PhD students seminar organizer *Feb'23–Dec'23*
- Judge, Research Experience for Undergraduates, University of Pennsylvania *Aug'23*

Teaching Assistant

- **SoC Architecture** (ESE5320), University of Pennsylvania *Fall 2021*, *Fall 2022*
  - Co-authored homework labs on multi-core, SIMD, HW acceleration, HLS, AMD Vitis
  - Held C/exam review sessions and weekly office hours for the graduate level course (20–40 students)
- **Mathematical Foundations of Electrical Engineering** (18-202), CMU *Fall 2014*
- **Structure and Design of Digital Systems** (18-240), CMU *Spring 2014*

Skills

Hardware Verilog, Vivado, Vitis HLS, Quartus, HDL Simulation tools, OpenCL
Software C++, Python, PyTorch, scikit-learn, Tcl, Shell scripting