

EDUCATION	<b>Ph.D. in ESE, University of Pennsylvania</b> <span style="float: right;"><i>Aug'16-Jul'18, Aug'21-Present</i></span> Advisor: Prof. André DeHon Research Interests: Tools for FPGAs, FPGA design methodology
	<b>B.S. in ECE, Carnegie Mellon University</b> <span style="float: right;"><i>Aug'12-Dec'15</i></span> Recipient of David Tuma Project Award – Best ECE Capstone Project Award Graduated with University Honors
ACADEMIC RESEARCH	<b>Software-like FPGA Development [1]</b> <span style="float: right;"><i>Feb'23-Present</i></span> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Novel incremental refinement for FPGA designs, iterating initial design points with separate compilations</li> <li>Created a multiple-clock system with a NoC (400MHz) and compute kernels (200–400MHz)</li> <li>Designed a runtime bottleneck identification for HLS dataflow designs using FIFO full/empty counters</li> <li>Utilized ML-based classifiers to reduce resource fragmentation for separate FPGA compile technique</li> <li>Showed 1.3–2.7× speedup in Design Space Exploration time and 2.2–12.7× in application latency</li> </ul>
	<b>Network-on-a-Chip (NoC) on FPGA [2]</b> <span style="float: right;"><i>Sep'22-Jan'23</i></span> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Designed a novel asymmetric Butterfly Fat Tree NoC in Verilog that excels in unbalanced traffic</li> <li>Demonstrated up to 32% and 76% throughput benefit in realistic workloads and synthetic traffic patterns</li> </ul>
	<b>Parallel FPGA Compilation using Hierarchical Partial Reconfiguration [4]</b> <span style="float: right;"><i>Jan'22-Aug'22</i></span> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Open-sourced the Makefile/Python/Tcl based FPGA's parallel compilation framework (<a href="#">link</a>)</li> <li>Utilized Xilinx Nested DFX to support flexible-sized slots for parallel FPGA compilations</li> <li>Demonstrated 1.4–4.9× latency improvement for realistic HLS applications over the previous work</li> </ul>
	<b>Accelerating FPGA Compilation using Partial Reconfiguration [6][7]</b> <span style="float: right;"><i>May'17-Aug'18</i></span> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Designed packet parser, reassembly buffer, and FIFO modules for NoC interface in Verilog</li> <li>Analyzed Xilinx Vivado's compile speed with case studies to optimize separate FPGA compile strategy</li> <li>Demonstrated 4.5× compile time speedup for a multi-core design on FPGA over Xilinx Vivado</li> </ul>
	<b>Detecting Voltage Anomalies in Scan-Testing Environment on FPGA</b> <span style="float: right;"><i>Dec'14-Oct'15</i></span> <i>Advisor: Prof. Shawn Blanton, Carnegie Mellon University</i> <ul style="list-style-type: none"> <li>Implemented synthesizable voltage sensors on FPGA using carry chains and latches</li> <li>Analyzed voltage activities for different sizes of ISCAS circuits in at-speed scan testing environment</li> </ul>
INDUSTRY EXPERIENCE	<b>AnaPass, South Korea</b> <span style="float: right;"><i>Jul'20-Jul'21</i></span> <i>SoC Engineer</i> <ul style="list-style-type: none"> <li>RTL verification of Timing Controller IP for Samsung Tablet display</li> </ul>
	<b>Korea Advanced Institute of Science and Technology (KAIST), South Korea</b> <span style="float: right;"><i>Aug'18-Jul'20</i></span> <i>Research Engineer</i> <ul style="list-style-type: none"> <li>Projects on Radar-based fall detector, FPGA-based beamforming system, IQ imbalance calibration</li> </ul>
	<b>CoMira Solutions, Pittsburgh, PA</b> <span style="float: right;"><i>Jun'14-Aug'14</i></span> <i>Hardware Engineering Intern</i>
COURSE PROJECTS	<b>HW/SW co-design for VGG16, University of Pennsylvania</b> <span style="float: right;"><i>Nov'21-Dec'21</i></span> <ul style="list-style-type: none"> <li>Designed a systolic array based FPGA kernel for 2D convolution function using HLS</li> <li>Integrated multiple FPGA kernels (on AWS EC2 F1 instance) with PyTorch using C++ extension</li> <li>Achieved 11–14.8× performance improvement over the SW baseline of 2D convolution function (<a href="#">report link</a>)</li> </ul>

PUBLICATIONS	[1]	REFINE: Runtime Execution Feedback for Incremental Evolution on FPGA Designs <u>D. Park</u> , A. DeHon ACM Int. Symp. on Field-Programmable Gate Arrays (FPGA), 2024 – <i>to appear</i>		
	[2]	Asymmetry in Butterfly Fat Tree FPGA NoC <u>D. Park</u> , Z. Yao, Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2023		
	[3]	ExHiPR: Extended High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, <u>D. Park</u> , Z. Niu, A. Hota , A. DeHon ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2023		
	[4]	Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration <u>D. Park</u> , Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2022 (acceptance rate: 25.2% = 31/123), Artifact Evaluated - Available, Functional, Reusable, Replicated		
	[5]	HiPR: High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, A. Hota, <u>D. Park</u> , A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2022 ( <i>Best Paper Candidate</i> : 7.0% = 9/129)		
	[6]	Reducing FPGA Compile Time with Separate Compilation for FPGA Building Blocks Y. Xiao, <u>D. Park</u> , A. Butt, H. Giesen, Z. Han, R. Ding, N. Magnezi, R. Rubin, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2019 (acceptance rate: 25.0% = 26/104)		
	[7]	Case for Fast FPGA Compilation using Partial Reconfiguration <u>D. Park</u> , Y. Xiao, N. Magnezi, A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2018		
TALKS		<ul style="list-style-type: none"><li>• <b>Asymmetry in Butterfly Fat Tree FPGA NoC</b> – at FPT 2023, Yokohama, Japan (<i>talk video, slides</i>)</li><li>• <b>Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration</b> – at FPT 2022, Hong Kong (<i>talk video, slides</i>) – at ESE PhD seminar, University of Pennsylvania, Philadelphia, PA (<i>slides</i>)</li><li>• <b>High-level Partial Reconfiguration for Fast Incremental FPGA Compilation</b> – at FPL 2022, Belfast, Northern Ireland (<i>slides</i>)</li><li>• <b>Case for Fast FPGA Compilation using Partial Reconfiguration</b> – at FPL 2018, Dublin, Ireland (<i>slides</i>)</li></ul>	<i>Dec'23</i> <i>Dec'22</i> <i>Oct'22</i> <i>Aug'22</i> <i>Aug'18</i>	
AWARDS/ SERVICE		<ul style="list-style-type: none"><li>• Student Recognition Award, University of Pennsylvania</li><li>• Best Presentation Award, Penn ESE PhD seminar (F2022-S2023)</li><li>• <b>Samsung Electronics Global Fellowship</b> with post-graduation employment offer</li><li>• <b>Best Paper Candidate</b>, FPL2022</li><li>• PhD Fellowship, University of Pennsylvania</li><li>• <b>Best ECE Capstone Project Award</b> (Project: NN on FPGA), Carnegie Mellon University</li><li>• University Honors, Carnegie Mellon University</li><li>• Penn ESE PhD students seminar organizer</li><li>• Judge, Research Experience for Undergraduates, University of Pennsylvania</li></ul>	<i>Apr'23</i> <i>Apr'23</i> <i>Oct'22</i> <i>Aug'22</i> <i>Aug'16</i> <i>May'16</i> <i>May'16</i> <i>Feb'23-Dec'23</i> <i>Aug'23</i>	
TEACHING ASSISTANT		<ul style="list-style-type: none"><li>• <b>SoC Architecture</b>, University of Pennsylvania – Co-authored homework labs on multi-core, SIMD, HW acceleration, HLS, Xilinx Vitis – Held C/exam review sessions and weekly office hours for the graduate level course (20-40 students) – High TA rating for Fall 2022: 3.74/4, the best of all 7 offerings of the course's history</li><li>• <b>Structure and Design of Digital Systems</b>, Carnegie Mellon University</li></ul>	<i>Fall 2021, Fall 2022</i> <i>Spring 2014</i>	
SKILLS		<b>Hardware</b> Verilog, Xilinx FPGA (Vivado, Vitis HLS), Intel FPGA (Quartus), OpenCL <b>Software</b> C++, Python, PyTorch, scikit-learn, Tcl		
RELEVANT COURSES		Computer Architecture HW/SW Co-Design for ML	Computer Organization Advanced Computer Arch. SoC Architecture Big Data Analytics	