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EDUCATION	<b>Ph.D. in ESE, University of Pennsylvania</b> Advisor: Prof. André DeHon Thesis: Software-like Incremental Refinement on FPGA using Partial Reconfiguration			<i>Aug'16-Jul'18, Aug'21-Dec'24(Expected)</i>
	<b>B.S. in ECE, Carnegie Mellon University</b> Recipient of David Tuma Project Award – Best ECE Capstone Project Award Graduated with University Honors			<i>Aug'12-Dec'15</i>
INDUSTRY	<b>AMD</b> , San Jose, CA, USA			<i>May'24-Present</i>
EXPERIENCE	<b>FPGA Architecture Intern</b> <ul style="list-style-type: none"> <li>Currently exploring optimizations of SpMV accelerator to fully utilize HBM bandwidth of modern FPGAs</li> </ul>			
	<b>AnaPass</b> , South Korea <i>SoC Engineer (in fulfilment of military service)</i> <ul style="list-style-type: none"> <li>RTL verification of Timing Controller IP for Samsung Tablet display</li> </ul>			<i>Jul'20-Jul'21</i>
	<b>Korea Advanced Institute of Science and Technology (KAIST)</b> , South Korea <i>Research Engineer (in fulfilment of military service)</i> <ul style="list-style-type: none"> <li>Projects on Radar-based fall detector and FPGA-based beamforming system</li> </ul>			<i>Aug'18-Jul'20</i>
	<b>CoMira Solutions</b> , Pittsburgh, PA, USA <i>Hardware Engineering Intern</i>			<i>Jun'14-Aug'14</i>
ACADEMIC RESEARCH	<b>Software-like Incremental Refinement on FPGA [1]</b> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Proposed a fast incremental refinement strategy for FPGA designs that resembles SW compilation</li> <li>Designed a runtime bottleneck identification for HLS dataflow designs using FIFO full/empty counters</li> <li>Created a multi-clock system with a NoC (400MHz) and compute kernels (200–400MHz)</li> <li>Accelerated design tuning time by 1.3–2.7× while improving application latency by 2.2–12.7×</li> </ul>			<i>Feb'23-May'24</i>
	<b>Network-on-a-Chip (NoC) on FPGA [3]</b> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Designed a novel asymmetric Butterfly Fat Tree NoC in Verilog that excels in unbalanced traffic</li> <li>Analyzed throughput and worst case latency in realistic graph workloads and synthetic traffic patterns</li> <li>Achieved up to 76% more throughput than existing Butterfly Fat Tree NoC with the similar resource usage</li> </ul>			<i>Sep'22-Jan'23</i>
	<b>Parallel FPGA Compilation using Hierarchical Partial Reconfiguration [4]</b> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Open-sourced the Makefile/Python/Tcl based FPGA's parallel compilation framework (<a href="#">link</a>)</li> <li>Provided flexibility in sizes of compile slots for parallel FPGA compilations, utilizing Xilinx Nested DFX</li> <li>Only 2–5 min to compile realistic benchmarks, from HLS to bitstream (2.2–5.3× speedup over Xilinx Vitis)</li> </ul>			<i>Jan'22-Aug'22</i>
	<b>Accelerating FPGA Compilation using NoC and Partial Reconfiguration [6][7]</b> <i>Advisor: Prof. André DeHon, University of Pennsylvania</i> <ul style="list-style-type: none"> <li>Designed packet parser, reassembly buffer, and FIFO modules in Verilog for the NoC interface</li> <li>Analyzed Xilinx Vivado's compile speed with case studies and revealed the limitations of the vendor tool</li> <li>Showed 4.5× speedup in PnR time over Xilinx Vivado's compilation with a divide-and-conquer approach</li> </ul>			<i>May'17-Aug'18</i>
	<b>Detecting Voltage Anomalies in Scan-Testing Environment on FPGA</b> <i>Advisor: Prof. Shawn Blanton, CMU</i> <ul style="list-style-type: none"> <li>Implemented a synthesizable, fine-grained voltage sensor on FPGA using carry chains and latches</li> <li>Analyzed voltage activities for three different ISCAS'89 circuits in at-speed scan testing environment</li> </ul>			<i>Dec'14-Oct'15</i>
	<b>HW/SW co-design for VGG16</b> , University of Pennsylvania <ul style="list-style-type: none"> <li>Designed a systolic array based FPGA acceleration kernel for 2D convolution function using HLS</li> <li>Integrated multiple FPGA kernels (on AWS EC2 F1) with PyTorch using C++ extension</li> <li>Demonstrated 11–14.8× performance improvement over the SW baseline of 2D convolution (<a href="#">report link</a>)</li> </ul>			<i>Nov'21-Dec'21</i>
COURSE PROJECTS				

PUBLICATIONS	[1]	REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs <b>D. Park</b> , A. DeHon ACM Int. Symp. on Field-Programmable Gate Arrays ( <b>FPGA</b> ), 2024 – (acceptance rate: 22.5%)	
	[2]	ExHiPR: Extended High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, <b>D. Park</b> , Z. Niu, A. Hota , A. DeHon ACM Transactions on Reconfigurable Technology and Systems ( <b>TRETS</b> ), 2024	
	[3]	Asymmetry in Butterfly Fat Tree FPGA NoC <b>D. Park</b> , Z. Yao, Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology ( <b>FPT</b> ), 2023	
	[4]	Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration <b>D. Park</b> , Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology ( <b>FPT</b> ), 2022 – (acceptance rate: 25.2%)	
	[5]	HiPR: High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, A. Hota, <b>D. Park</b> , A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications ( <b>FPL</b> ), 2022 ( <i>Best Paper Candidate</i> : 7.0%)	
	[6]	Reducing FPGA Compile Time with Separate Compilation for FPGA Building Blocks Y. Xiao, <b>D. Park</b> , A. Butt, H. Giesen, Z. Han, R. Ding, N. Magnezi, R. Rubin, A. DeHon IEEE Int. Conf. on Field-Programmable Technology ( <b>FPT</b> ), 2019 – (acceptance rate: 25.0%)	
	[7]	Case for Fast FPGA Compilation using Partial Reconfiguration <b>D. Park</b> , Y. Xiao, N. Magnezi, A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications ( <b>FPL</b> ), 2018	
TALKS	•	<b>REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs</b> – at AMD – FPGA Architecture team, San Jose, CA, USA ( <i>slides</i> ) <span style="float:right">Mar’24</span> – at Altera – FPGA Architecture team, San Jose, CA, USA ( <i>slides</i> ) <span style="float:right">Mar’24</span> – at FPGA 2024, Monterey, CA, USA ( <i>talk video, slides</i> ) <span style="float:right">Mar’24</span>	
	•	<b>Asymmetry in Butterfly Fat Tree FPGA NoC</b> – at FPT 2023, Yokohama, Japan (virtual) ( <i>talk video, slides</i> ) <span style="float:right">Dec’23</span>	
	•	<b>Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration</b> – at FPT 2022, Hong Kong ( <i>talk video, slides</i> ) <span style="float:right">Dec’22</span> – at ESE PhD seminar, University of Pennsylvania, Philadelphia, PA, USA ( <i>slides</i> ) <span style="float:right">Oct’22</span>	
	•	<b>High-level Partial Reconfiguration for Fast Incremental FPGA Compilation</b> – at FPL 2022, Belfast, Northern Ireland ( <i>slides</i> ) <span style="float:right">Aug’22</span>	
	•	<b>Case for Fast FPGA Compilation using Partial Reconfiguration</b> – at FPL 2018, Dublin, Ireland ( <i>slides</i> ) <span style="float:right">Aug’18</span>	
AWARDS/ SERVICE	•	AKF Scholarship (1st place), KSEA – Andrew Kim Memorial Foundation ( <i>slides</i> ) <span style="float:right">Apr’24</span>	
	•	Student Recognition Award, University of Pennsylvania <span style="float:right">Apr’23</span>	
	•	Best Presentation Award, Penn ESE PhD seminar (F2022–S2023) <span style="float:right">Apr’23</span>	
	•	<b>Samsung Electronics Global Fellowship</b> with post-graduation employment offer <span style="float:right">Oct’22</span>	
	•	<b>Best Paper Candidate</b> , FPL2022 <span style="float:right">Aug’22</span>	
	•	PhD Fellowship, University of Pennsylvania <span style="float:right">Aug’16</span>	
	•	<b>Best ECE Capstone Project Award</b> (Project: Neural Networks on FPGA), CMU <span style="float:right">May’16</span>	
	•	University Honors, CMU <span style="float:right">May’16</span>	
	•	Artifact Evaluation Committee for FCCM 2024	
	•	Penn ESE PhD students seminar organizer <span style="float:right">Feb’23–Dec’23</span>	
	•	Judge, Research Experience for Undergraduates, University of Pennsylvania <span style="float:right">Aug’23</span>	
TEACHING ASSISTANT	•	<b>SoC Architecture</b> (ESE5320), University of Pennsylvania <span style="float:right">Fall 2021, Fall 2022</span> – Co-authored homework labs on multi-core, SIMD, HW acceleration, HLS, AMD Vitis – Held C/exam review sessions and weekly office hours for the graduate level course (20–40 students)	
	•	<b>Mathematical Foundations of Electrical Engineering</b> (18-202), CMU <span style="float:right">Fall 2014</span>	
	•	<b>Structure and Design of Digital Systems</b> (18-240), CMU <span style="float:right">Spring 2014</span>	
SKILLS	<b>Hardware</b>	Verilog, Vivado, Vitis HLS, Quartus, HDL Simulation tools, OpenCL	
	<b>Software</b>	C++, Python, PyTorch, scikit-learn, Tcl, Shell scripting	