

EDUCATION	<b>Ph.D. in ESE, University of Pennsylvania</b> <span style="float: right;"><i>Aug'16-Jul'18, Aug'21-Present</i></span> Advisor: Prof. André DeHon Research Interests: FPGA design methodology, Tools/CAD for FPGAs, Hardware Acceleration
	<b>B.S. in ECE, Carnegie Mellon University</b> <span style="float: right;"><i>Aug'12-Dec'15</i></span> Recipient of David Tuma Project Award – Best ECE Capstone Project Award Graduated with University Honors
ACADEMIC RESEARCH	<b>Software-like Incremental Refinement on FPGA [1]</b> <span style="float: right;"><i>Feb'23-Present</i></span> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> <li>Proposed a fast incremental refinement strategy for FPGA designs that resembles SW compilation</li> <li>Created a multi-clock system with a NoC (400MHz) and compute kernels (200–400MHz)</li> <li>Designed a runtime bottleneck identification for HLS dataflow designs using FIFO full/empty counters</li> <li>Improved application latency 2.2–12.7× while reducing Design Space Exploration time by 1.3–2.7×</li> </ul>
	<b>Network-on-a-Chip (NoC) on FPGA [2]</b> <span style="float: right;"><i>Sep'22-Jan'23</i></span> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> <li>Designed a novel asymmetric Butterfly Fat Tree NoC in Verilog that excels in unbalanced traffic</li> <li>Analyzed throughput and worst case latency in realistic graph workloads and synthetic traffic patterns</li> <li>Achieved up to 76% more throughput than existing Butterfly Fat Tree NoC with the similar resource usage</li> </ul>
	<b>Parallel FPGA Compilation using Hierarchical Partial Reconfiguration [4]</b> <span style="float: right;"><i>Jan'22-Aug'22</i></span> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> <li>Open-sourced the Makefile/Python/Tcl based FPGA's parallel compilation framework (<a href="#">link</a>)</li> <li>Provided flexibility in sizes of compile slots for parallel FPGA compilations, utilizing Xilinx Nested DFX</li> <li>Only 2–5 min to compile realistic benchmarks, from HLS to bitstream (2.2–5.3× speedup over Xilinx Vitis)</li> </ul>
	<b>Accelerating FPGA Compilation using NoC and Partial Reconfiguration [6][7]</b> <span style="float: right;"><i>May'17-Aug'18</i></span> Advisor: Prof. André DeHon, University of Pennsylvania <ul style="list-style-type: none"> <li>Designed packet parser, reassembly buffer, and FIFO modules in Verilog for the NoC interface</li> <li>Analyzed Xilinx Vivado's compile speed with case studies and revealed the limitations of the vendor tool</li> <li>Showed 4.5× speedup in PnR time over Xilinx Vivado's compilation with a divide-and-conquer approach</li> </ul>
	<b>Detecting Voltage Anomalies in Scan-Testing Environment on FPGA</b> <span style="float: right;"><i>Dec'14-Oct'15</i></span> Advisor: Prof. Shawn Blanton, CMU <ul style="list-style-type: none"> <li>Implemented a synthesizable, fine-grained voltage sensor on FPGA using carry chains and latches</li> <li>Analyzed voltage activities for three different ISCAS'89 circuits in at-speed scan testing environment</li> </ul>
INDUSTRY EXPERIENCE	<b>AMD, San Jose, CA, USA</b> <span style="float: right;"><i>(incoming) May'24-Aug'24</i></span> <i>(incoming) FPGA Architecture Intern</i>
	<b>AnaPass, South Korea</b> <span style="float: right;"><i>Jul'20-Jul'21</i></span> <i>SoC Engineer (in fulfilment of military service)</i> <ul style="list-style-type: none"> <li>RTL verification of Timing Controller IP for Samsung Tablet display</li> </ul>
	<b>Korea Advanced Institute of Science and Technology (KAIST), South Korea</b> <span style="float: right;"><i>Aug'18-Jul'20</i></span> <i>Research Engineer (in fulfilment of military service)</i> <ul style="list-style-type: none"> <li>Projects on Radar-based fall detector, FPGA-based beamforming system, IQ imbalance calibration</li> </ul>
	<b>CoMira Solutions, Pittsburgh, PA, USA</b> <span style="float: right;"><i>Jun'14-Aug'14</i></span> <i>Hardware Engineering Intern</i> <ul style="list-style-type: none"> <li>Optimized hardware implementation of CRC in area and timing using a table-based approach</li> </ul>
	<b>HW/SW co-design for VGG16, University of Pennsylvania</b> <span style="float: right;"><i>Nov'21-Dec'21</i></span> <ul style="list-style-type: none"> <li>Designed a systolic array based FPGA acceleration kernel for 2D convolution function using HLS</li> <li>Integrated multiple FPGA kernels (on AWS EC2 F1) with PyTorch using C++ extension</li> <li>Demonstrated 11–14.8× performance improvement over the SW baseline of 2D convolution (<a href="#">report link</a>)</li> </ul>

PUBLICATIONS	[1] REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs <u>D. Park</u> , A. DeHon ACM Int. Symp. on Field-Programmable Gate Arrays (FPGA), 2024 – <i>to appear</i>		
	[2] Asymmetry in Butterfly Fat Tree FPGA NoC <u>D. Park</u> , Z. Yao, Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2023		
	[3] ExHiPR: Extended High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, <u>D. Park</u> , Z. Niu, A. Hota , A. DeHon ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2023		
	[4] Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration <u>D. Park</u> , Y. Xiao, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2022 (acceptance rate: 25.2% = 31/123), Artifact Evaluated - Available, Functional, Reusable, Replicated		
	[5] HiPR: High-level Partial Reconfiguration for Fast Incremental FPGA Compilation Y. Xiao, A. Hota, <u>D. Park</u> , A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2022 ( <b>Best Paper Candidate</b> : 7.0% = 9/129)		
	[6] Reducing FPGA Compile Time with Separate Compilation for FPGA Building Blocks Y. Xiao, <u>D. Park</u> , A. Butt, H. Giesen, Z. Han, R. Ding, N. Magnezi, R. Rubin, A. DeHon IEEE Int. Conf. on Field-Programmable Technology (FPT), 2019 (acceptance rate: 25.0% = 26/104)		
	[7] Case for Fast FPGA Compilation using Partial Reconfiguration <u>D. Park</u> , Y. Xiao, N. Magnezi, A. DeHon IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2018		
TALKS	<ul style="list-style-type: none"> <li>• <b>Asymmetry in Butterfly Fat Tree FPGA NoC</b> – at FPT 2023, Yokohama, Japan (<i>talk video, slides</i>) <span style="float:right">Dec'23</span></li> <li>• <b>Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration</b> – at FPT 2022, Hong Kong (<i>talk video, slides</i>) <span style="float:right">Dec'22</span> – at ESE PhD seminar, University of Pennsylvania, Philadelphia, PA, USA (<i>slides</i>) <span style="float:right">Oct'22</span></li> <li>• <b>High-level Partial Reconfiguration for Fast Incremental FPGA Compilation</b> – at FPL 2022, Belfast, Northern Ireland (<i>slides</i>) <span style="float:right">Aug'22</span></li> <li>• <b>Case for Fast FPGA Compilation using Partial Reconfiguration</b> – at FPL 2018, Dublin, Ireland (<i>slides</i>) <span style="float:right">Aug'18</span></li> </ul>		
AWARDS/ SERVICE	<ul style="list-style-type: none"> <li>• Student Recognition Award, University of Pennsylvania <span style="float:right">Apr'23</span></li> <li>• Best Presentation Award, Penn ESE PhD seminar (F2022-S2023) <span style="float:right">Apr'23</span></li> <li>• <b>Samsung Electronics Global Fellowship</b> with post-graduation employment offer <span style="float:right">Oct'22</span></li> <li>• <b>Best Paper Candidate</b>, FPL2022 <span style="float:right">Aug'22</span></li> <li>• PhD Fellowship, University of Pennsylvania <span style="float:right">Aug'16</span></li> <li>• <b>Best ECE Capstone Project Award</b> (Project: Neural Networks on FPGA), CMU <span style="float:right">May'16</span></li> <li>• University Honors, CMU <span style="float:right">May'16</span></li> <li>• Penn ESE PhD students seminar organizer <span style="float:right">Feb'23-Dec'23</span></li> <li>• Judge, Research Experience for Undergraduates, University of Pennsylvania <span style="float:right">Aug'23</span></li> </ul>		
TEACHING ASSISTANT	<ul style="list-style-type: none"> <li>• <b>SoC Architecture</b> (ESE5320), University of Pennsylvania <span style="float:right">Fall 2021, Fall 2022</span> – Co-authored homework labs on multi-core, SIMD, HW acceleration, HLS, Xilinx Vitis – Held C/exam review sessions and weekly office hours for the graduate level course (20-40 students) – TA rating for Fall 2022: 3.74/4, the highest of all 7 offerings of the course's history</li> <li>• <b>Mathematical Foundations of Electrical Engineering</b> (18-202), CMU <span style="float:right">Fall 2014</span></li> <li>• <b>Structure and Design of Digital Systems</b> (18-240), CMU <span style="float:right">Spring 2014</span></li> </ul>		
SKILLS	<b>Hardware</b>	Verilog, Vivado, Vitis HLS, Quartus, HDL Simulation tools, OpenCL	
	<b>Software</b>	C++, Python, PyTorch, scikit-learn, Tcl, Shell scripting	
RELEVANT COURSES	Computer Architecture HW/SW Co-Design for ML	Computer Organization Advanced Computer Arch. (GPU)	SoC Architecture Big Data Analytics