Dongjoon(DJ) Park

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Education

Ph.D. in **ESE**, **University of Pennsylvania** *Aug'16-Jul'18, Aug'21-Present*
Advisor: Prof. André DeHon
Research Interests: Tools for FPGAs, FPGA design methodology

B.S. in **ECE**, **Carnegie Mellon University** *Aug'12–Dec'15*
Recipient of David Tuma Project Award – Best ECE Capstone Project Award
Graduated with University Honors

Academic Research

Software-like FPGA Development [1] *Feb'23–Present*
Advisor: Prof. André DeHon, University of Pennsylvania
- Novel incremental refinement for FPGA designs, iterating initial design points with separate compilations
- Created a multiple-clock system with a NoC (400MHz) and compute kernels (200–400MHz)
- Designed a runtime bottleneck identification for HLS dataflow designs using FIFO full/empty counters
- Utilized ML-based classifiers to reduce resource fragmentation for separate FPGA compile technique
- Showed 1.3–2.7× speedup in Design Space Exploration time and 2.2–12.7× in application latency

Network-on-a-Chip (NoC) on FPGA [2] *Sep'22–Jan'23*
Advisor: Prof. André DeHon, University of Pennsylvania
- Designed a novel asymmetric Butterfly Fat Tree NoC in Verilog that excels in unbalanced traffic
- Demonstrated up to 32% and 76% throughput benefit in realistic workloads and synthetic traffic patterns

Parallel FPGA Compilation using Hierarchical Partial Reconfiguration [4] *Jan'22–Aug'22*
Advisor: Prof. André DeHon, University of Pennsylvania
- Open-sourced the Makefile/Python/Tcl based FPGA's parallel compilation framework (*link*)
- Utilized Xilinx Nested DFX to support flexible-sized slots for parallel FPGA compilations
- Demonstrated 1.4–4.9× latency improvement for realistic HLS applications over the previous work

Accelerating FPGA Compilation using Partial Reconfiguration [6][7] *May'17–Aug'18*
Advisor: Prof. André DeHon, University of Pennsylvania
- Designed packet parser, reassembly buffer, and FIFO modules for NoC interface in Verilog
- Analyzed Xilinx Vivado's compile speed with case studies to optimize separate FPGA compile strategy
- Demonstrated 4.5× compile time speedup for a multi-core design on FPGA over Xilinx Vivado

Detecting Voltage Anomalies in Scan-Testing Environment on FPGA *Dec'14–Oct'15*
Advisor: Prof. Shawn Blanton, Carnegie Mellon University
- Implemented synthesizable voltage sensors on FPGA using carry chains and latches
- Analyzed voltage activities for different sizes of ISCAS circuits in at-speed scan testing environment

Industry Experience

AnaPass, South Korea *Jul'20–Jul'21*
SoC Engineer
- RTL verification of Timing Controller IP for Samsung Tablet display

Korea Advanced Institute of Science and Technology (KAIST), South Korea *Aug'18–Jul'20*
Research Engineer
- Projects on Radar-based fall detector, FPGA-based beamforming system, IQ imbalance calibration

CoMira Solutions, Pittsburgh, PA *Jun'14–Aug'14*
Hardware Engineering Intern

Course Projects

HW/SW co-design for VGG16, University of Pennsylvania *Nov'21–Dec'21*
- Designed a systolic array based FPGA kernel for 2D convolution function using HLS
- Integrated multiple FPGA kernels (on AWS EC2 F1 instance) with PyTorch using C++ extension
- Achieved 11–14.8× performance improvement over the SW baseline of 2D convolution function (*report link*)

Publications

[1] REFINE: Runtime Execution Feedback for INcremental Evolution on FPGA Designs
D. Park, A. DeHon
ACM Int. Symp. on Field-Programmable Gate Arrays (FPGA), 2024 – *to appear*

[2] Asymmetry in Butterfly Fat Tree FPGA NoC
D. Park, Z. Yao, Y. Xiao, A. DeHon
IEEE Int. Conf. on Field-Programmable Technology (FPT), 2023

[3] ExHiPR: Extended High-level Partial Reconfiguration for Fast Incremental FPGA Compilation
Y. Xiao, **D. Park**, Z. Niu, A. Hota , A. DeHon
ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2023

[4] Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration
D. Park, Y. Xiao, A. DeHon
IEEE Int. Conf. on Field-Programmable Technology (FPT), 2022
(acceptance rate: 25.2% = 31/123), Artifact Evaluated - Available, Functional, Reusable, Replicated

[5] HiPR: High-level Partial Reconfiguration for Fast Incremental FPGA Compilation
Y. Xiao, A. Hota, **D. Park**, A. DeHon
IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2022
(***Best Paper Candidate***: 7.0% = 9/129)

[6] Reducing FPGA Compile Time with Separate Compilation for FPGA Building Blocks
Y. Xiao, **D. Park**, A. Butt, H. Giesen, Z. Han, R. Ding, N. Magnezi, R. Rubin, A. DeHon
IEEE Int. Conf. on Field-Programmable Technology (FPT), 2019
(acceptance rate: 25.0% = 26/104)

[7] Case for Fast FPGA Compilation using Partial Reconfiguration
D. Park, Y. Xiao, N. Magnezi, A. DeHon
IEEE Int. Conf. on Field-Programmable Logic and Applications (FPL), 2018

Talks

- **Asymmetry in Butterfly Fat Tree FPGA NoC**
  – at FPT 2023, Yokohama, Japan (*talk video*, *slides*) *Dec'23*
- **Fast and Flexible FPGA development using Hierarchical Partial Reconfiguration**
  – at FPT 2022, Hong Kong (*talk video*, *slides*) *Dec'22*
  – at ESE PhD seminar, University of Pennsylvania, Philadelphia, PA (*slides*) *Oct'22*
- **High-level Partial Reconfiguration for Fast Incremental FPGA Compilation**
  – at FPL 2022, Belfast, Northern Ireland (*slides*) *Aug'22*
- **Case for Fast FPGA Compilation using Partial Reconfiguration**
  – at FPL 2018, Dublin, Ireland (*slides*) *Aug'18*

Awards/ Service

- Student Recognition Award, University of Pennsylvania *Apr'23*
- Best Presentation Award, Penn ESE PhD seminar (F2022-S2023) *Apr'23*
- **Samsung Electronics Global Fellowship** with post-graduation employment offer *Oct'22*
- **Best Paper Candidate**, FPL2022 *Aug'22*
- PhD Fellowship, University of Pennsylvania *Aug'16*
- **Best ECE Capstone Project Award** (Project: NN on FPGA), Carnegie Mellon University *May'16*
- University Honors, Carnegie Mellon University *May'16*
- Penn ESE PhD students seminar organizer *Feb'23-Dec'23*
- Judge, Research Experience for Undergraduates, University of Pennsylvania *Aug'23*

Teaching Assistant

- **SoC Architecture**, University of Pennsylvania *Fall 2021*, *Fall 2022*
  – Co-authored homework labs on multi-core, SIMD, HW acceleration, HLS, Xilinx Vitis
  – Held C/exam review sessions and weekly office hours for the graduate level course (20-40 students)
  – High TA rating for Fall 2022: 3.74/4, the best of all 7 offerings of the course's history
- **Structure and Design of Digital Systems**, Carnegie Mellon University *Spring 2014*

Skills

Hardware Verilog, Xilinx FPGA (Vivado, Vitis HLS), Intel FPGA (Quartus), OpenCL
Software C++, Python, PyTorch, scikit-learn, Tcl

Relevant Courses

Computer Architecture	Computer Organization	SoC Architecture
HW/SW Co-Design for ML	Advanced Computer Arch.	Big Data Analytics