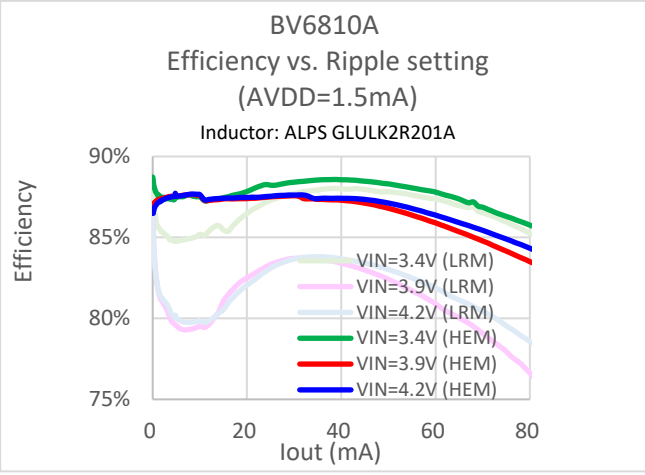
# AMOLED Power Solution

## 1 General Description

The BV6810A is a highly integrated power solution for AMOLED Display application, which uses a single-inductor-tripolar-output (SITO) converter to generate two positive and one negative voltage outputs. It does not need an extra charge pump circuit to generate the negative voltage output so that external capacitors required by the charge pump circuit can be eliminated and the PCB space can be achieved with very small.

The output voltages can be adjusted by SWIRE pin. Compared with the scheme of generating negative voltage by a charge pump circuit, the best energy conversion efficiency can only be obtained near the negative voltage ratio provided by its charge pump circuit. This SITO architecture can provide a stable high conversion efficiency throughout the entire negative voltage adjusting range. Therefore, this solution can provide the optimal negative voltage output value according to different brightness requirements to reduce the power consumption of the AMOLED display significantly. This is the best solution that can optimize the solution form factor as well as display power consumption.

With its input voltage range from 2.9V to 5.5V, BV6810A is optimized for products powered by single-cell batteries with output currents up to 80mA. The BV6810A is available in the WL-CSP-12B 1.39mm x 1.64mm package.




## 2 Features

- Input Voltage Range: 2.9V to 5.5V
- Positive Output Voltage AVDD Range: 2.8V to 3.7V
  (SET=Floating Default is 2.8V±1%)
  (SET=High/Low Default is 3.3V±1%)
- Positive Output Voltage OVDD Range: 2.6V to 5.3V
  (SET=High/Floating Default is 4.6V±1%)
  (SET=Low Default is 3.3V±1%)
- Negative Output Voltage OVSS Range: -0.6V to -4.7V
  (SET=High/Floating Default is -2.4V±1%)
  (SET=Low Default is -3.3V±1%)
- Low Quiescent Current: 25μA
- AVDD Max. Loading is 10mA, OVDD and OVSS Max. loading is 80mA.
- Built-in Internal Soft start
- UVLO, UVP, SCP, OCP, OTP, and SSP protection

## 3 Applications

- Wearable AMOLED Product

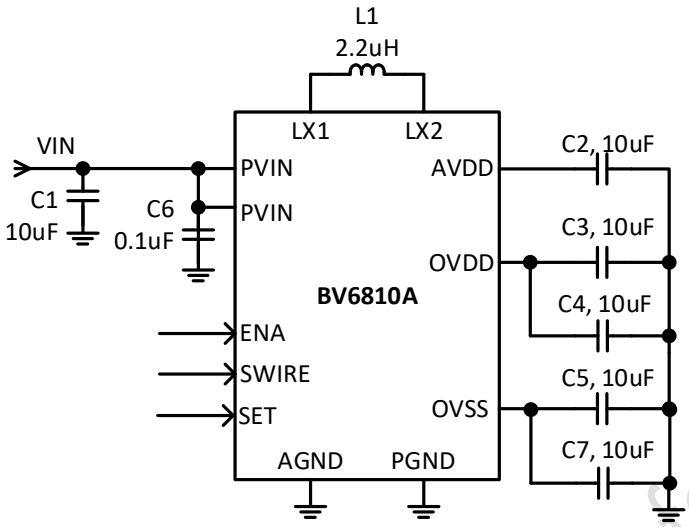
## 4 Ordering Information

| Part Number | Package | Body Size |
|---|---|---|
| BV6810A | WLCSP (12) | 1.39mmx1.64mm |

(1) For all available package, see the orderable addendum at the end of the datasheet.

Note:
Bravotek products are RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020Package Information.

## 5 Application Circuit




Note: AVDD=3.3V, OVDD=3.3V, OVSS=-3.3V when SET pull Low after power on

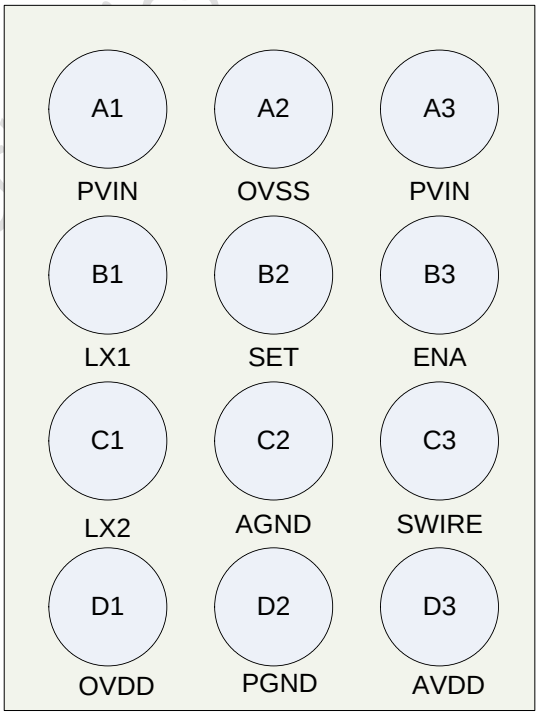
AVDD=3.3V, OVDD=4.6V, OVSS=-2.4V when SET pull High after power on

AVDD=2.8V, OVDD=4.6V, OVSS=-2.4V when SET is floating after power on

The SET pull-high/low resistor must have a resistance of 0 ohm

## 6 Pin Configuration and Function

**BV6810A**



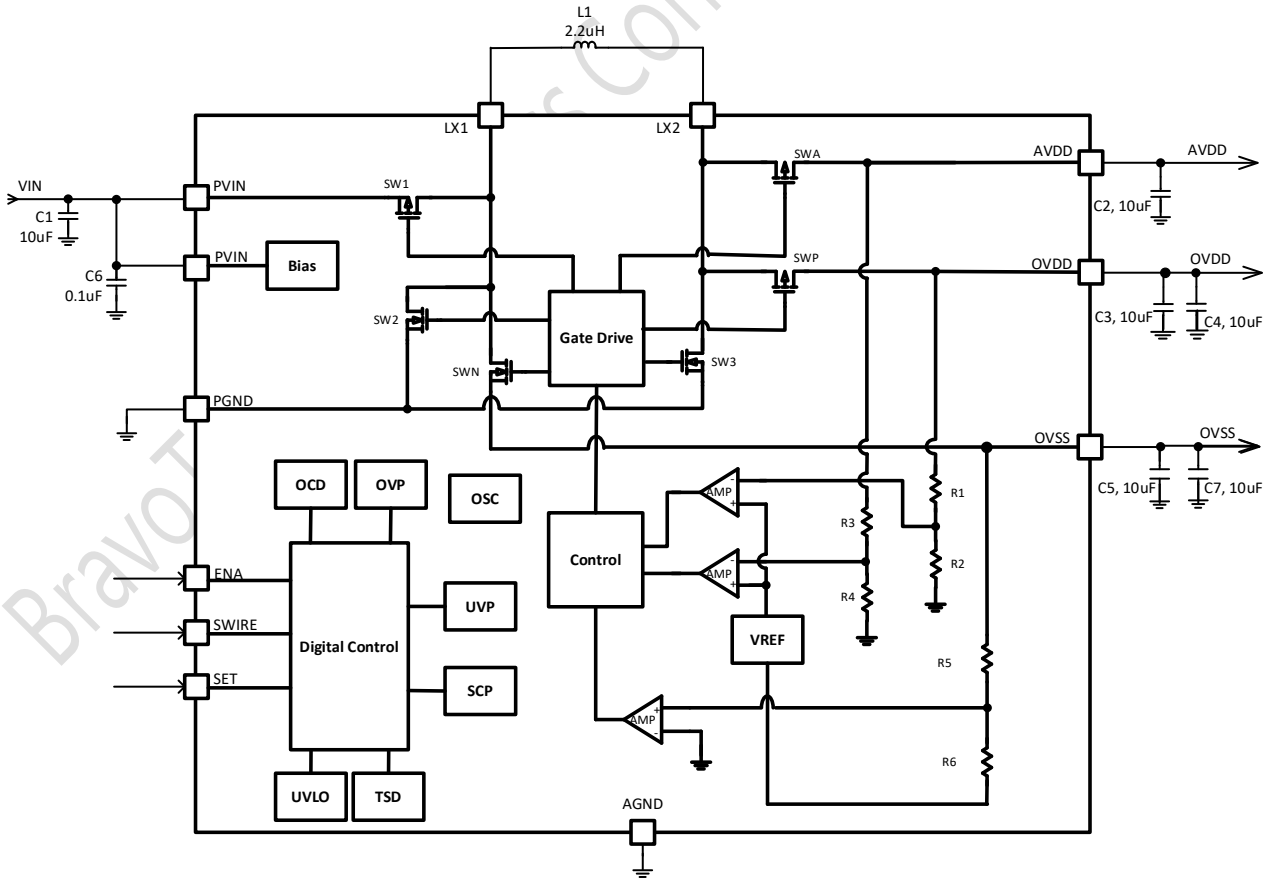

Top View

| Pin | Name | Function |
|---|---|---|
| A1 | PVIN | Power Input for SITO |
| A2 | OVSS | OVSS Output |
| A3 | PVIN | Power Input for SITO |
| B1 | LX1 | LX1 switching node for SITO |
| B2 | SET | The Pin for Setting default voltage |
| B3 | ENA | Enable for IC and AVDD |
| C1 | LX2 | LX2 switching node for SITO |
| C2 | AGND | Analog Ground |
| C3 | SWIRE | SWIRE Control Interface |
| D1 | OVDD | OVDD Output |
| D2 | PGND | Power Ground |
| D3 | AVDD | AVDD Output |

## 7 Device Comparable Table

| Device Option | Package | Rated Current | Output Voltage |
|---|---|---|---|
| BV6810AW | WLCSP-12B 1.39mm x 1.64mm | OVDD, OVSS: 80mA<br>AVDD: 10mA | Set by SWIRE |

## 8 Functional Block Diagram



## 9 Absolute Maximum Ratings

- Supply Input Voltage: PVIN to ANGD, PGND .....-0.3V to 6.0V
- AVDD, OVDD, SWIRE, ENA, SET to AGND, PGND .....-0.3V to 6.0V
- OVSS to AGND, PGND .....-6.0V to 0.3V
- Power Dissipation, PD@ TA=25°C
  WL-CSP-12B ..... 1.42W
- Package Thermal Resistance
  WL-CSP-12B, $\theta_{JA}$ ..... 80.84°C/W
  WL-CSP-12B, $\theta_{Jc}$ ..... 4.5°C/W
- Lead Temperature (Soldering, 10sec.) ..... 260°C
- Junction Temperature ..... 150°C
- Storage Temperature .....-65°C to 150°C
- ESD Susceptibility
  HBM (Human Body Model) ..... 2KV
  CDM (Machine Model) ..... 500V

## 10 Recommended Operating Conditions

- Supply Input Voltage ..... 2.9V to 5.5V
- Junction Temperature Range .....-40°C to 125°C
- Ambient Temperature Range .....-40°C to 85°C

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The device is not guaranteed to function outside its recommended operating conditions.

# 11 Components Selection

## 11.1 Inductor

| Reference | Value | Component supplier | Package | Isat / DCR |
|---|---|---|---|---|
| L1 | 2.2uH | ALPS GLULK2R201A | 2.5mm x 2.0mm x 1.0mm | 1.8A / 85mΩ |
| L1 | 2.2uH | Cyntec HTQA20161T-2R2MSRG | 2.0mm x 1.6mm x 1.0mm | 2.6A / 100mΩ |

## 11.2 Capacitors

| Reference | Value | Component supplier | Package |
|---|---|---|---|
| C1, C2, C5, C7(*2) C3, C4 | 10uF/6.3V | GRM155R60J106ME15D | 0402 |
| C6 | 0.1uF/6.3V | GRM033R60J104KE19D | 0201 |
| C3(*1), C4(*1) | 22uF/6.3V | GRM158R60J226ME01D | 0402 |
| C3(*1) C4 (*1) : 10uF capacitance is also recommended for C3 and C4, depending on visual performance.<br>C7 (*2) : Removing C7 is also recommended, depending on visual performance. | | | |

## 12 Electrical Characteristics

| $V_{IN}$=3.7V, AVDD=2.8V, OVDD=4.6V, OVSS=-2.4V, $T_A$=25°C, unless otherwise specified. | | | | | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
| Input Power Supply | | | | | | |
| Input Supply Voltage | $V_{IN}$ | | 2.9 | 3.7 | 5.5 | V |
| Quiescent Current | $I_Q$ | SWIRE=High, AVDD_EN=High, measured into VIN pin. No load | - | 25 | - | µA |
| Idle Current | $I_{IDLE}$ | AVDD_EN =High and SWIRE =Low | - | 14 | - | µA |
| Shutdown Current | $I_{SHDN}$ | AVDD_EN and SWIRE = Low | - | 0.2 | 1 | µA |
| Under-Voltage Lockout Threshold | $V_{UVLOH}$ | VIN Rising | - | 2.4 | 2.5 | V |
| | $V_{UVLOL}$ | VIN falling | - | 2.25 | 2.35 | V |
| Thermal Shutdown | $T_{SD}$ | | - | 140 | - | ˚C |
| Thermal Shutdown Hysteresis | $\Delta T_{SD}$ | | - | 10 | - | ˚C |
| SWIRE | | | | | | |
| SWIRE Logical High-Level Voltage | $V_{SRH}$ | $V_{IN}$=2.9V to 5.5V | 1.2 | - | - | V |
| SWIRE Logic Low-Level Voltage | $V_{SRL}$ | $V_{IN}$=2.9V to 5.5V | 0 | - | 0.4 | V |
| SWIRE Turn-off Detection | $T_{OFF\_DLY}$ | | - | - | 300 | µs |
| SWIRE Signal Stop Indicate Time | $T_{STOP}$ | | - | - | 300 | µs |
| SWIRE Rising Time | $T_r$ | | - | - | 200 | ns |
| SWIRE Falling Time | $T_f$ | | - | - | 200 | ns |
| Clocked SWIRE High | $T_{ON}$ | | 2 | 5 | 20 | µs |
| Clocked SWIRE Low | $T_{OFF}$ | | 2 | 5 | 20 | µs |
| Input Clocked SWIRE Frequency | $F_{SWIRE}$ | | 25 | - | 250 | KHz |
| ENA | | | | | | |
| AVDD Enable Input Voltage | $V_{IH}$ | $V_{IN}$=2.9V to 5.5V | 1.2 | - | - | V |
| | $V_{IL}$ | $V_{IN}$=2.9V to 5.5V | 0 | - | 0.4 | V |
| SITO | | | | | | |
| Over Current Protection | $I_{OCP}$ | | 0.75 | 0.9 | 1.15 | A |
| AVDD | | | | | | |
| Positive Output Voltage Range | $V_{AVDD\_RANGE}$ | SET=High/Low | 2.8 | 3.3 | 3.7 | V |
| | | SET=Floating | 2.8 | 2.8 | 3.7 | V |
| Positive Output Voltage Accuracy | $V_{AVDD\_ACC}$ | | -1 | - | 1 | % |
| Output Current Capability | $I_{AVDD}$ | | - | - | 10 | mA |
| Line Regulation | $V_{AVDD\_LINE}$ | $V_{IN}$=2.9 to 5.5V, $I_{AVDD}$=1.5mA | - | 3 | 5 | mV |
| Load Regulation | $V_{AVDD\_LOAD}$ | $I_{AVDD}$ = 0 to 10mA | - | - | 5 | mV |

| | | | | | | |
|---|---|---|---|---|---|---|
| Output Ripple | $V_{AVDD\_RIPPLE}$ | $I_{AVDD}$ = 1.5mA | - | - | 15 | mV |
| Current Limit | $I_{AVDD\_LIMIT}$ | | - | 20 | - | mA |
| Discharge Resistance | $R_{AVDD\_RDIS}$ | | - | 100 | - | Ω |
| Under Voltage Protection | | | 75 | 80 | 85 | % |
| UVP Detection Time | | | 0.4 | 0.5 | 0.5 | ms |
| Short Circuit Protection | $V_{AVDD\_SCP}$ | | - | 50 | - | % |
| OVDD | | | | | | |
| Positive Output Voltage Range | $V_{OVDD\_RANGE}$ | SET=High/Floating | 2.6 | 4.6 | 5.3 | V |
| | | SET=Low | 2.6 | 3.3 | 5.3 | V |
| Positive Output Voltage Accuracy | $V_{OVDD\_ACC}$ | | -1 | - | 1 | % |
| Output Current Capability | $I_{OVDD}$ | | - | - | 80 | mA |
| Line Regulation | $V_{OVDD\_LINE}$ | $V_{IN}$=2.9 to 5.5V, $I_{OVDD}$=1mA | - | 4 | 5 | mV |
| Load Regulation | $V_{OVDD\_LOAD}$ | $I_{OVDD}$ = 0 to 30mA | - | - | 5 | mV |
| Output Ripple | $V_{OVDD\_RIPPLE}$ | $I_{OVDD}$ = 10mA | - | - | 10 | mV |
| Discharge Resistance | $R_{OVDD\_RDIS}$ | | - | 100 | - | Ω |
| Under Voltage Protection | | | 85 | 90 | 95 | % |
| UVP Detection Time | | | 0.4 | 0.5 | 0.5 | ms |
| Short Circuit Protection | $V_{OVDD\_SCP}$ | | - | 50 | - | % |
| OVSS | | | | | | |
| Negative Output Voltage Range | $V_{OVSS\_RANGE}$ | SET=High/Floating | -4.7 | -2.4 | -0.6 | V |
| | | SET=Low | -4.7 | -3.3 | -0.6 | V |
| Negative Output Voltage Accuracy | $V_{OVSS\_ACC}$ | | -1 | - | 1 | % |
| Output Current Capability | $I_{OVSS}$ | | - | - | 80 | mA |
| Line Regulation | $V_{OVSS\_LINE}$ | $V_{IN}$=2.9 to 5.5V, $I_{OVSS}$=1mA | - | 4 | 5 | mV |
| Load Regulation | $V_{OVSS\_LOAD}$ | $I_{OVSS}$ = 0 to 30mA | - | - | 7 | mV |
| Output Ripple | $V_{OVSS\_RIPPLE}$ | $I_{OVSS}$ = 10mA | - | - | 15 | mV |
| Discharge Resistance | $R_{OVSS\_RDIS}$ | | - | 100 | - | Ω |
| Under Voltage Protection | | | 75 | 80 | 85 | % |
| UVP Detection Time | | | 0.4 | 0.5 | 0.5 | ms |
| Short Circuit Protection | $V_{OVSS\_SCP}$ | | - | 50 | - | % |

# 13 Detail Descriptions

The BV6810A operates with a six-switch buck-boost converter topology to generation a negative and two positive output voltages with a single inductor. The IC have the best efficiency over the entire load-current range. It is implemented by reducing the converter switching frequency into the PSM mode for light load. The output voltage can be set by SWIRE pin, OVSS voltage is from -0.6V to -4.7V. BV6810A can supply the maximum output current up to 80mA for high luminance application.

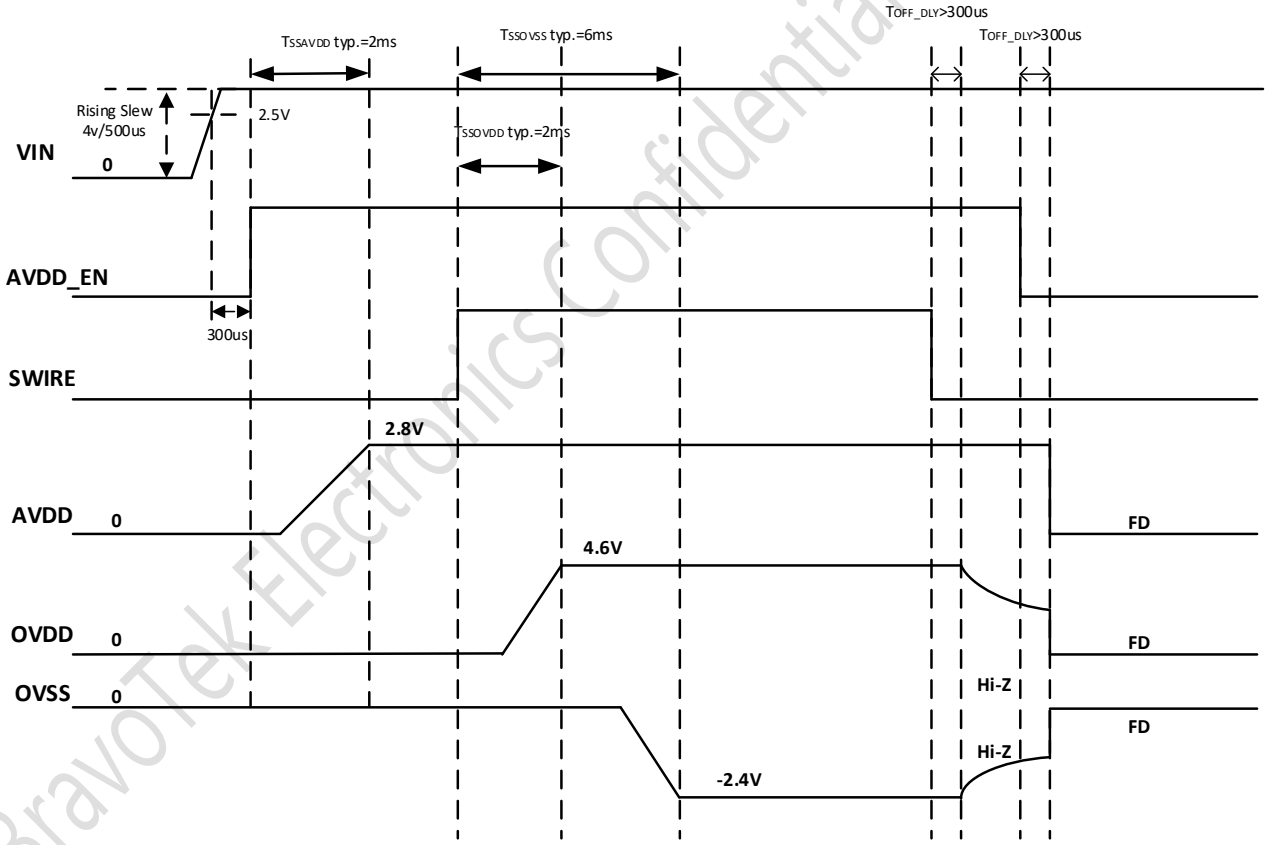
The BV6810A provides the Under-Voltage Protection (UVP), Short-Circuit Protection (SCP), Over-Temperature Protection (OTP) and Over-Current Protection (OCP).

## 13.1 Power Sequence

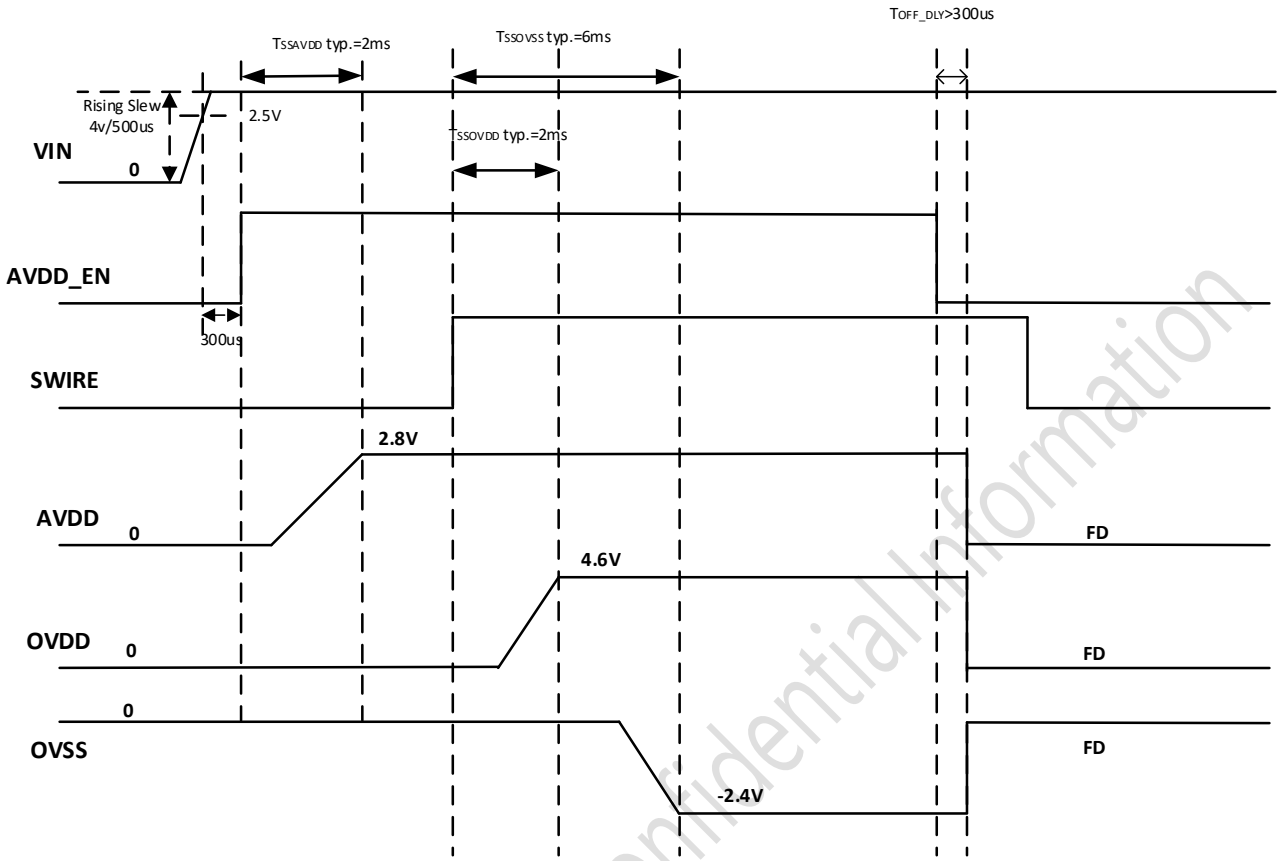
Note:

VIN rising time is not recommended if faster than 100us/4V

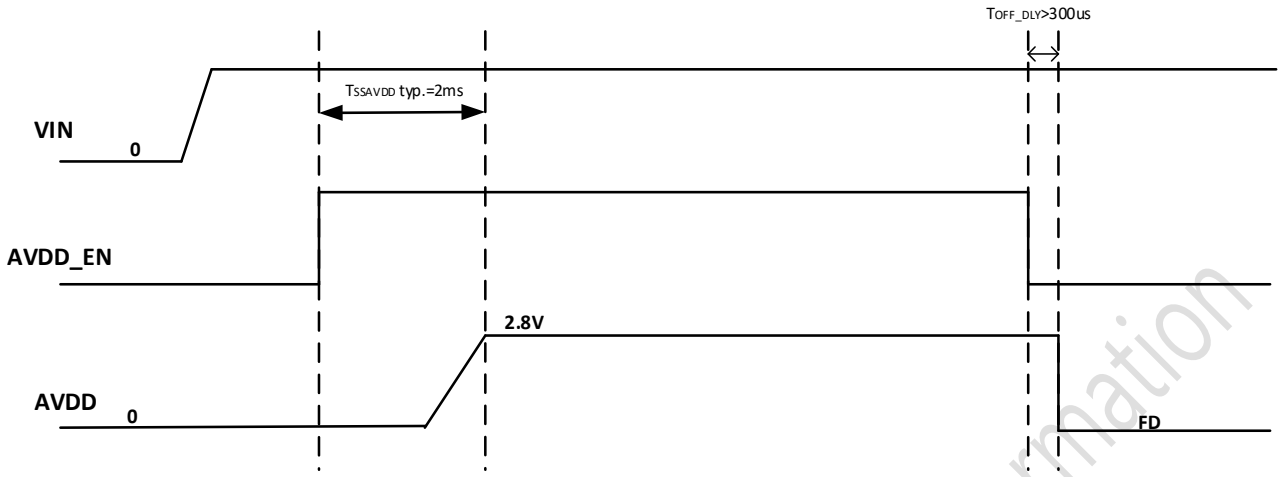
### 13.1.1 ENA = ON ➡ SWIRE=ON ➡ SWIRE=OFF ➡ ENA=OFF



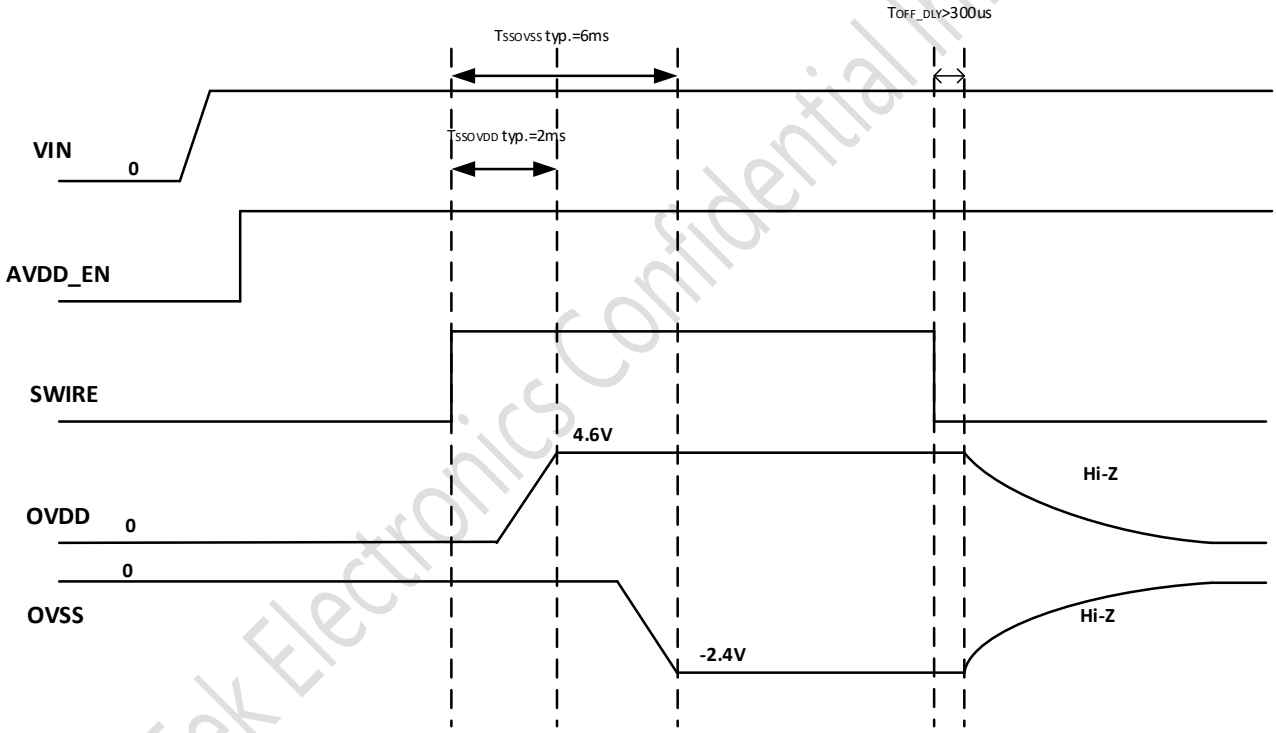
### 13.1.2 ENA = ON ➡ SWIRE=ON ➡ ENA=OFF ➡ SWIRE=OFF



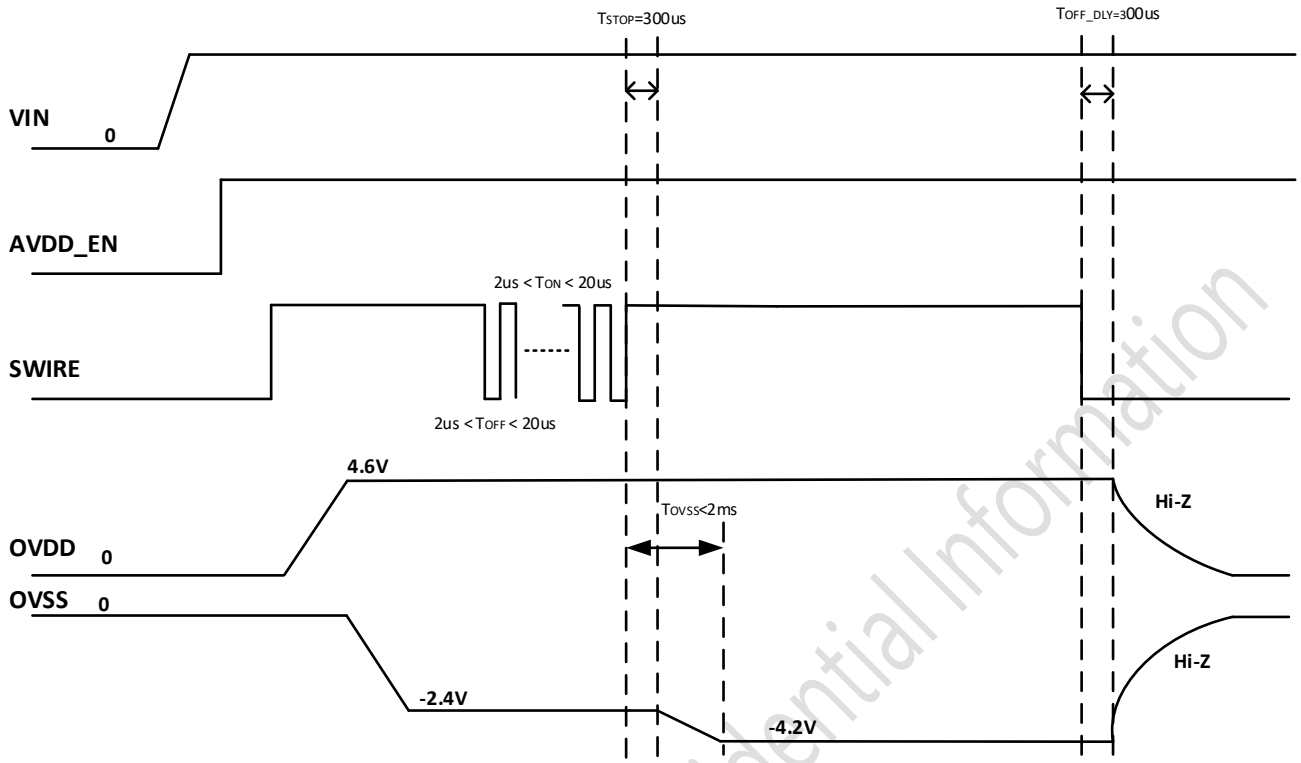
### 13.1.3 ENA Power ON-OFF Sequence




### 13.1.4 SWIRE Power ON-OFF Sequence



### 13.1.5 OVSS Voltage setting by SWIRE




## 13.2 Protection Functions

### 13.2.1 Under-Voltage Protection

All outputs are protected against short circuits either to GND. The IC will go into shutdown mode when the output voltage is under the limit level (OVDD=90%, AVDD/OVSS=80% and keep 0.5ms). The IC can only restart normal operation after re-power on.

### 13.2.2 Over-Temperature Protection

The BV6810A include an over temperature protection circuit to prevent overheating. The IC will disable positive and negative output when the junction temperature exceeds 140°C. Once the junction temperature drops down 10°C approximately, IC will automatically recovery into normal operation.

### 13.2.3 Short-Circuit Protection

All outputs are protected against short circuits either to GND. The IC will go into shutdown mode immediately when the output short to ground, and the output voltage is under the limit level (50%). The IC can only restart normal operation after re-power on.

### 13.2.4 Over-Current Protection

The BV6810A includes a cycle-by-cycle current limit function which monitor the inductor current during Phase 1 period. The power switch will be forced off to avoid large current damage IC when the current is over the limit level (0.9A).

### 13.3 SWIRE Setting

| Pulse | Function Description |
|---|---|
| 150 | AVDD, OVDD, OVSS setting switch to table II |
| 151 | AVDD, OVDD, OVSS setting switch to table I (Default) |

## Table I

| Pulse | Function Description |
|---|---|
| 3-5 | LX Slew rate Control |
| 10-13 | OVSS transient time method |
| 14-17 | VRC function |
| 18-19 | Ring-Killer function |
| 22-31 | AVDD setting (2.8V to 3.7V) |
| 36-63 | OVDD setting (2.6V to 5.3V) |
| 70-111 | OVSS setting (-4.7V to -0.6V) |
| 118-119 | Sleep Mode |
| 124 | OVDD and OVSS fast discharge when SWIRE pull low |
| 125 | OVDD and OVSS Hi-Z when SWIRE pull low |
| 128 | OVDD turn off (Hi-Z) |
| 129 | OVSS turn off (Hi-Z) |
| 130 | OVSS discharge to GND |
| 131 | Soft-Reset, clear above settings to default code (OVSS voltage setting doesn't) |

### 3~5 Pulse – LX Slew rate Control

| Pulse | Description |
|---|---|
| 3 | 1nS |
| 4 | 3nS |
| 5 | 5nS |

### 10, 13 Pulse – OVSS transient time method

| Pulse | Description |
|---|---|
| 10 | Direct change (40uS/0.1V) |
| 13 | Smoothly change within 16mS |

## 14~17 Pulse – VRC (VOUT Ripple Control) function

| Pulse | Description |
|---|---|
| 14 | Low Ripple Mode (LRM) |
| 15 | High Efficiency Mode (HEM) |
| 16 | Middle Ripple Mode (MRM) |
| 17 | Middle Efficiency Mode (MEM) |

## 18~19 Pulse – Ring-Killer function

| Pulse | Description |
|---|---|
| 18 | On |
| 19 | Off |

## 118~119 Pulse – Sleep Mode function

| Pulse | Description |
|---|---|
| 118 | Off |
| 119 | ON |

## 124 and 125 Pulse – Discharge function

| Default (125 Pulse) | | | | |
|---|---|---|---|---|
| AVDD_EN | SWIRE | AVDD | OVDD | OVSS |
| 0 | 0 | FD | FD | FD |
| 0 | 1 | FD | FD | FD |
| 1 | 0 | | Hi-Z | Hi-Z |

| 124 Pulse | | | | |
|---|---|---|---|---|
| AVDD_EN | SWIRE | AVDD | OVDD | OVSS |
| 0 | 0 | FD | FD | FD |
| 0 | 1 | FD | FD | FD |
| 1 | 0 | | FD | FD |

| Pulse | AVDD |
|---|---|
| 22 | 2.8V |
| 23 | 2.9V |
| 24 | 3.0V |
| 25 | 3.1V |
| 26 | 3.2V |
| 27 | 3.3V |
| 28 | 3.4V |
| 29 | 3.5V |
| 30 | 3.6V |
| 31 | 3.7V |

| Pulse | OVDD |
|---|---|
| 36 | 2.6V |
| 37 | 2.7V |
| 38 | 2.8V |
| 39 | 2.9V |
| 40 | 3.0V |
| 41 | 3.1V |
| 42 | 3.2V |
| 43 | 3.3V |
| 44 | 3.4V |
| 45 | 3.5V |
| 46 | 3.6V |
| 47 | 3.7V |
| 48 | 3.8V |
| 49 | 3.9V |
| 50 | 4.0V |
| 51 | 4.1V |
| 52 | 4.2V |
| 53 | 4.3V |
| 54 | 4.4V |
| 55 | 4.5V |
| 56 | 4.6V |
| 57 | 4.7V |
| 58 | 4.8V |
| 59 | 4.9V |
| 60 | 5.0V |
| 61 | 5.1V |
| 62 | 5.2V |
| 63 | 5.3V |

| Pulse | OVSS | Pulse | OVSS |
|---|---|---|---|
| 70 | -4.7V | 91 | -2.6V |
| 71 | -4.6V | 92 | -2.5V |
| 72 | -4.5V | 93 | -2.4V |
| 73 | -4.4V | 94 | -2.3V |
| 74 | -4.3V | 95 | -2.2V |
| 75 | -4.2V | 96 | -2.1V |
| 76 | -4.1V | 97 | -2.0V |
| 77 | -4.0V | 98 | -1.9V |
| 78 | -3.9V | 99 | -1.8V |
| 79 | -3.8V | 100 | -1.7V |
| 80 | -3.7V | 101 | -1.6V |
| 81 | -3.6V | 102 | -1.5V |
| 82 | -3.5V | 103 | -1.4V |
| 83 | -3.4V | 104 | -1.3V |
| 84 | -3.3V | 105 | -1.2V |
| 85 | -3.2V | 106 | -1.1V |
| 86 | -3.1V | 107 | -1.0V |
| 87 | -3.0V | 108 | -0.9V |
| 88 | -2.9V | 109 | -0.8V |
| 89 | -2.8V | 110 | -0.7V |
| 90 | -2.7V | 111 | -0.6V |

# Table II

| Pulse | Function Description |
|---|---|
| 3-5 | LX Slew rate Control |
| 10-13 | OVSS transient time method |
| 14-17 | VRC function |
| 18-19 | Ring-Killer function |
| 20-61 | OVSS setting (-4.7V to -0.6V) |
| 70-79 | AVDD setting (2.6V to 3.5V) |
| 80-107 | OVDD setting (2.6V to 5.3V) |
| 118-119 | Sleep Mode |
| 124 | OVDD and OVSS fast discharge when SWIRE pull low |
| 125 | OVDD and OVSS Hi-Z when SWIRE pull low |
| 128 | OVDD turn off (Hi-Z) |
| 129 | OVSS turn off (Hi-Z) |
| 130 | OVSS discharge to GND |
| 131 | Soft-Reset, clear above settings to default code (OVSS voltage setting doesn't) |

## 3~5 Pulse – LX Slew rate Control

| Pulse | Description |
|---|---|
| 3 | 1nS |
| 4 | 3nS |
| 5 | 5nS |

## 10, 13 Pulse – OVSS transient time method

| Pulse | Description |
|---|---|
| 10 | Direct change (40uS/0.1V) |
| 13 | Smoothly change within 16mS |

## 14~17 Pulse – VRC (VOUT Ripple Control) function

| Pulse | Description |
|---|---|
| 14 | Low Ripple Mode (LRM) |
| 15 | High Efficiency Mode (HEM) |
| 16 | Middle Ripple Mode (MRM) |
| 17 | Middle Efficiency Mode (MEM) |

## 18~19 Pulse – Ring-Killer function

| Pulse | Description |
|---|---|
| 18 | On |
| 19 | Off |

## 118~119 Pulse – Sleep Mode function

| Pulse | Description |
|---|---|
| 118 | Off |
| 119 | ON |

## 124 and 125 Pulse – Discharge function

| Default (125 Pulse) | | | | |
|---|---|---|---|---|
| AVDD_EN | SWIRE | AVDD | OVDD | OVSS |
| 0 | 0 | FD | FD | FD |
| 0 | 1 | FD | FD | FD |
| 1 | 0 | | Hi-Z | Hi-Z |

| 124 Pulse | | | | |
|---|---|---|---|---|
| AVDD_EN | SWIRE | AVDD | OVDD | OVSS |
| 0 | 0 | FD | FD | FD |
| 0 | 1 | FD | FD | FD |
| 1 | 0 | | FD | FD |

## Vout Pulse - Voltage function

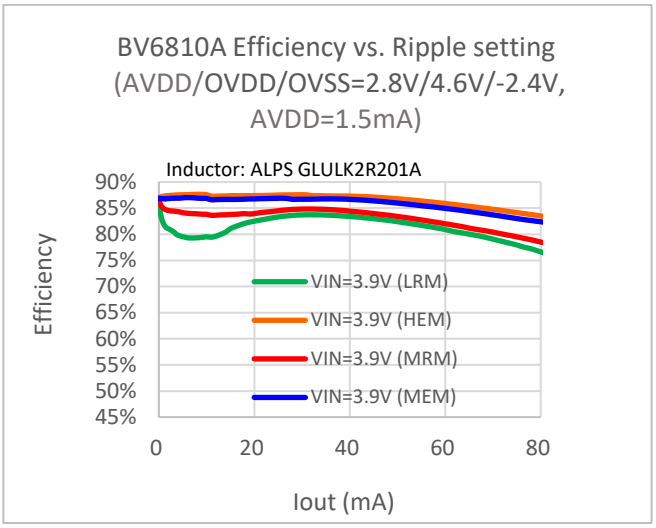
| Pulse | AVDD |
|---|---|
| 70 | 2.8V |
| 71 | 2.9V |
| 72 | 3.0V |
| 73 | 3.1V |
| 74 | 3.2V |
| 75 | 3.3V |
| 76 | 3.4V |
| 77 | 3.5V |
| 78 | 3.6V |
| 79 | 3.7V |

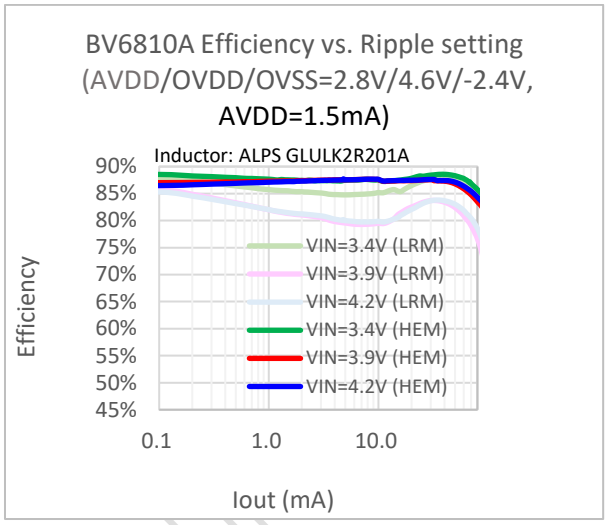
| Pulse | OVDD |
|---|---|
| 80 | 2.6V |
| 81 | 2.7V |
| 82 | 2.8V |
| 83 | 2.9V |
| 84 | 3.0V |
| 85 | 3.1V |
| 86 | 3.2V |
| 87 | 3.3V |
| 88 | 3.4V |
| 89 | 3.5V |
| 90 | 3.6V |
| 91 | 3.7V |
| 92 | 3.8V |
| 93 | 3.9V |
| 94 | 4.0V |
| 95 | 4.1V |
| 96 | 4.2V |
| 97 | 4.3V |
| 98 | 4.4V |
| 99 | 4.5V |
| 100 | 4.6V |
| 101 | 4.7V |
| 102 | 4.8V |
| 103 | 4.9V |
| 104 | 5.0V |
| 105 | 5.1V |
| 106 | 5.2V |
| 107 | 5.3V |

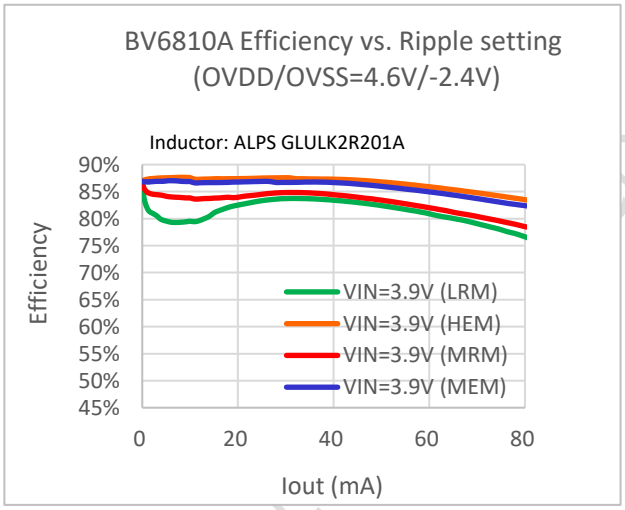
| Pulse | OVSS | Pulse | OVSS |
|---|---|---|---|
| 20 | -4.7V | 41 | -2.6V |
| 21 | -4.6V | 42 | -2.5V |
| 22 | -4.5V | 43 | -2.4V |
| 23 | -4.4V | 44 | -2.3V |
| 24 | -4.3V | 45 | -2.2V |
| 25 | -4.2V | 46 | -2.1V |
| 26 | -4.1V | 47 | -2.0V |
| 27 | -4.0V | 48 | -1.9V |
| 28 | -3.9V | 49 | -1.8V |
| 29 | -3.8V | 50 | -1.7V |
| 30 | -3.7V | 51 | -1.6V |
| 31 | -3.6V | 52 | -1.5V |
| 32 | -3.5V | 53 | -1.4V |
| 33 | -3.4V | 54 | -1.3V |
| 34 | -3.3V | 55 | -1.2V |
| 35 | -3.2V | 56 | -1.1V |
| 36 | -3.1V | 57 | -1.0V |
| 37 | -3.0V | 58 | -0.9V |
| 38 | -2.9V | 59 | -0.8V |
| 39 | -2.8V | 60 | -0.7V |
| 40 | -2.7V | 61 | -0.6V |

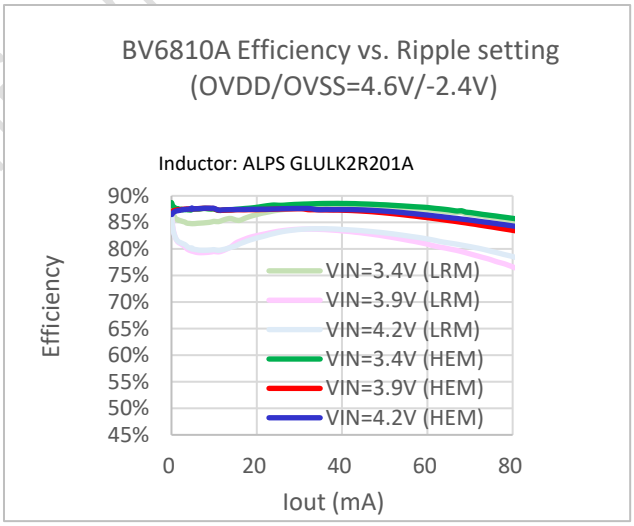
## 14 Operating Curve

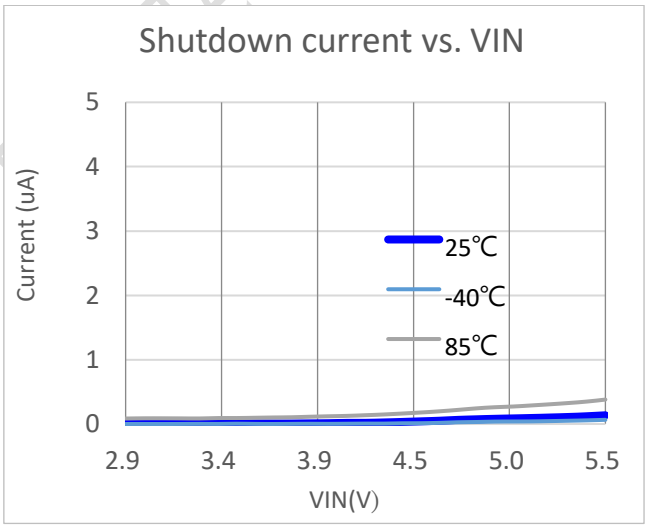
VIN=3.7V, AVDD=2.8V, OVDD=4.6V, OVSS=-2.4V, TA=25°C, unless otherwise specified

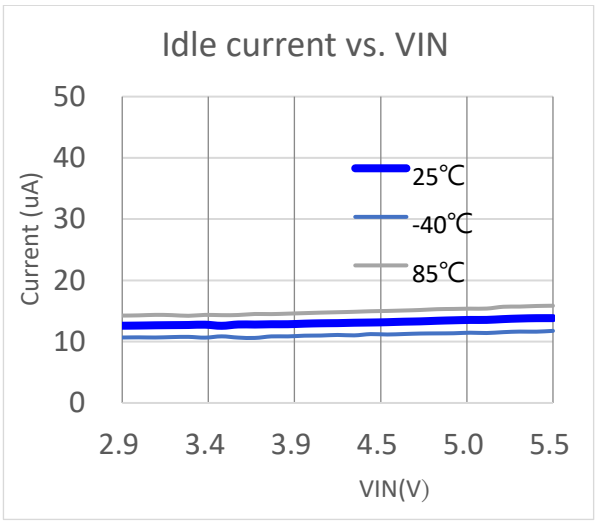


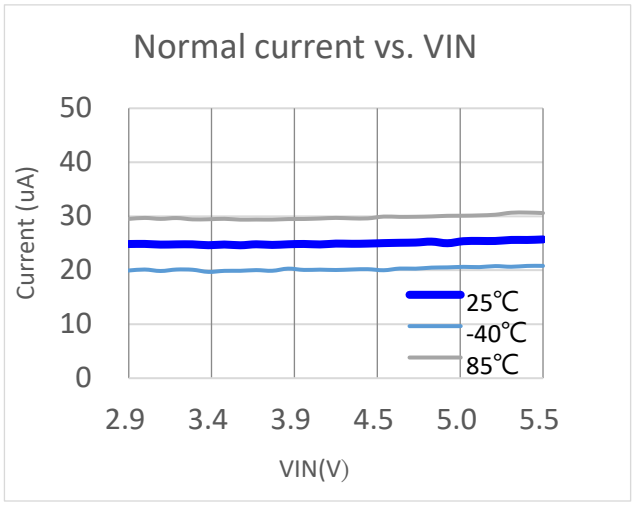



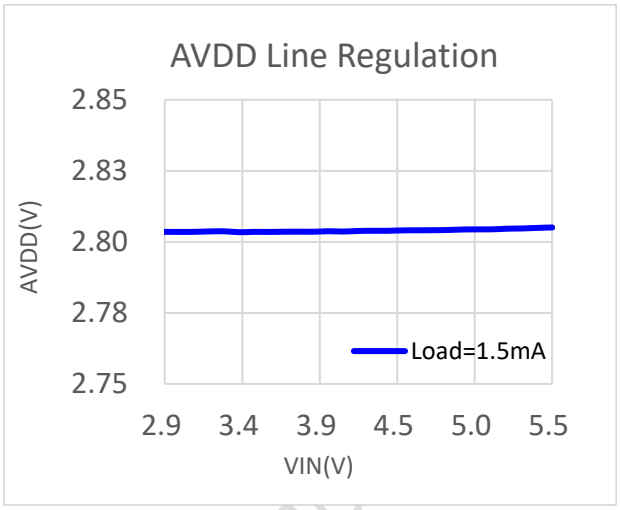



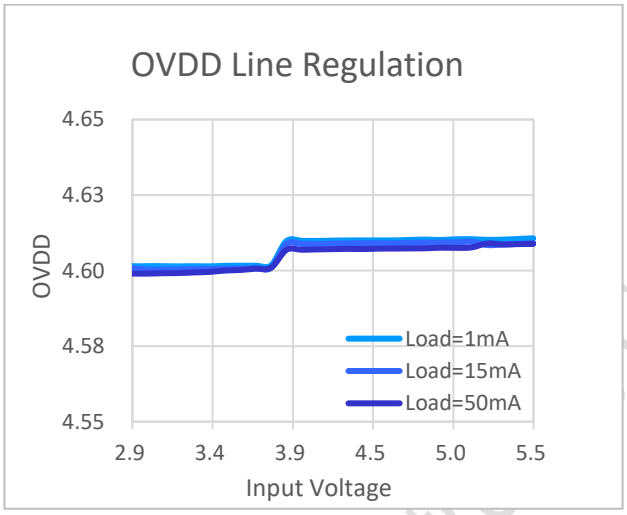



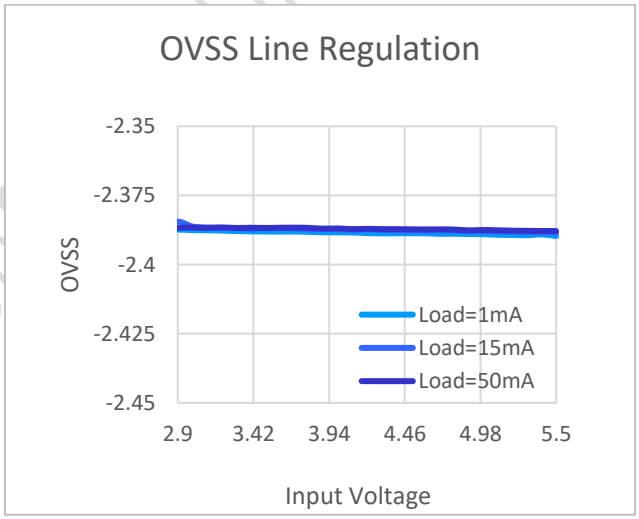



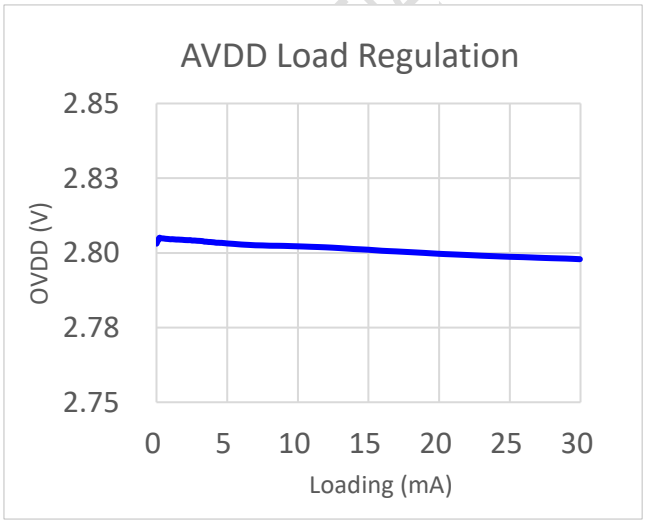



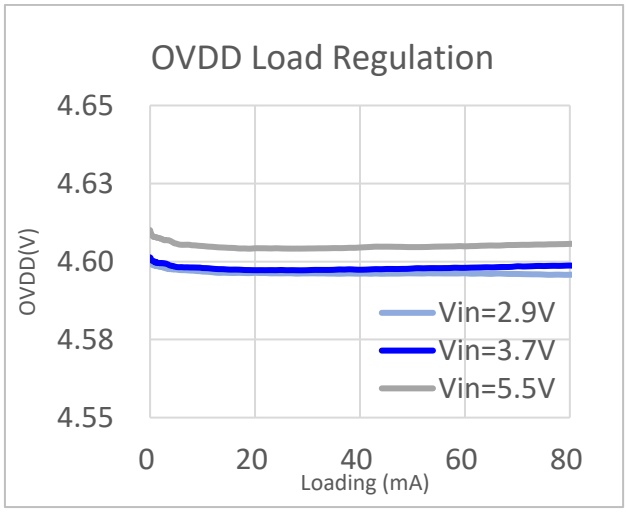


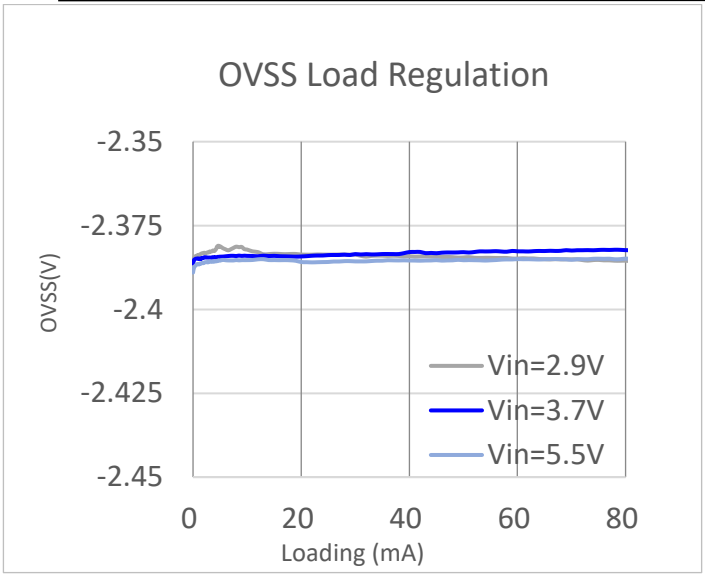



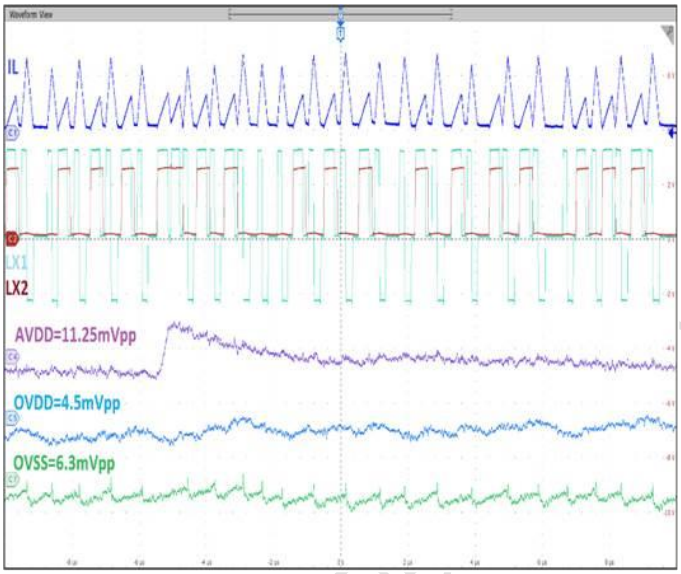



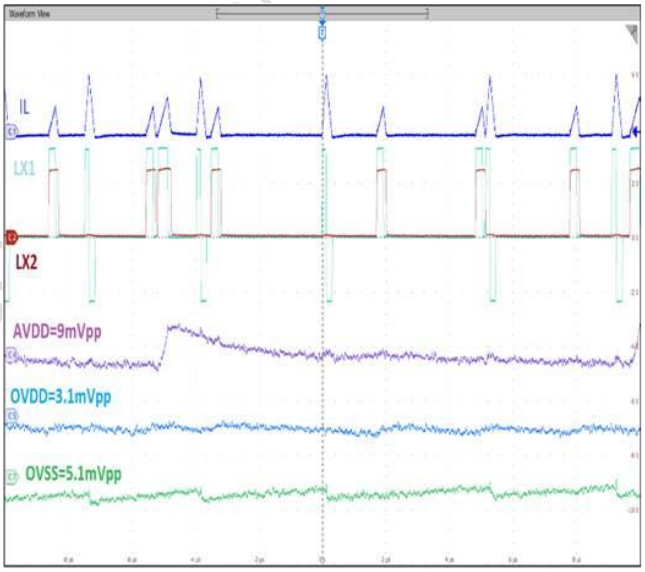






Waveform (CCM)

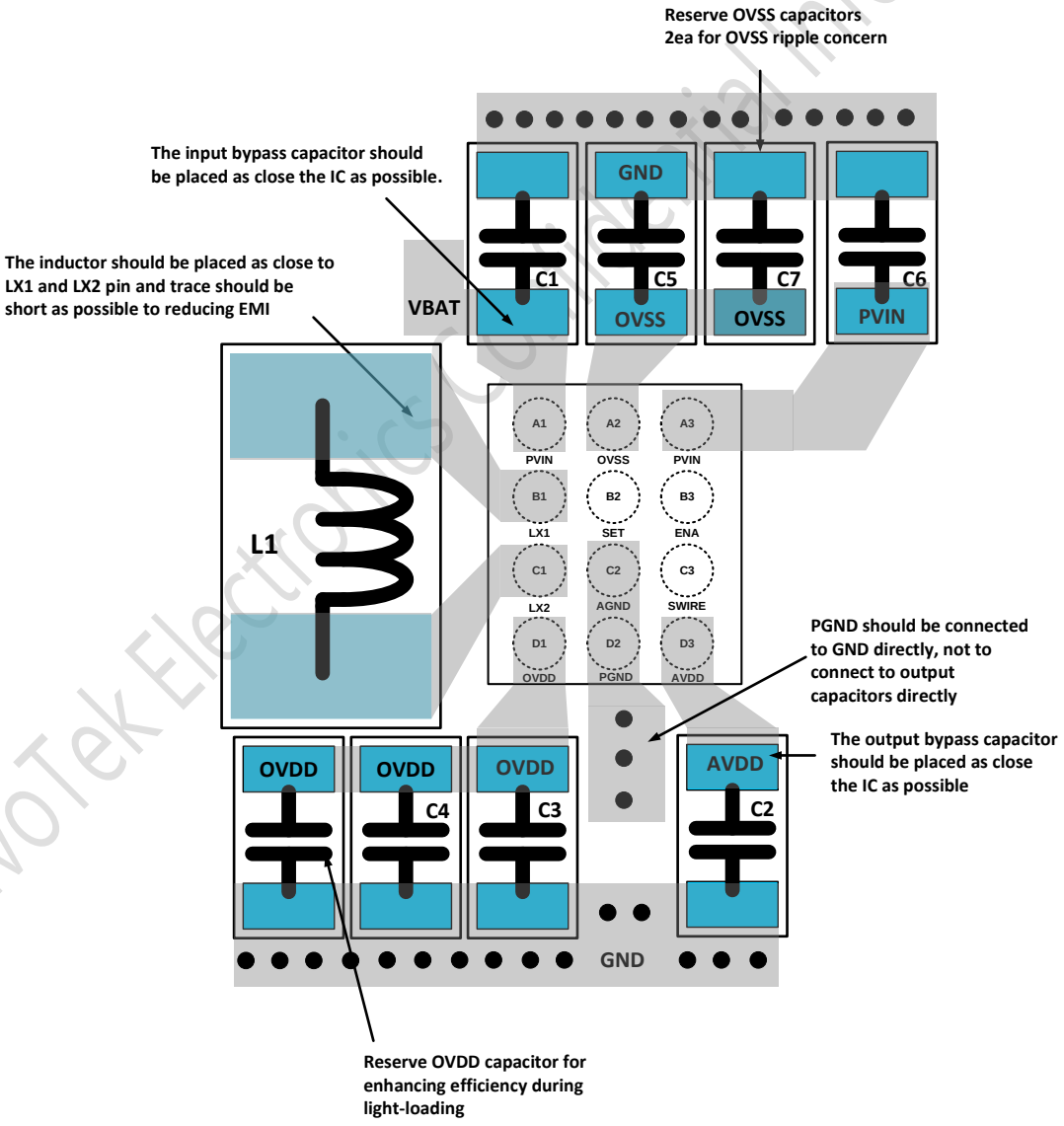



Waveform (DCM)

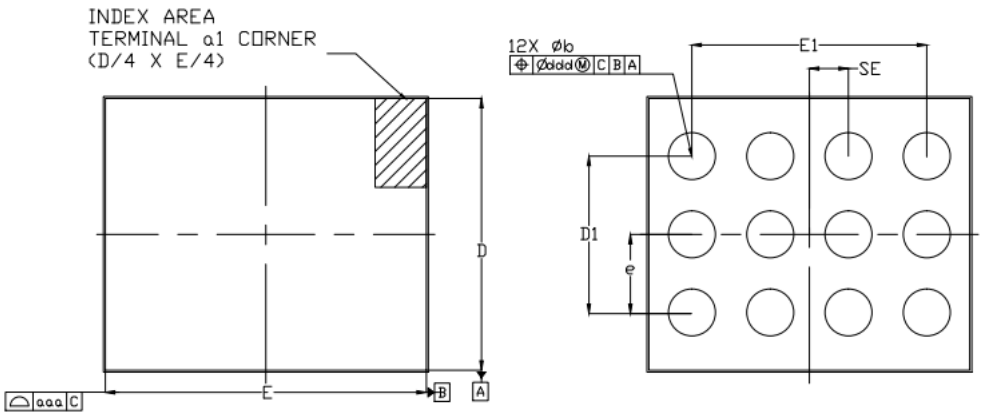
## 15 Layout Guidelines

For the best performance of the BV6810A, the basic principles listed should be strictly followed.

- Place C1 and C6 as close as possible to the PVIN pins respectively.
- Place C2, C3, C4 and C5 as close as possible to the AVDD, OVDD and OVSS pins respectively.
- Place L1 as close as possible to the LX1 and LX2 pins.
- For good regulation, the power traces should be wide and short especially for the high current output loop.
- Do not connect PGND with output ground directly.
- Reserve OVSS capacitors 2ea for OVSS ripple concern.
- Reserve OVDD capacitor for enhancing efficiency when light-loading
- Bottom layer should have ground plant

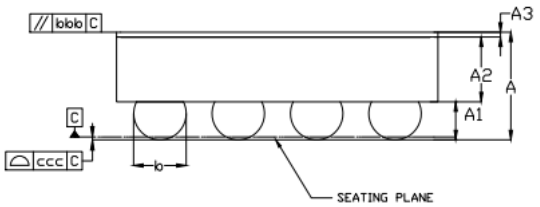


## 16 Outline Dimension




TOP VIEW (BUMP SIDE DOWN)

BOTTOM VIEW (BUMP SIDE UP)




SIDE VIEW

| DIMENSIONAL REFERENCES (mm) | | | |
|---|---|---|---|
| REF. | MIN | NOM | MAX |
| A | 0.502 | 0.549 | 0.596 |
| A1 | 0.175 | 0.194 | 0.213 |
| A2 | 0.305 | 0.330 | 0.355 |
| A3 | 0.022 | 0.025 | 0.028 |
| D | | 1.390 | |
| E | | 1.640 | |
| b | 0.228 | 0.268 | 0.308 |
| D1 | | 0.800 BSC | |
| E1 | | 1.200 BSC | |
| SD | | – | |
| SE | | 0.200 BSC | |
| e | | 0.400 BSC | |
| aaa | | 0.030 | |
| bbb | | 0.060 | |
| ccc | | 0.050 | |
| ddd | | 0.015 | |

## 17 Packing Information

| Orderable Device | Status | Package Type | Pins | Package Qty | Eco Plan | Lead/Ball Finish | MSL Peak Temp | Op Temp ($^0$C) | Device Marking |
|---|---|---|---|---|---|---|---|---|---|
| BV6810AW | ACTIVE | WLCSP | 12 | 3,000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-1 YEAR | -40 to 85 | 6810A |

1. The status is to reflect current situation in marketing.
   ACTIVE: The product currently is on sale.
   LAST TIME BUY in EOL: Bravotekcorp announced this product will be discontinued. Only last time buy supported within a half of a year.
   SAMPLES BY REQUEST: The product is still in developing. Samples may or may not be available.
   OBSOLETE: Bravotekcorp has terminated the production of this product.

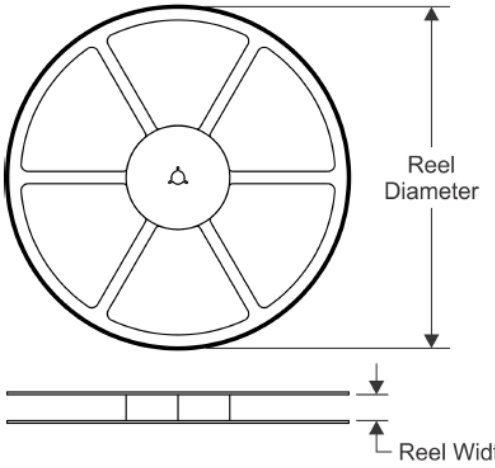
2. Green: Bravotekcorp defines that the product follow JS709B low halogen requirements of <= 1,000 ppm.
   RoHS: Bravotekcorp defines that the product follows current EU RoHS requirements.

3. MSL, Peak Temp.: The Moisture Sensitivity Level rating was based on JEDEC industry standard classification, and peak solder temperature.

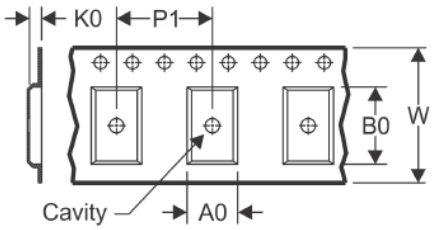
4. Device marking: The device marking of the product will follow Bravotekcorp's marking rule that may contain multiple information for tracing.

## 18 Tape and Reel Information

REEL DIMENSIONS

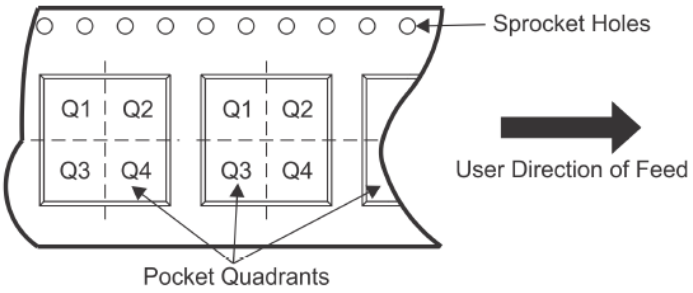



TAPE DIMENSIONS



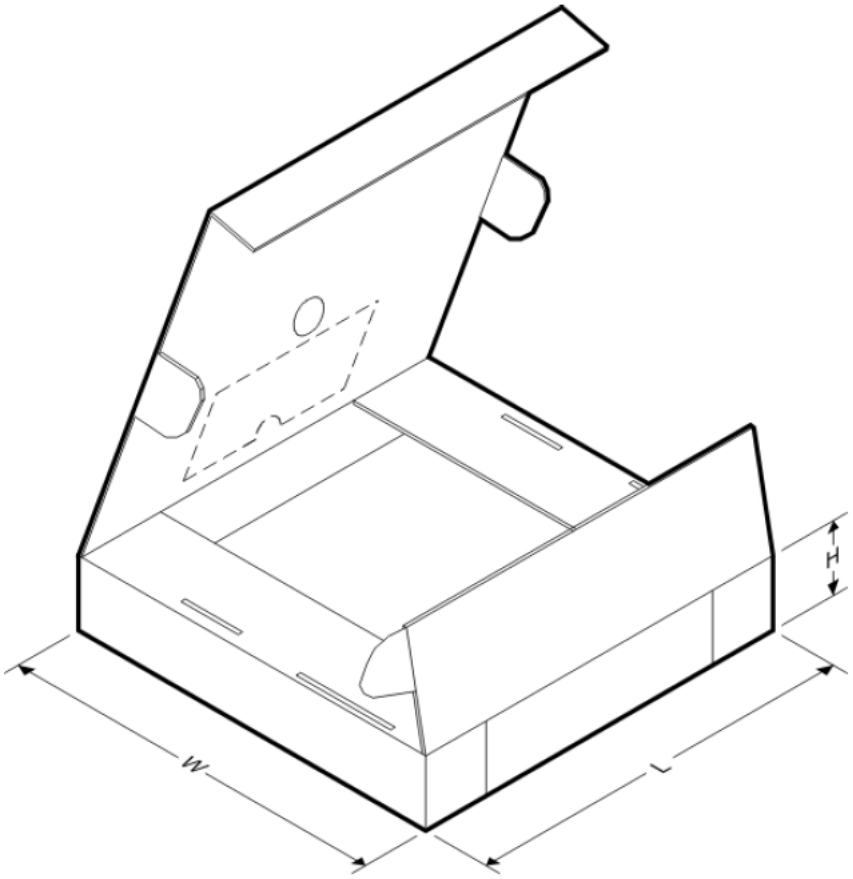

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




| Device | Package Type | Pins | SPQ | Reel Diameters (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BV6810AW | WLCSP | 12 | 3000 | 180 | 9 | 1.57+/-0.05 | 1.81+/-0.05 | 0.77+/-0.05 | 4 | 8 | Q1 |

## 19 Tape and Reel Box Dimension




| Device | Package Type | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| BV6810AW | WLCSP | 12 | 3000 | 183+/-5 | 183+/-5 | 85+/-5 |

## 20 VERSION HISTORY

| Version # | Implemented By | Revision Date | Approved By | Approval Date | Reason |
|---|---|---|---|---|---|
| 0.1 | Elvie | 03.15.2024 | | | Initial Design Definition |
| 0.2 | Elvie | 04.02.2024 | | | Add<br>. $I_{AVDD\_LIMIT}$ 20(Typ)<br>Modify<br>. $I_{OCP}$ 1.05➞1.15(Max)<br>. LX Slew rate Control -Pulse 3 ➞Pulse 5 (Default) |
| 0.3 | Elvie | 04.15.2024 | | | Change capacitor Component supplier<br>. C1, C2, C5, C7, C3-C4CL05A106MP5NRNC(10uF/10V)➞GRM155R60J106ME15D (10uF/6.3V)<br>. C6-CL05A105KP5NFN(1uF/10V) ➞GRM153R60J105ME15D(1uF/6.3V)<br>. C3, C4-GRM158R61A226ME15D(22uF/10V)➞GRM158R60J226ME01D(22uF/6.3V) |
| 0.4 | Elvie | 04.23.2024 | | | Add a Description for the Note in Chapter 5 - Application Circuit |
| 0.5 | Elvie | 05.11.2024 | | | . Change PIN- AVIN to PVIN.<br>. Change in part number and specifications of C6 GRM153R60J105ME15D➞ GRM033R60J104KE19D |

Template Version: 09/09, 2019