Triple Output for AMOLED Bias

General Description

TRP8715 is a highly integrated chip, including two LDOs (one channel for OVDD and one channel for OVSS) and negative charge pump which generates negative output voltage. With its input voltage range of 2.9V to 5.5V, TRP8715 is optimized for products powered by single-cell battery and provides maximum output current up to 50mA.

TRP8715 is available in UQFN-12L 2.5mmx2.5mm package to achieve optimized solution for PCB space.

Features

- **2.9V to 5.5V Supply Voltage Range**
- **OVDD Positive Voltage Output 2.8V to 3.3V**
- **OVSS Negative Voltage Output -2.8V to -3.3V**
- **OVDD Maximum Output Current 70mA**
- **OVSS Maximum Output Current 50mA**
- **Built-in Soft-Start**
- **Programmable Output Fast Discharge Function**
- **High Impedance Output when IC Shutdown**
- **UVLO, OCP, SCP, OTP Protection**
- **Shutdown Current < 1μA**
- **Available in 12-L QFN Package**

Applications

- AMOLED Bias in Portable Device

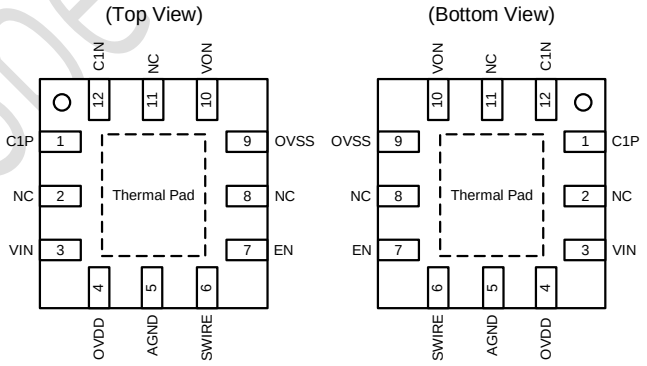
Ordering and Marking Information

Part No.	Package Marking	Package Type
TRP8715AD-33UQN-CT	TA2 XXXXX YWWD	UQFN-12L
TRP8715BD-33UQN -CT	TB2 XXXXX YWWD	
TRP8715BD-30UQN -CT	TB4 XXXXX YWWD	

TRP8715□□ – □□UQN – CT

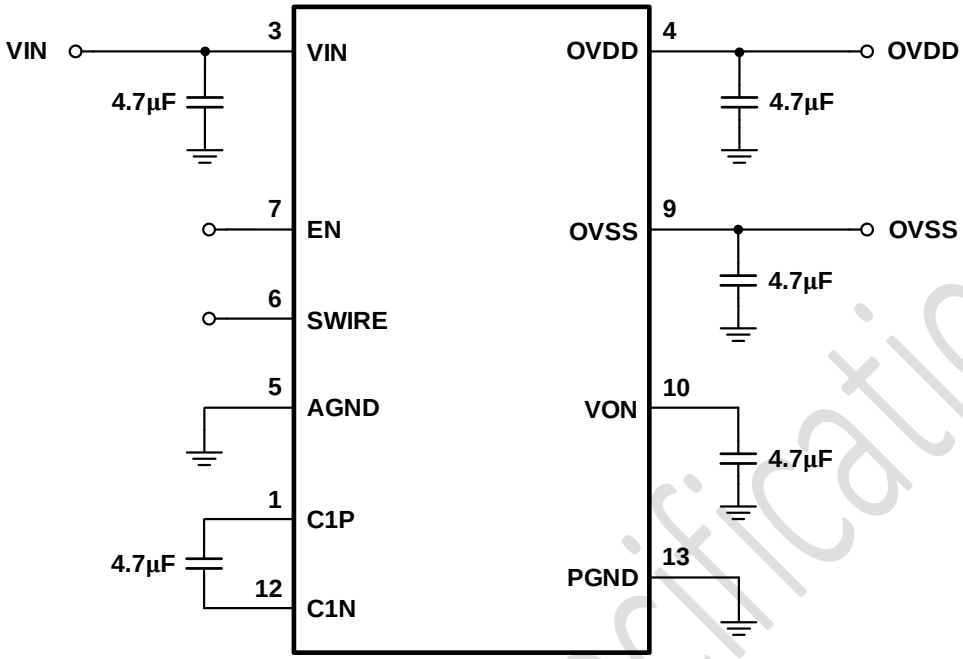
- Packing Type : C : Consumer, T : Tape & Reel
- Package Tape : UQN : UQFN-12L
- Output Voltage : 33 : OVDD = 3.3V, OVSS = -3.3V; 30 : OVDD = 3.0V, OVSS = -3.0V; 28 : OVDD = 2.8V, OVSS = -2.8V
- Fast Discharge Function : D : Disable, E : Enable
- Output Voltage Headroom Control : A : Disable, B : Enable
- Part Number : TRP8715

Pin Configurations



UQFN-12L 2.5mmx2.5mm

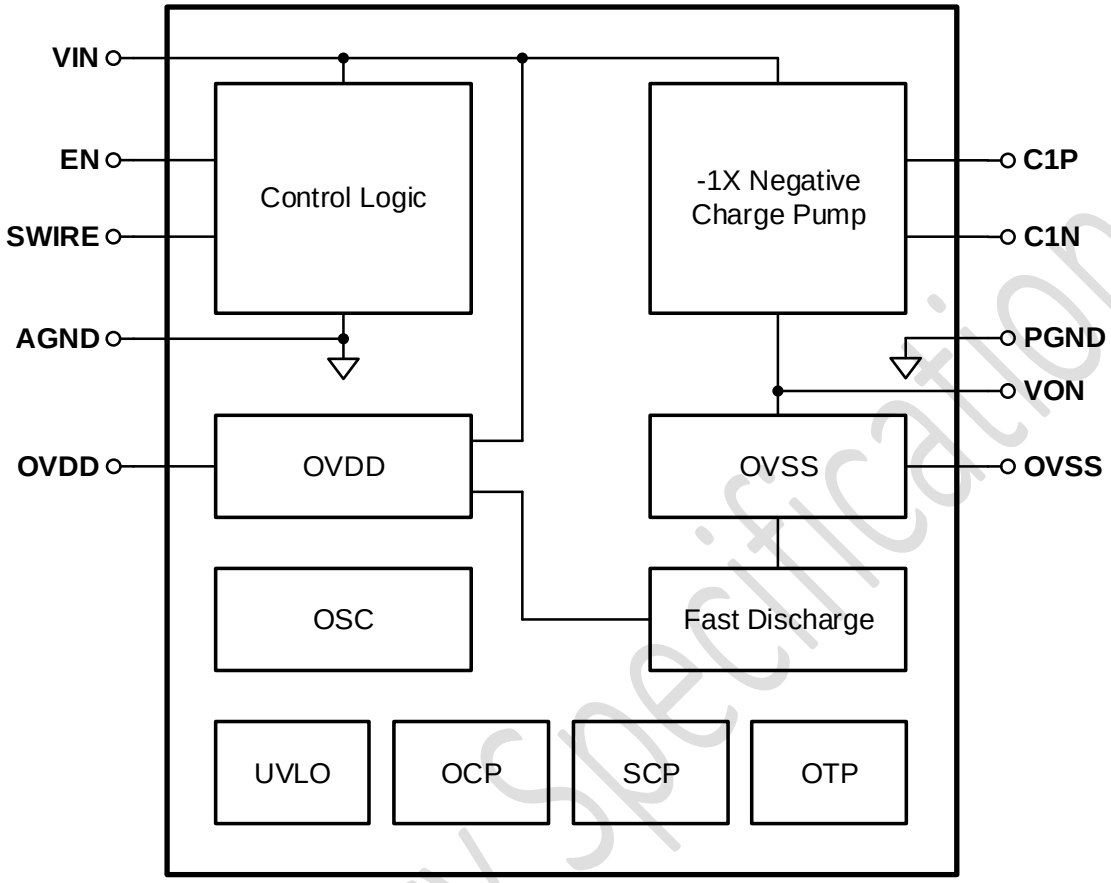
Typical Application Circuit



Functional Pin Description

Pin No. UQFN-12L	Pin Name	Pin Function
1	C1P	Positive Connection for Negative Charge Pump Flying Capacitor
2	NC	
3	VIN	Power Supply Input
4	OVDD	Positive Output Voltage for OLED Bias
5	AGND	Analog Ground
6	SWIRE	AOD Mode Setting
7	EN	Enable Output Channels
8	NC	
9	OVSS	Negative Output Voltage for OLED Bias
10	VON	Negative Charge Pump Output
11	NC	
12	C1N	Negative Connection for Negative Charge Pump Flying Capacitor
13/Thermal Pad	PGND	Power ground.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage VIN to GND ---------- –0.3V to 6V
- Input Signal EN, SWIRE to GND ---------- –0.3V to (VIN + 0.3V)
- Output Voltage OVDD, C1P to GND ---------- –0.3V to 6V
- Output Voltage OVSS, VON, C1N to PGND ---------- –6V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C

  QFN-12L 2.5x2.5 ---------- W
- Package Thermal Resistance, θ_{JA} (Note 2)

  QFN-12L 2.5x2.5 ---------- °C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 3kV

  MM (Machine Mode) ---------- 300V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- VOUT+0.2V to 5.5V
- Ambient Temperature Range, T_A ---------- –40°C to 85°C
- Junction Temperature Range, T_J ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN}=3.7V, V_{OVDD}=3.3V, V_{OVSS}=-3.3V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage Range	V_{IN}		2.9	-	5.5	V
Under Voltage Lockout Threshold Voltage	V_{UVLO_H}	V_{IN} rising	2.5	2.6	2.7	V
	V_{UVLO_HYS}	V_{IN} hysteresis	-	400	-	mV
Over-temperature Protection	T_{OTP}		-	140	-	°C
Over-temperature Protection Hysteresis	T_{OTP_HYST}		-	20	-	°C
Shutdown Current	I_{SHDN}	EN = low, SWIRE = low	-	-	1	μA
Quiescent Current	I_Q	V_{IN} = 3.7V, EN = high, SWIRE = low, and no load	-	30	-	μA
EN Logic-High	V_{IH}		1.2	-	VIN	V
EN Logic-Low	V_{IL}		0	-	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Pull down Resistor	R_{PD_EN}		-	1	-	MΩ
OVDD						
Output Voltage Range	V_{OVDD}		-	3.3	-	V
Output Voltage Accuracy	$OVDD_{\_ACC}$	OVDD = 3.3V, I_{OVDD} = 1mA	-0.5	-	0.5	%
Output Current Capability	I_{OVDD_MAX}	V_{IN} = 3.5V to 5.5V V_{OVDD} = 3.3V, V_{OVSS} = -3.3V	70	-	-	mA
Output Current Limit	I_{OVDD_LIM}		-	100	-	mA
Line Regulation	$OVDD_{\_LINE}$	V_{IN} = 3.5V to 5.5V, V_{OVDD} = 3.3V, V_{OVSS} = -3.3V, I_{OVDD} = 50mA	-	10	-	mV
Load Regulation	$OVDD_{\_LOAD}$	V_{OVDD} = 3.3V, V_{OVSS} = -3.3V, I_{OVDD} = 1mA to 50mA	-	10	-	mV
Output Voltage Ripple		V_{IN} = 3.7V, V_{OVDD} = 3.3V, I_{OVDD} ≤ 30mA V_{OVSS} = -3.3V, I_{OVSS} ≤ 30mA	-	-	10	mV
Under Voltage Protect Voltage	V_{UVP_OVDD}		-	0.8 * V_{OVDD}	-	V
Duration to UVP Trigger Time	t_{UVP_OVDD}		-	1	-	ms
Fast Discharge Resistance	R_{OVDD_DISC}		-	70	-	Ω
Soft Start Time	t_{SS_OVDD}		-	2	-	ms
Negative Charge Pump						
Switching Frequency	f_{SW}		-	1.0	-	MHz
VON Maximum Load Current	I_{VON_MAX}	V_{OVDD} = 3.3V, V_{OVSS} = -3.3V	50	-	-	mA
OVSS						
Output Voltage Range	V_{OVSS}		-	-3.3	-	V
Output Voltage Accuracy	$OVSS_{\_ACC}$	OVSS = -3.3V, I_{OVSS} = 1mA	-1	-	1	%
Output Current Capability	I_{OVSS_MAX}	V_{IN} = 3.5V to 5.5V, V_{OVDD} = 3.3V, V_{OVSS} = -3.3V	50	-	-	mA
Output Current Limit	I_{OVSS_LIM}		-	100	-	mA
Line Regulation	$OVSS_{\_LINE}$	V_{IN} = 3.5V to 5.5V, V_{OVDD} = 3.3V, V_{OVSS} = -3.3V, I_{OVSS} = 50mA	-	10	-	mV
Load Regulation	$OVSS_{\_LOAD}$	V_{OVDD} = 3.3V, V_{OVSS} = -3.3V, I_{OVSS} = 1mA to 50mA	-	10	-	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Ripple		V_{IN} = 3.7V, V_{OVDD} = 3.3V, I_{OVDD} ≤ 30mA V_{OVSS} = -3.3V, I_{OVSS} ≤ 30mA	-	-	10	mV
Under Voltage Protect Voltage	V_{UVP_OVSS}		-	0.4 * V_{OVSS}	-	V
Duration to UVP Trigger Time	t_{UVP_OVSS}		-	1	-	ms
Fast Discharge Resistance	R_{OVSS_DISC}		-	70	-	Ω
Soft Start Time	t_{SS_OVSS}		-	2	-	ms
Logic Input (SWIRE)						
SWIRE Input High Voltage	V_{IH}		1.2	-	V_{IN}	V
SWIRE Input Low Voltage	V_{IL}		0	-	0.4	V
SWIRE Pull down Resistor	R_{PD_SWIRE}		-	750	-	kΩ

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at TA = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Power Sequence

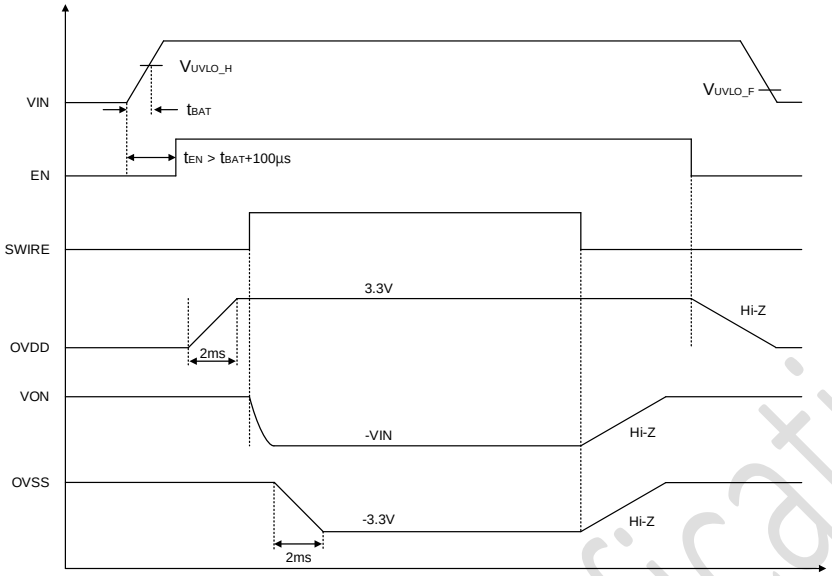


Figure 1. Power ON/OFF Sequence without Fast Discharge Function

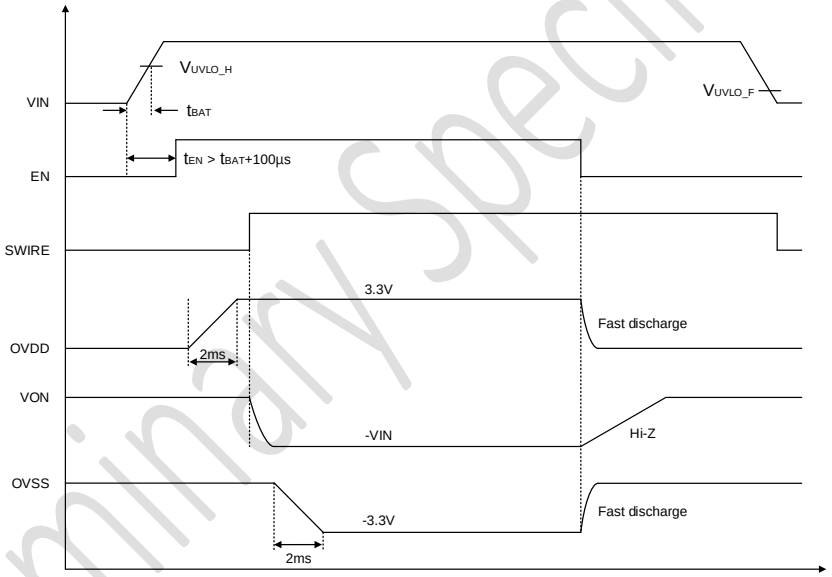


Figure 2. Power ON/OFF Sequence with Fast Discharge Function

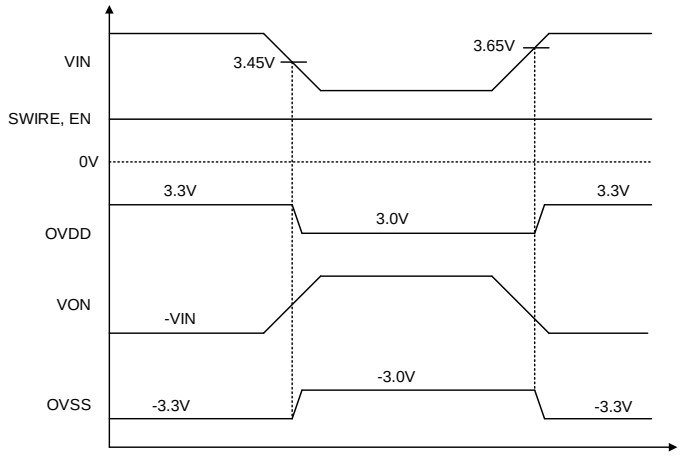


Figure 3. Output Voltage Headroom Control Function

Application Information

General Description

The TRP8715 is a highly integrated LDO and negative charge pump to generate positive and negative output voltages for driver and AMOLED bias. It can support input voltage range from 2.9V to 5.5V and the output current up to 50mA. The OVDD positive output voltage is generated from the LDO supplied from VIN, and OVDD is set at a typical value of 3.3V. The VIN also drives a negative charge pump controller to generate VON negative output voltage. The OVSS negative output voltage is generated from the LDO supplied from negative charge pump, and OVSS is set at a typical value of -3.3V.

Input Capacitor Selection

VIN input ceramic capacitor with 4.7μF capacitance is suggested for applications. For better voltage filtering, need to select ceramic capacitors with low ESR, X5R and X7R types are suitable because of their voltage and thermal range.

Output Capacitor Selection

The output capacitor selection determines the output voltage ripple and transient response. It is recommended to use ceramic capacitors placed as close as possible to output and GND pins of the IC.

Under Voltage Lockout

The prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included which shuts down IC operation when input voltage is lower than the specified threshold voltage.

Under Voltage Protection (UVP)

To prevent any abnormal condition to damage the panel system, TRP8715 employees UVP protection in all 2 LDOs. As soon as the output drops below 40% of V_{OVDD} or 40% of V_{OVSS}, TRP8715 will enter shutdown mode. After UVP, TRP8715 can normal operation by toggling EN pin and VIN UVLO

Short Circuit Protection (SCP)

The TRP8715 has a short-circuit protection mechanism which prevents damage the device.

Shutdown Mode

TRP8715 will enter shutdown mode and only consume 1μA of input current when EN and SWIRE pins are driven to Low. Therefore, system controller can save the battery power consumption by force TRP8715 into shutdown mode when display is allowed to be off.

Standby Mode

TRP8715 will enter standby mode when SWIRE pin is driven to Low. Therefore, system controller can save the battery power consumption by force TRP8715 into standby mode when display is allowed to be into Always On Display mode (AOD).

Over Temperature Protection

The TRP8715 equips an over temperature protection circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down the bias operation when junction temperature exceeds 140°C. Once the temperature cools down by approximately 20°C, IC will automatically resume normal operation. To maintain continuous operation.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For QFN-12L package, the thermal

resistance, θ_{JA}, is °C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C - 25°C) / (°C/W) = W

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}.

Layout Consideration

For the best performance of the TRP8715, the following PCB layout guidelines should be strictly followed.

- For good regulation, place the power component as close to the IC as possible. The traces should be wide and short especially for the high current output loop.
- The input and output bypass capacitor should be placed as close the IC as possible and connected to the ground plane of the PCB.
- The flying capacitor should be placed as close to the C1P/C1N pin as possible to avoid noise injection.
- Disconnect AGND and PGND pins on top layer under the device and then PGND is connected to the ground plane at bottom layer through the via.
- VIN and OVDD capacitors should be connected to PCB ground plane.
- VON and OVSS capacitors should be connected to PCB ground plane.

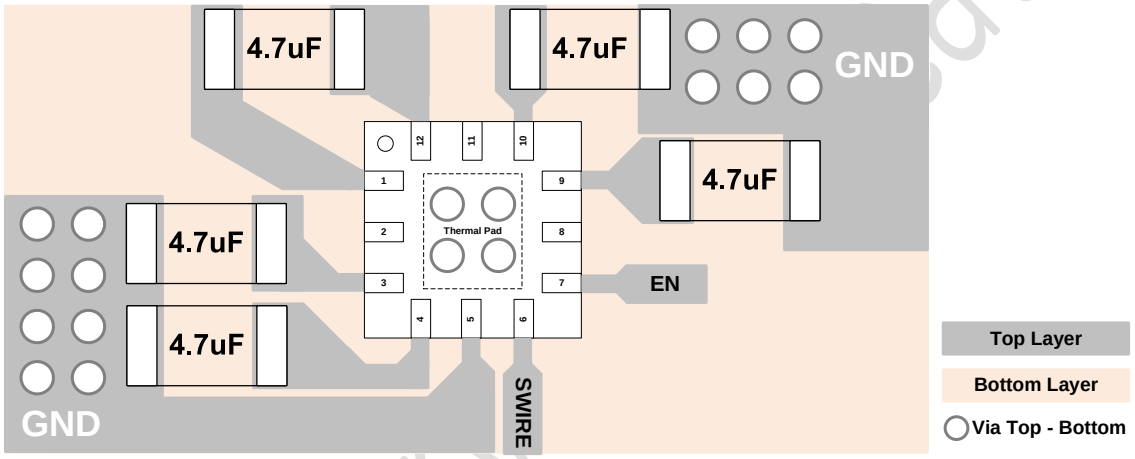
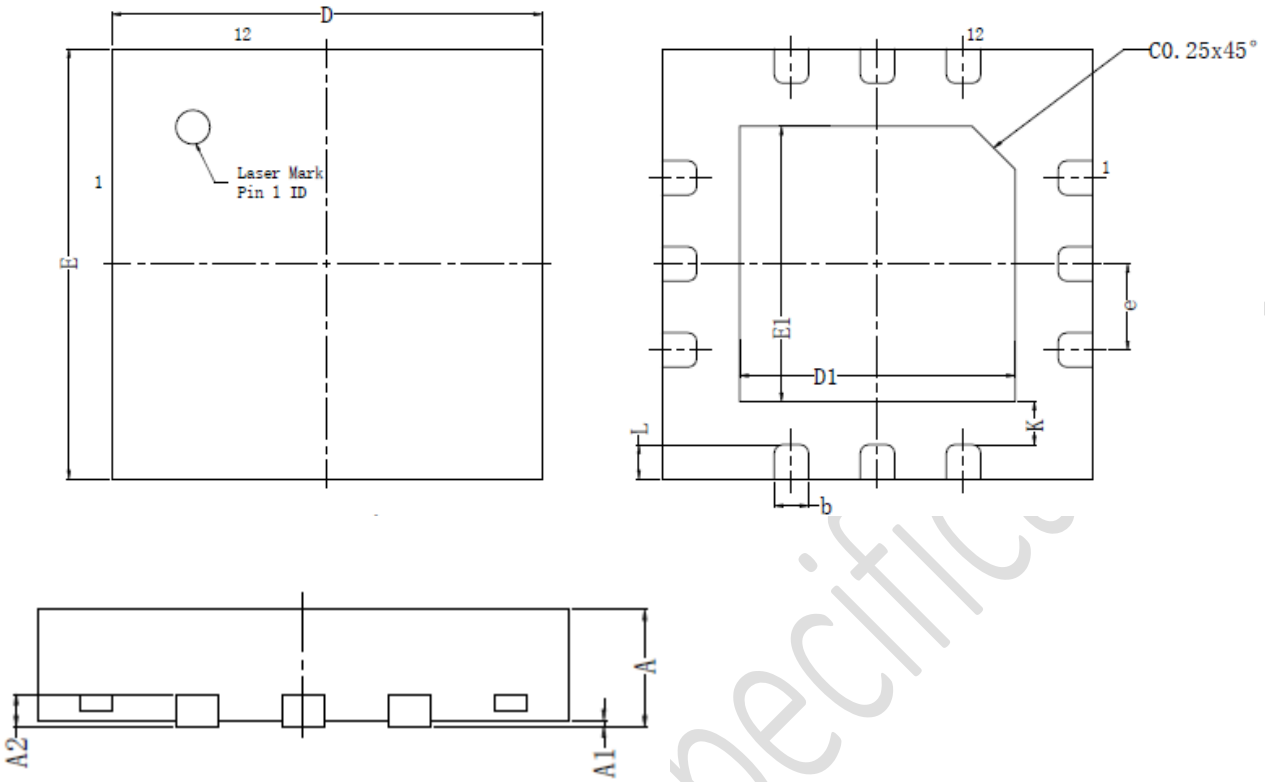


Figure 3. Layout Guide

Outline Dimension



UQFN-12L Package

Symbol	Dimensions In Millimeters		
	MIN.	TYP.	MAX.
A	0.50	0.55	0.60
A1	0.00	-	0.05
A2	0.152 REF		
b	0.15	0.2	0.25
D	2.40	2.50	2.60
D1	1.50	1.60	1.70
E	2.40	2.50	2.60
E1	1.50	1.60	1.70
e	0.50 BSC		
k	0.25 REF		
L	0.10	0.20	0.30