Djat/Leonard Bong

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Competency

- CAD automation flow for Cadence CAD tools and Synopsys CAD tools (20+ years)
- Unix/Linux system (25 years of experience)
- Shell scripts (25 years of experience)
- Java and Javascript (2 years of experience)
- Language C (25 years of experience), C++ (2 years of experience)
- Tcl/TK scripting (20 years)
- Python/PyQt scripting (3 years)
- Perl scripting (5 years)
- Angular 2 / Typescript
- HTML, CSS, REST API
- NoSql Splunk
- RDBMS (SQL, Oracle, Sybase) (15 years of experience)
- Excellent communication and enjoy team work
- Proactive to provide/suggest solutions and/or enhancement

Note:

I am taking time off between Jan 2018 (After the contract with Intel) until Now

Professional Summary

Online Classes

- **100 Days of Code – The complete Python Pro Bootcamp 2021 (On Going)**
  - IDE: PyCham
  - Python lists
  - Python dictionaries
  - Flow Control
  - Object Oriented Programming
  - Graphics with Turtle package
  - Manipulating CVS file with Pandas Package
  - Manipulating json file with json madules
  - Build GUI interface with tkinter package
  - Handling Exception
  - Sending email with sms interface
  - Work with interface with API with HTTP Request modules (Get, Post, Put and Delete requests, receive response, create json file)
  -

Senior Software Engineer (Altera/Intel)

- **Contractor at Altera/Intel (Sept 04, 2017 – Jan 2018)**
    - IDE: Visual Studio
    - Worked on Dashboard application using Angular 2/ Typescript, REST API, HTML, CSS and NoSQL Splunk

Senior software engineer

- Architected, designed, and implemented physical design verification flow for ASIC design by integrating design tools from Synopsys and Cadence to meet IC design team specific needs.
- Architected, designed, and implemented memory compiler software for memory design team as an in house tool
- Implemented backend manufacturing flow for scribe-line, reticle, wafer maps, and generation of stepper job to drive the stepper machine for 8" and 10" wafer.
- Managed a team of software engineers to design wire bonding and flip chip manufacturing flow.
- Side Job
    - IDE: Visual Studio
    - Join HNL-Ventures developing software tools for predicting stock market on Windows 7 using C, MySQL, php and python. Responsible for setting up and maintaining Database using MySQL.
- Core competency
    - C language, Perl, TCL/TK, Python/QT, Csh Scripting, SQL (Sybase, Oracle, MySQL)
    - Linux/Unix, Windows

Experience

Software Engineer

HNL Ventures (June 2010 – August 2017)

- **Part time (Side work)** for HNL Ventures, a startup company in the stock market field.
    - Environment – Window 7
    - Visio Studio
    - Language – C, Python, Java and javascript for UI
    - RDBMS -- MySQL

Principal Software Engineer

Oracle (November 2013 – January 2015 (1 year 3 months) – Santa Clara, CA

- Backend verification flow for deep sub-microns processes
    - Implemented Re-Tape-out Flow for 20NM process node using Mentor Graphics Calibre verification tool.
        - Environment – Linux
        - Language – TCL/TK
        - RDBMS -- MySQL
    - * Implemented Cut OD Flow for 16NM process node in Mentor Graphics Calibre verification tool.
        - Environment – Linux
        - Language – TCL/TK
        - RDBMS -- MySQL
    - * Implemented queuing system in "Inter-active" Graphical User Interface tool, where the tool will maintain multiple submitted verification jobs in queue and dispatch them

one at a time to avoid using multiple Calibre's licenses, and to avoid overlapping of output.
    - Environment -- Linux
    - Scripting – c shell to invoke command/external program in the tcl codes
    - Language -- TCL/TK
    - RDBMS -- MySQL
- Support, Maintain, and Enhancing GDS Application
    - Environment -- Linux
    - Language -- C, C++
    - Scripting – c shell to get user's input and to tie the flow together

Sabbatical Leave

- Jan 2015 – Now
- Part time work with HNL-Ventures/Seegnals
    - Environment – MS-Dos, MS Visual Studio
    - Language – C, PHP, Perl
    - Database - MySQL

Sr. Software CAD Engineer

Texas Instruments (July 2011 – July 2013 (2 years 1 months) – Santa Clara, CA

- Collaborated with R&D group to design, develop and QA the tool for transformer/inductor optimization and synthesis tool using mathematical equation based to calculate the inductance value given other physical parameters (i.e. metal width trace, metal spacing trace, and number of turns) and vice versa for fast turn-around prototyping, before running actual simulation. The tool was written in Python and Qt4 with graphs comparison for various results.
    - Environment -- Linux
    - Language -- Python & PyQT4

- Took over existing Memory Compiler software created by TI software team and collaborated with memory designers to enhance the tool to support additional EDA views (Mixed Signal Verilog, Cadence EPS for IR Drop analysis) for IC design digital tools flow.
    - Environment -- Linux
    - Language -- C, Perl
    - RDBMS -- MySQL

Software CAD Engineering Manager

National Semiconductor (August 1984 – July 2011 (26 years 10 months) – Santa Clara, CA

- Collaborated with memory designers to design, architect and develop "Memory Compiler" software which has the capabilities to generate various design views, such as layout in GDS and Cadence CDB and OADB, Schematic, EPS, LEF, CDL Netlist, Datasheet, Liberty, Timing verilog, Milkyway, and interface to Synopsys P&R tool for verification
    - Environment -- Linux
    - Language -- C, hiDB scripting (Internal language, similar to TCL)
    - Scripting – TK/Tcl, C shell (as top level user interface and invokes various programs between the flow)

- Project leader to develop "Reticle Generation" system tool by collaborating with multiple fabrication sites and mask making group to define the specification, and worked with remote

site software group to design, implement and QA the system which has the following capabilities:
    - Creates scribe-line with and without test patterns according to each fab site's spec.
    - Creates optimum reticle with maximum number of dies with and without test pattern according to each fab site's spec.
    - Creates optimum wafer map with maximum number of dies and less steps to maximize the stepper machine through put.
    - Creates stepper job control deck that can be feed directly to the stepper machine.
    - Create Mask Order Form
    - Using Sybase's RDMBS as the back-bone database to store the data where the fab's operator can down load the information from.
    - Environment -- Linux
    - Language -- C, TCL/TK, C shell (to control the flow to invoke various EDA tools)

- Project leader to develop "TapeOut Cockpit tool" that run final verification flow (such as DRC, ERC, Soft-Check, LVS for both Cadence Assura and Synopsys Hercules tools) on a design before mask-making process, according to each process technology's verification flow to ensure the design is verified and meet technology design rules. The process design rule is provided by process design engineer and captured/stored in Oracle RDBMS.
- Managed a team of CAD engineers to develop standard cell library characterization flow.
- Managed a team of CAD engineers to develop front-end IO library cell checker.
    - Environment -- Linux
    - Language -- C, TCL/TK, C shell (to control the flow to invoke various EDA tools)

Proficient

- Environment
    - Linux/Unix
    - Microsoft Windows 7
        - Visual Studio
- Software programming language
    - C
- Scripting Language
    - TCL/TK, Python, Qt4, Shell script, Java, PHP, Cadence's skill language(training)
    - HTML, CSS, JavaScript programming
    - Angular 2 / Typescript
- Database
    - RDBMS (Sybase, Oracle, mySQL)
    - Splunk (NoSQL)
- Revision Control
    - Perforce
    - Vcs

Notes

- I am currently using PHP, Python, SQL, and C in my current project with HNL Venture

Education

BS Computer Science
January 1980 – April 1982
Central Michigan University

MS Computer Science
August 1982 – December 1983
Central Michigan University