COMPARC **3rd Term 2017-2018**

Case Project

INTRODUCTION

In this case project, you will implement a simulator for a simplified MIPS64 processor, μMIPS. The μMIPS processor offers the following subset of MIPS64 instructions:

Common instructions: LD, SD, DADDIU, DADDU, SLT, NOP, BC

Group 1: BLTZC/AND; Group 2: BGEZC/OR; Group 3: BGTZC/XOR; Group 4: BLTC/DSUBU;
Group 5: BGEC/DAUI; Group 6: BEQC/DAHI; Group7: BNEC/DATI; Group 8: BEQZC/DSLLV
Group 9: BNEZC/DSRAV

The μMIPS processor is based on the MIPS64 architecture.

The objective this project is to "execute" the program

Besides the first module which you have already done the following:

1. Utility program to input the MIPS program.
2. Generate the equivalent opcode of the MIPS program (in HEX)
3. Perform error checking and generate the appropriate error message

On the **second** module, you will add the following:

1. Graphics User Interface (GUI) with the following output screen:
    a. Output screen #1: the equivalent opcode of the MIPS program (in HEX)
    b. Output screen #2: Error message screen
    c. Output screen #3: Registers R0 to R31
    d. Output screen #4: Memory with range form **0000-FFFF** for data and **1000-1FFF** for instruction
    e. Output screen #5: the internal MIPS64 registers as follows:
    IF Cycle: IF/ID.IR, IF/ID.PC
    ID Cycle: ID/EX.IR, ID/EX.A, ID/EX.B, ID/EX. IMM
    EX Cycle: EX/MEM.IR, EX/MEM.ALUOUTPUT, EX/MEM.B, EX/MEM.cond
    MEM Cycle: MEM/WB.IR, MEM/WB.ALUOUTPUT, MEM/WB.LMD, actual memory affected
    WB Cycle: Registers affected (see letter c)
2. Utility program to input value for registers R1 to R31
3. Utility program to input value for memory (data segment). Note: the data segment is from **0000-0FFF**.
4. The equivalent opcode of the MIPS program should also be stored in memory starting at address **1000.**
5. Provide a "GOTO Memory" option to go to target memory location

Note: Upload source code on CANVAS: Filename: MOD2??.* (where ?? is the group number and * is the appropriate extension. Example: MOD201.java (for group 1)

Deadline: July 17, 2018 (Tuesday), demo during class-time