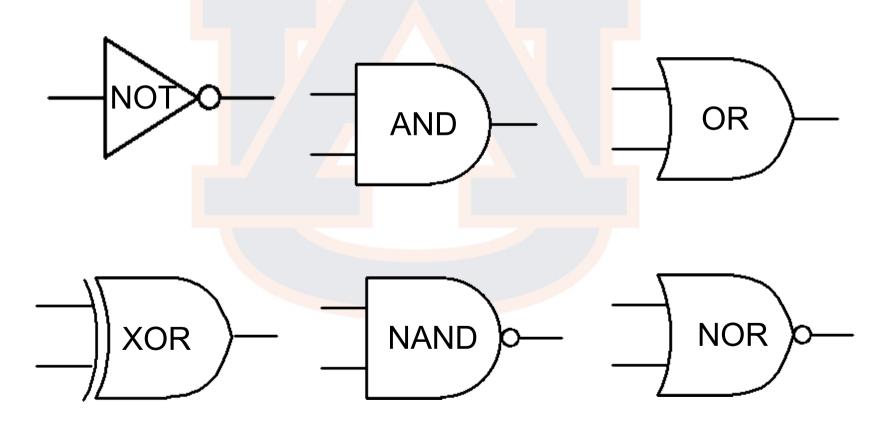
Digital Logic Circuits 'Circuit Diagrams' ELEC2200 Summer 2009

David J. Broderick brodedj@auburn.edu http://www.auburn.edu/~brodedj Office: Broun 360



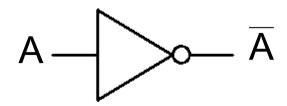
Circuit Diagrams

 Let's employ our design techniques and draw the corresponding circuit



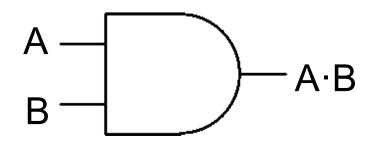


- Complement, Invert,
 Not
- Two notations: A' and
 - A A A 1 0



- And
- Notated as A-B

Α	В	A·B
0	0	0
0	1	0
1	0	0
1	1	1

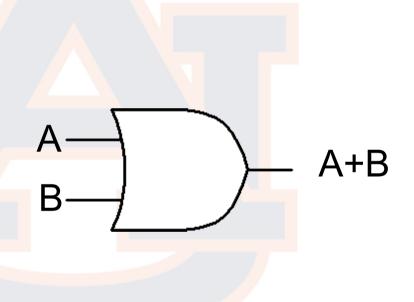




• Or

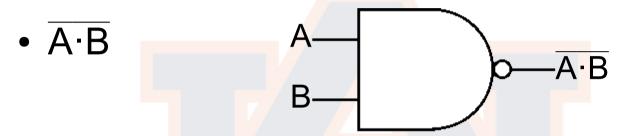
Notated as A+B

Α	В	A+B
0	0	0
0	1	1
1	0	1
1	1	1





NAND

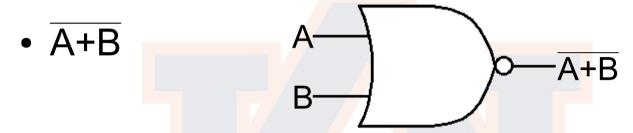


DeMorgan's gives us A·B=A+B

Α	В	A·B	$A \longrightarrow A$
0	0	1	
0	1	1	}————————————————————————————————————
1	0	1	
1	1	0	
			$B \longrightarrow B$



• NOR

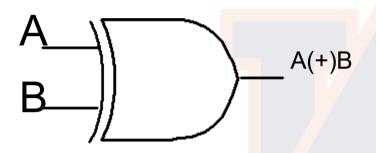


DeMorgan's gives us A+B=A·B

Α	В	A+B	$A \longrightarrow \overline{A}$
0	0	1	
0	1	0	
1	0	0	A·E
1	1	0	
			$B \longrightarrow \overline{B}$

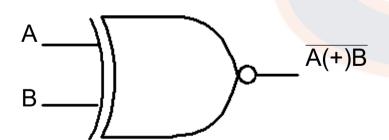


• XOR



4	Α	В	A(+)B	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	

XNOR



Α	В	A(+)B	
0	0	1	
0	1	0	
1	0	0	
1	1	1	



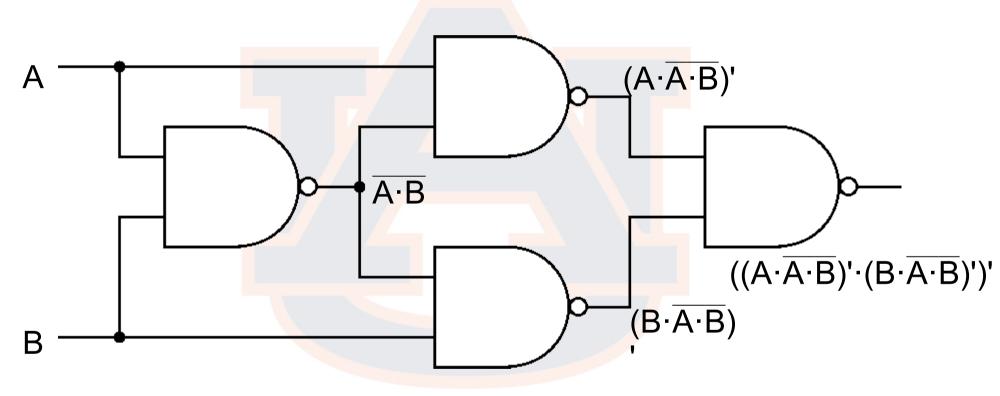
XOR Properties

- XOR has some unique properties
 - Controlled Inverter
 - A(+)0=A
 - $A(+)1=\overline{A}$
 - Invert one XOR input->XNOR
 - $A(+)B=\overline{A}(+)B=\overline{A}(+)B$
 - Invert one XOR input->XNOR
 - $(A(+)\overline{B})'=(\overline{A}(+)B)'=A(+)B$
 - Constant output
 - A(+)A=0
 - $A(+)\overline{A}=1$
- Multiple implementations of XOR possible



XOR Implementations

4 Gates

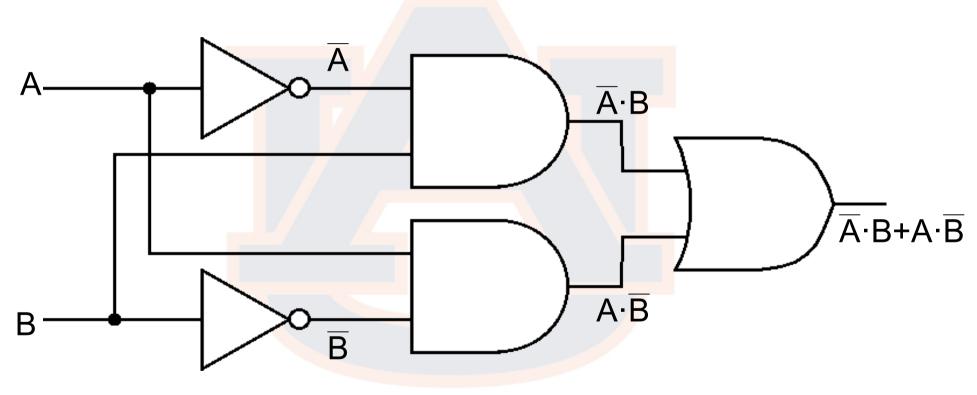


$$((A \cdot \overline{A \cdot B})' \cdot (B \cdot \overline{A \cdot B})')' = A(+)B$$



XOR Implementations

• 5 Gates

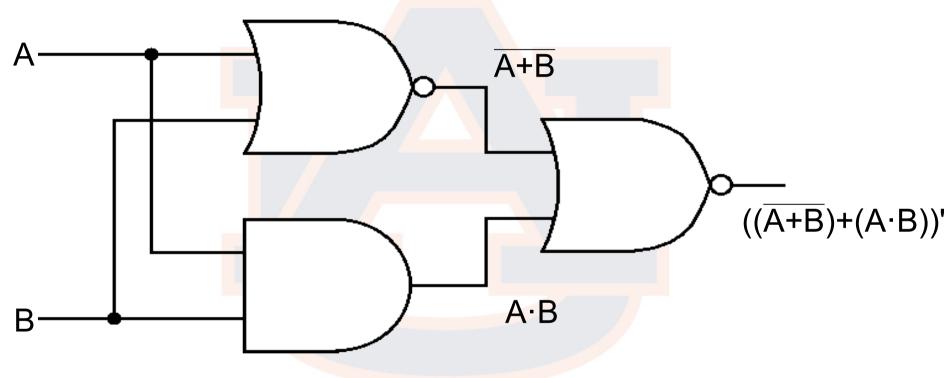


$$\overline{A} \cdot B + A \cdot \overline{B} = A(+)B$$



XOR Implementations

• 3 Gates

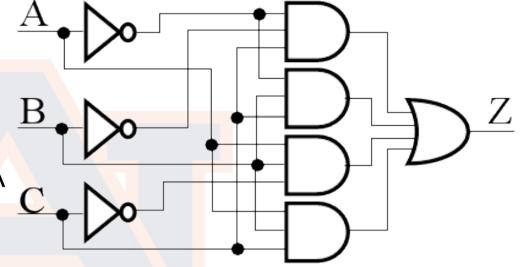


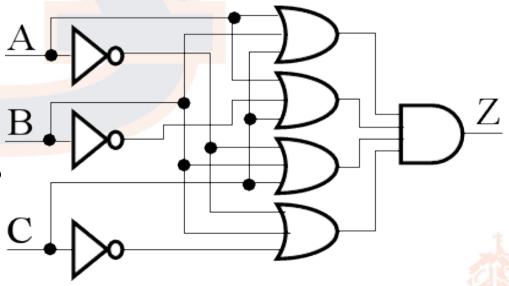
$$((\overline{A+B})+(A\cdot B))'=A(+)B$$



SOP/POS Circuits

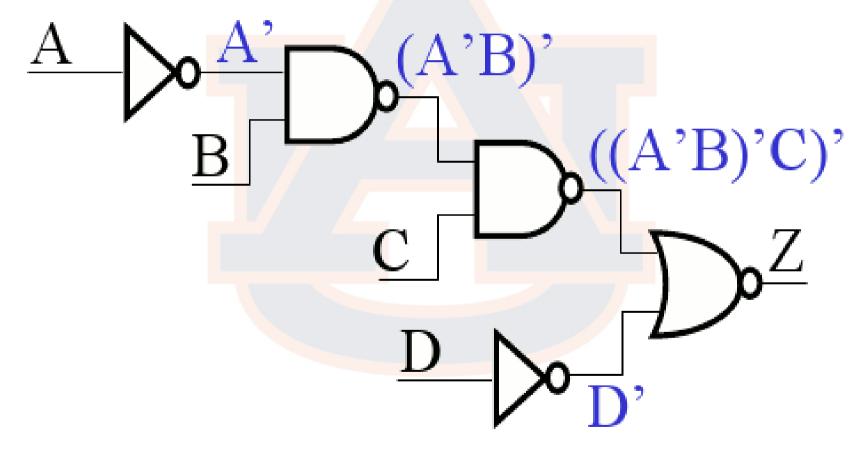
- SOP expressions
 - AND-OR
 - Inverters for complemented literals
 - Z=Ā·B·C+Ā·B·C+A·B·C+A ·B·C
 - 2-level AND-OR logic
- POS expressions
 - OR-AND
 - Inverters for complemented literals
 - $Z=(A+B+C)\cdot(A+\overline{B}+C)\cdot(\overline{A}+B+C)\cdot(\overline{A}+B+\overline{C})$
 - 2-level OR-AND logic





Gate Level Representation

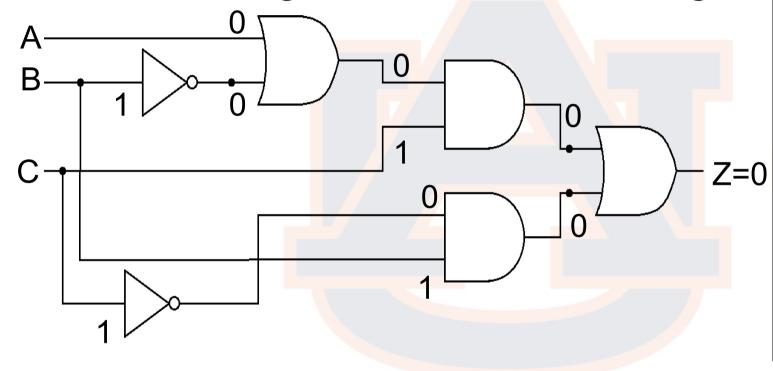
• From $Z=\overline{(((A'\cdot B)'\cdot C)'+D')}$





Circuit Analysis

Recovering truth table from design



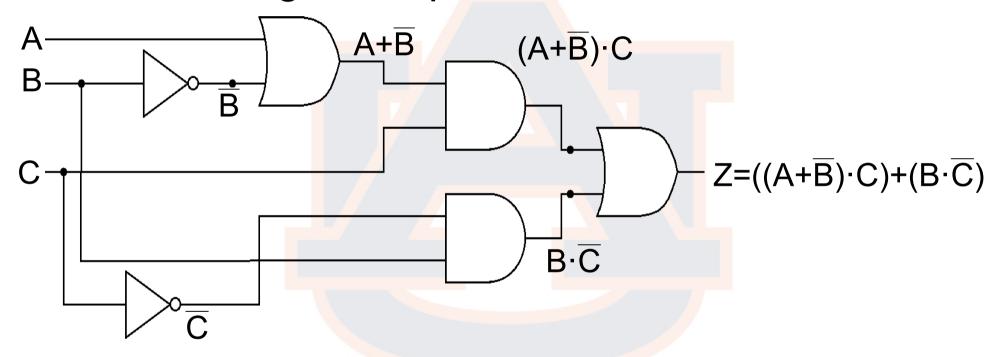
Α	В	С	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	0
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Apply inputs for each row and calculate output



Circuit Analysis

Recovering the expression

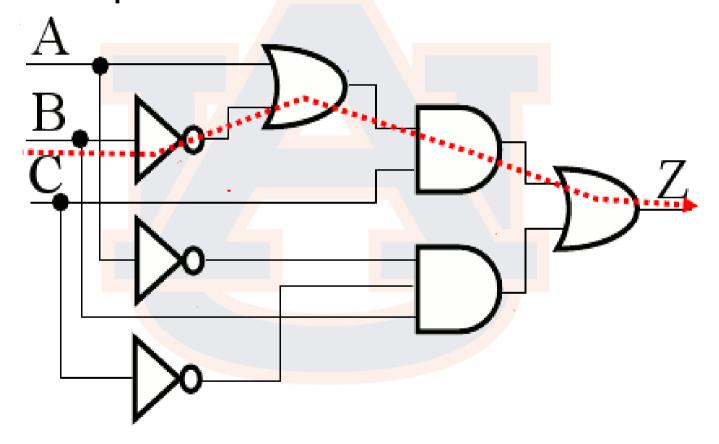


Propagate the expressions from input to output



Circuit Analysis

Find the expression and truth table



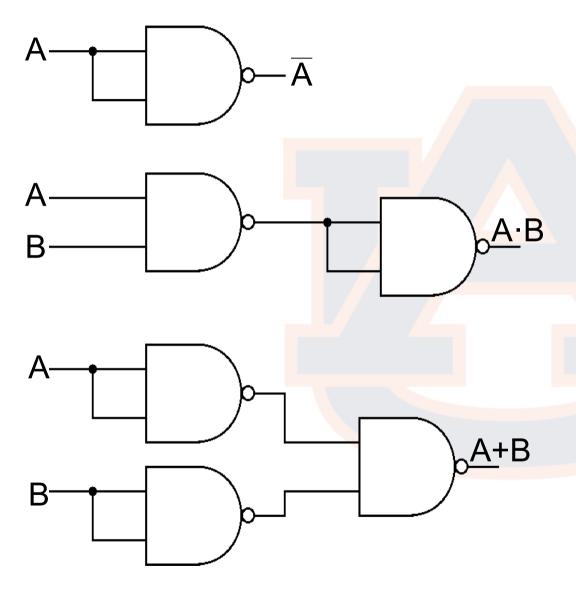


Functionally Complete Sets

- If any digital circuit can be built from a set of gates (types), that set is said to be functionally complete
 - NOT, AND, OR
 - NAND
 - NOR
 - Multiplexers
- If a set can be used to construct NOT, AND, and OR functions it is functionally complete



NAND Logic



- The NAND gate is a functionally complete set
- DeMorgan's needed for OR function
- Same approach can be taken with NOR
- Can build any circuit from NAND gates alone