Circuits Lab 8

Daniel Connolly
William Fairman

April 22, 2019

1 Experiment 1: Voltage Transfer Characteristics

In Experiment 1, we focused on observing the voltage transfer characteristics of a differential amplifier circuit. This involved analyzing the relationship between the input voltage (V_1) and output voltage (V_{out}) while the circuit was in weak and strong inversion: shown in Figure 2 and 3 respectively. We also observed the voltage transfer characteristics at varied gate voltages of the other nMOS transistor (M_2).

1.1 Circuit

The differential circuit shown in Figure 1 was setup to allow us to vary the gate voltage of M_1 and observe the output voltage at the drain of M_2. Voltage dividers were used to set the voltage of both V_b and V_2. To observe the circuit in weak inversion, V_b was set to $.63V$. Strong inversion results were recorded while V_b was set to $1.11V$. For both weak and strong inversion, V_2 was set to $2.49V$, $3.56V$, and $4.51V$.

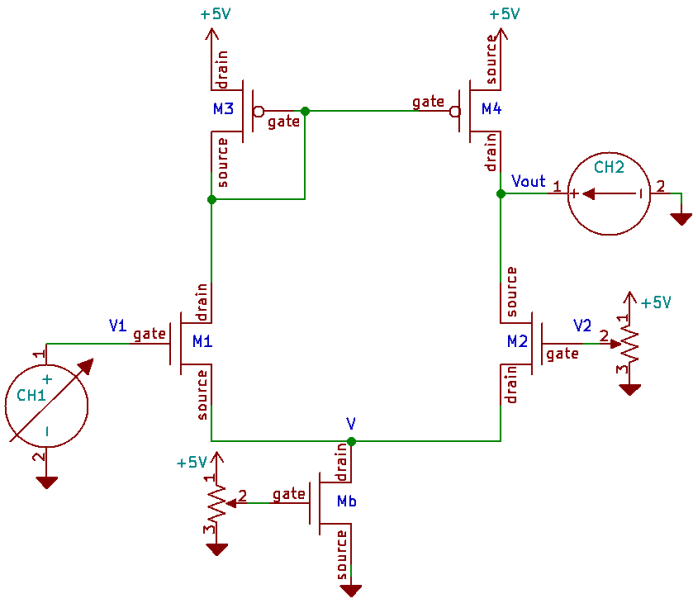

Figure 1: Circuit used to measure the voltage at V_{out} while varying the gate voltage (V_1) of the M_1 transistor.

1.2 Observations

As the voltage transfer characteristics in Figures 2 and 3 demonstrate, the output voltage(V_{out}) of the differential amplifier increases linearly with V_1 once V_1 reaches the threshold voltage and until V_1 is quite close to V_2. The region of linear increase is best explained by the circuit behaving like a source-follower, a concept we will explore in greater depth in the postlab assignment. When $V_1 \approx V_2$, V_{out} quickly jumps and begins to rail at the supply voltage of our circuit ($V_{dd} = 5V$). When the bias transistor is held in weak inversion, as shown in Figure 2, this transition to railing is rather sharp and immediate.

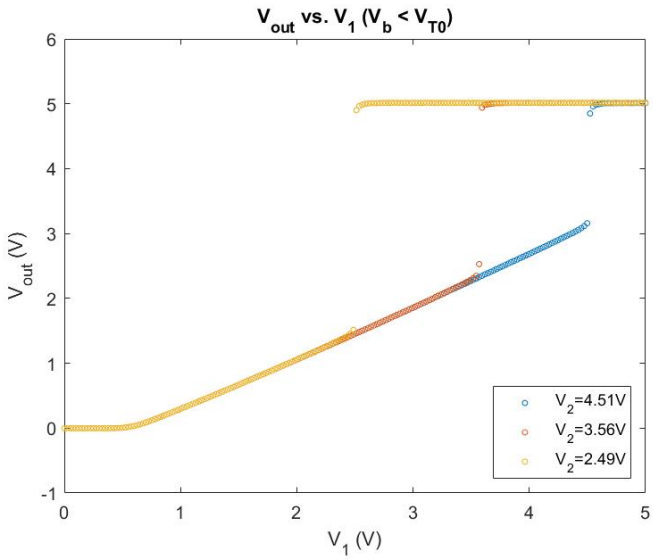

Figure 2: Voltage transfer characteristics for the differential amplifier at three different values of V_2 when the bias transistor is held in weak inversion.

When the bias transistor is in strong inversion, as in Figure 3, the voltage transfer characteristic is nearly the same, except that it approaches the region of high gain more gradually. The fact that V_{out} approaches V_{dd} more gradually can be explained by the fact that the drain characteristics of the MOS transistors move from the ohmic region to saturation and vice versa in a less immediate manner in strong inversion as compared to weak inversion. We will explore this concept more in the postlab assignment.

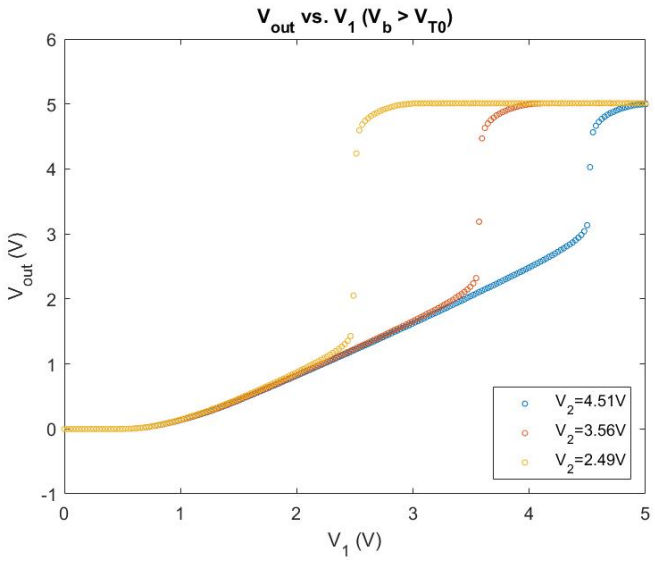

Figure 3: Voltage transfer characteristics for the differential amplifier at three different values of V_2 when the bias transistor is held in strong inversion.

2 Experiment 2: Transconductance, Output Resistance, and Gain

In Experiment 2, we measured the transconductance, output resistance, and gain of our differential amplifier with the bias transistor held in weak inversion.

2.1 Circuit

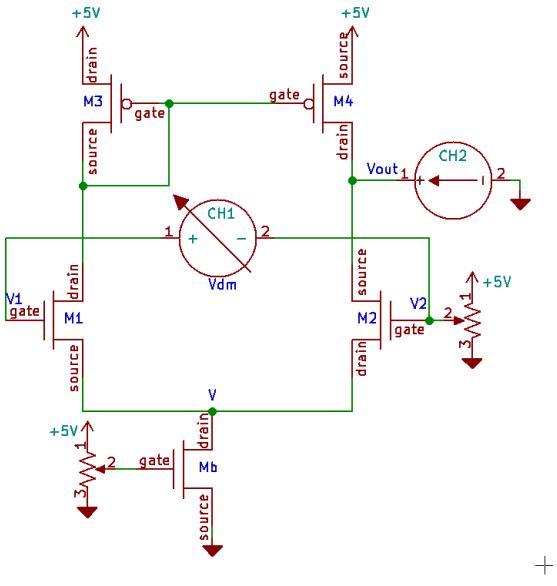

Figure 4: Circuit used to measure voltage transfer characteristics, transconductance, and output resistance of the differential amplifier.

2.2 Observations

For the voltage transfer characteristic shown in Figure 5, we see that around where $V_{dm} = 0$, V_{out} increases rapidly. The fact that this rapid increase is slightly offset below zero most likely indicates that the transistors we chose for this experiment are not perfectly matched. The slope of this rapid increase represents the differential-mode voltage gain of the circuit, which is equal to 240.93 in this case. For the plot below, as with all of the plots in Experiment 2, we held V_2 at $2.49V$ and swept V_1 around V_2.

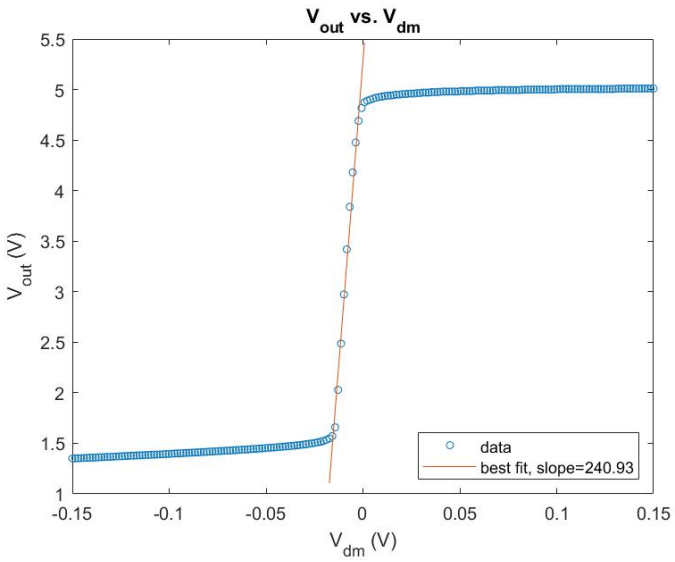

Figure 5: Plot showing V_{out} as a function of V_{dm} in the differential amplifier around the region of high gain where V_{dm} is close to zero with the bias transistor held in weak inversion.

Figure 6 highlights the output resistance of the circuit. The shallow region of this I-V characteristic shows the range of output voltages over which the gain of the circuit is large, and the slope of this region corresponds to the reciprocal of the circuit's output resistance. Because sign convention for measuring incremental output resistance dictates that current should be flowing into the circuit, we do not need to flip the sign of the current. We obtain a slope of $1.386\text{x}10^{-7} 1/\Omega$ for the graph below which is equivalent to an incremental output resistance of $7.213\text{x}10^{6}\Omega$.

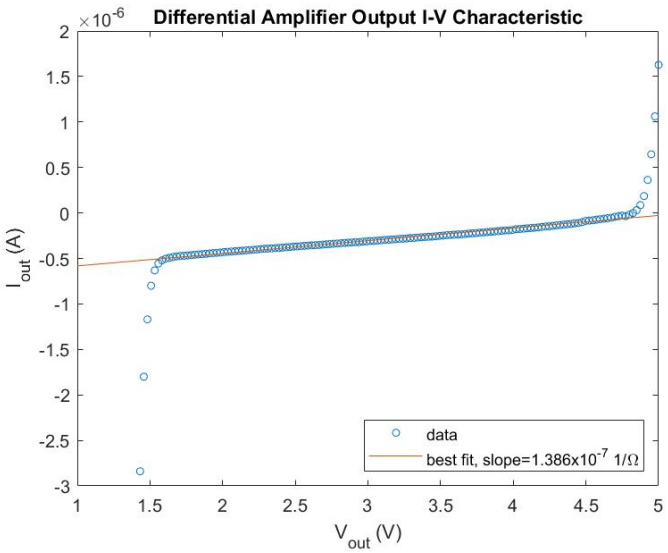

Figure 6: Plot showing I_{out} vs. V_{out} with V_{dm} held at zero. Note that the x-axis begains at $1V$, as we have zoomed in on the shallow region of the curve.

To find the incremental transconductance gain of the circuit, we held the output voltage at $3.25V$, which was approximately in the shallow region of Figure 6 where the gain of the circuit is large. We then swept V_1 around V_2 in order to measure the output current of the circuit. The slope of the region within approximately $100mV$ of $V_{dm} = 0$ gives us the incremental transconductance, equal to $2.925\text{x}10^{-5}1/\Omega$.

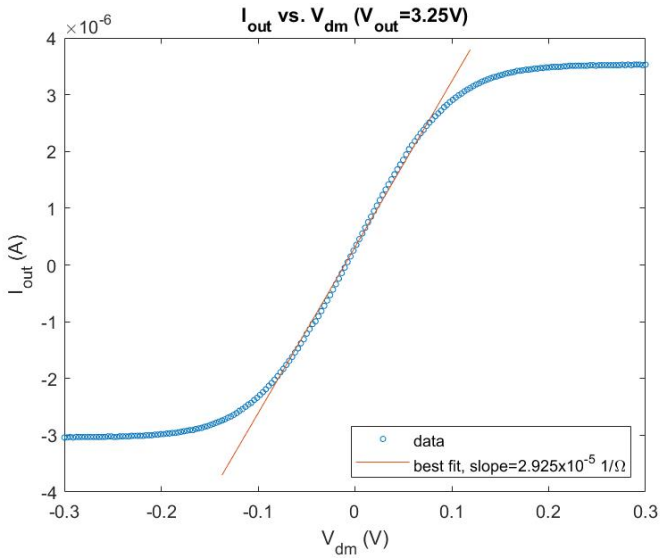

Figure 7: Plot showing I_{out} as a function of V_{dm} with V_{out} held at $3.25V$, which lies in the middle of the high gain region of Figure 6.

Using the values we obtained for the incremental output resistance and incremental transconductance gain with Equation 1, we found the differential-mode voltage gain of the circuit to be 211.01. This value of A_{dm} is slightly lower than the value, 240.93, that we obtained directly from the voltage transfer characteristic. This difference in extracted values for the gain may be attributable

to the value we obtained for V_{out} from Figure 6, as we simply chose a voltage near the middle of the shallow region of the plot. Additionally, our best-fit lines may not fit the data exactly. If we were to consider a few more or less points to be in the region of high gain in any of our plots, the fits would likely still appear visually accurate but might differ slightly in such a way as to make the gains we obtained closer to equaling one another.

$$A_{dm} = \frac{\partial V_{out}}{\partial V_{in}} = \frac{\partial V_{out}}{\partial I_{out}} \frac{\partial I_{out}}{\partial V_{dm}} = R_{out} G_m \tag{1}$$

3 Experiment 3: Unity-Gain Follower

In Experiment 3, we configured the amplifier to work as a unity-gain follower by connecting the output to the inverting input terminal and observed the behavior of the circuit.

3.1 Circuit

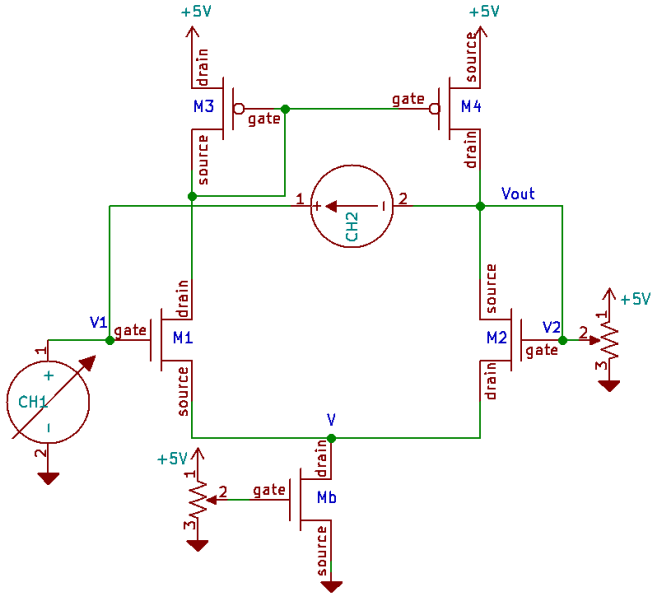

Figure 8: Differential circuit setup as a unity-gain amplifier. The SMU is setup to supply a voltage at V_1 while measuring V_{out} and $V_{out} - V_{in}$.

3.2 Observations

As Figure 9 shows, the incremental gain of our unity-gain follower is extremely close to unity at 0.9915. This slight deviation from unity could be due to marginal differences in the transistors we used or inaccuracies in our wiring or measurement devices.

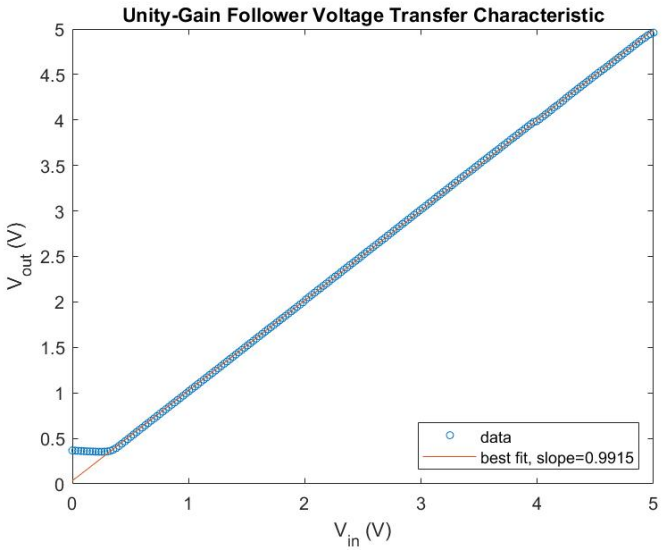

Figure 9: Voltage transfer characteristic for our unity-gain follower.

In Figure 10, we directly observed the offset voltage of the amplifier. The unusual behavior when V_{in} is near $0V$ is likely due to either properties of the source measurement unit or currents too low to accurately measure. Once we move past this region, $V_{out} - V_{in}$ remains near zero but continues to decrease slightly over the remainder of the range through which we sweep V_{in}. In fact, best fit line to the data has a slope of just -0.003 in this region of operation.

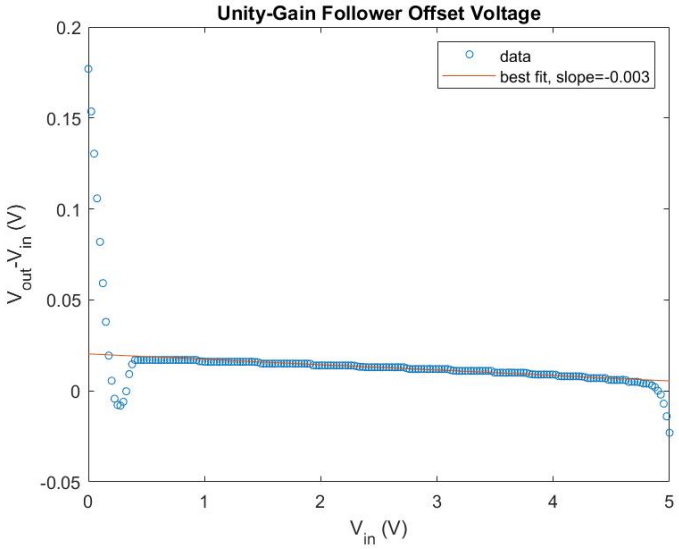

Figure 10: Plot showing the offset voltage of our unity gain follower.