# Circuits Lab 6

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## 1 Experiment 1: Transistor Matching

Experiment 1 focuses on measuring the channel current as a function of the gate voltage for all four transistors on a nMOS ALD1106 chip.

### 1.1 Circuit

The circuit schematic for experiment 1 is shown in Figure 1. In order to measure the characteristics of each transistor on the chip, we applied a voltage through channel 1 to the gate of each transistor and measured the corresponding current through the source terminal with channel 2. The drain of each transistor was set to $V_{dd}$.

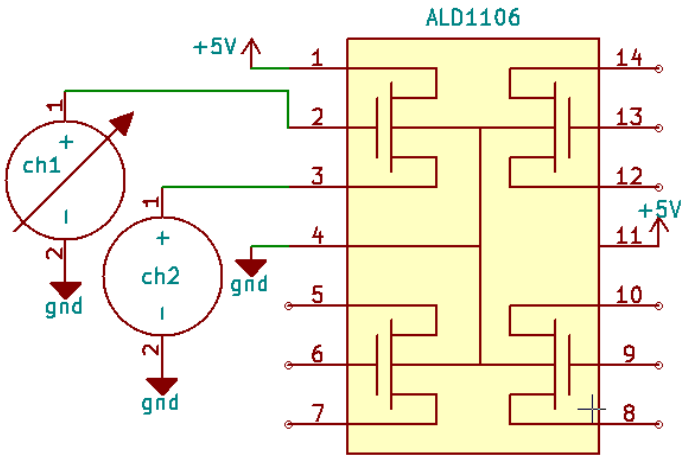


Figure 1: Schematic depicting our setup for measuring the channel current as a function of gate voltage for one of the four nMOS transistors on the ALD1106 chip. We used the same SMU setup to conduct measurements on the other three transistors on the chip.

### 1.2 Observations

After collecting our data, we used the Matlab ekvfit script on the data we collected in order to obtain values for kappa ($\kappa$), specific current ($I_s$), and threshold voltage ($V_{T0}$). These are shown for all four transistors in Table 1.

| Q | $\kappa$ | $I_s$ | $V_{T0}$ |
|---|---|---|---|
| Q1 | .549 | $1.847\text{x}10^{-6}A$ | $.696V$ |
| Q2 | .524 | $1.584\text{x}10^{-7}A$ | $.729V$ |
| Q3 | .544 | $1.686\text{x}10^{-7}A$ | $.722V$ |
| Q4 | .481 | $1.471\text{x}10^{-7}A$ | $.742V$ |

Table 1: The values of $\kappa$, $I_s$, and $V_{T0}$ for each of the nMOS transistors we tested on the ALD1106 transistor array, respectively.

As the plot in Figure 2 displays, the characteristics of all four transistors on the ALD1106 are nearly identical. As we expect, an increase in the gate voltage causes an increase in the transistors' channel currents ($I$). We used Equation 1, with $U_T = 0.0256V$, and the ekvfit data to fit the EKV model to our data over the entire range of voltages as the transistors shifted between weak, moderate, and strong inversion. For all four of the nmos transistors, the EKV model matches our data in all stages of inversion, although for one transistor the EKV model slightly diverges from our data in the weak inversion region. This divergence could be due to the values of epsilon that we input when using the ekvfit script on our data.

$$I_{sat,nmos} = I_s log^2(1 + e^{(\kappa(V_{GB}-V_{T0})-V_{SB})/2U_T}) \tag{1}$$

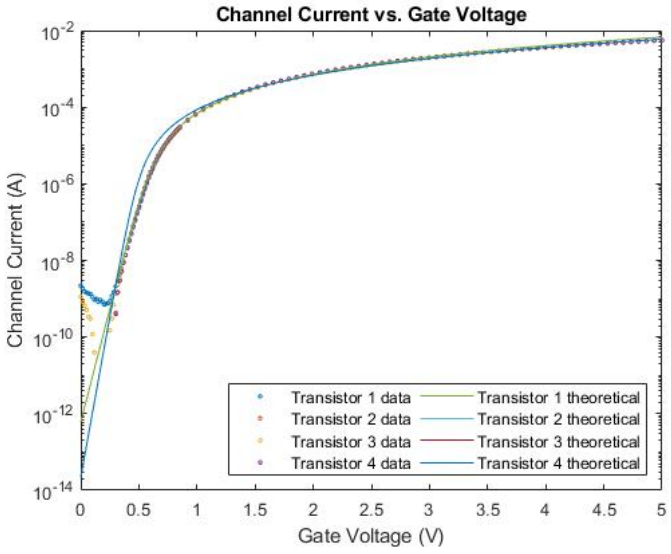


Figure 2: Channel current ($I$) versus gate voltage ($V_g$) plotted for each transistor in the ALD1106 chip alongside their theoretical fits.

To better compare the difference between each transistor in our ALD1106 chip, we plotted the percent difference between the each of the transistors' channel currents and the mean channel current of all four transistors, calculated using Equation 2. The percent difference of each transistor varies between $+/-6\%$ while the transistors are in weak inversion. However, as soon as the transistors enter strong inversion, the percent difference in their channel current's converge around zero (within $+/-2\%$ when $I_{mean} > 10^{-5}A$) implying that their channel currents converge in the region of strong inversion. This convergence could either be due to the transistors behaving more similarly to one another in strong inversion or because the currents are nearly identical when the

gate voltage is set to $5V$ because the resultant channel current would simply be the current limit of the SMU.

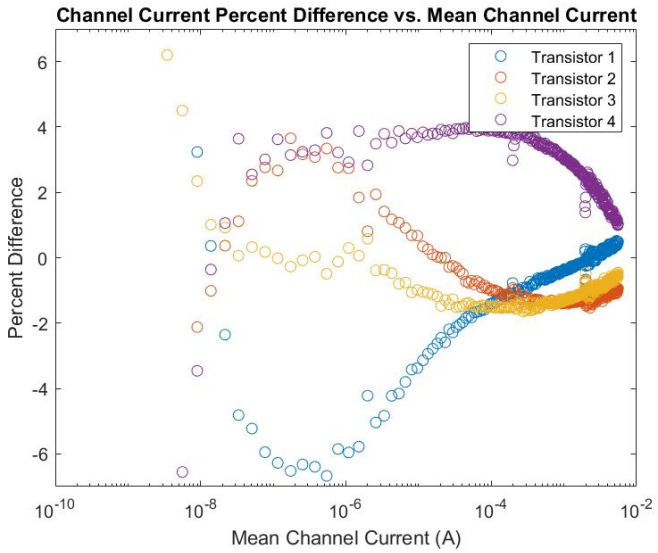


Figure 3: Graph of percent difference between the channel current of an individual transistor and the mean channel current of all four transistors.

$$\text{Percent Difference Qn} = \frac{I_{channel,n} - I_{channel,mean}}{I_{channel,mean}} \text{ x } 100 \tag{2}$$

# 2 Experiment 2: MOS Transistors in Series and Parallel

Our goal in experiment two was to observe how configurations of matched nMOS transistors can be used in parallel or series to divide or multiple the current flowing through a single nMOS transistor.

## 2.1 Circuit

The first section of this experiments requires measuring the channel current through a single nMOS transistor. The schematic used for this measurement is the same as the schematic shown in Figure 1. We also measured the cumulative channel current (I) flowing through a set of transistors setup in parallel and series to each other. In both of these cases, the channel current was a function of the gate voltage($V_g$). The schematics for these circuits are shown in Figure 4.

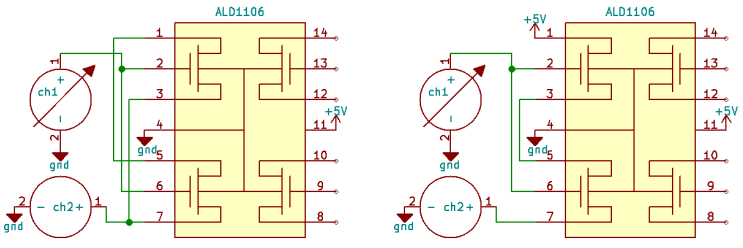


Figure 4: Circuit schematics used to measure two nMOS transistors in parallel (left) and two nMOS transistors in series (right) as a function of $V_g$.

## 2.2 Observations

To observe the cumulative current characteristics across a wide range of nMOS operation modes, we measured $I$ versus $V_g$ with $V_{ds} = 10mV$ and $V_{ds} = V_{dd}$. The results of our I versus $V_g$ measurements for all three circuits (single, parallel, and series) are plotted in Figure 5. As we can see, for both values of $V_{DS}$, the channel current is highest when the matched pair of transistors are oriented in a parallel configuration and lowest when they are in a series configuration. Qualitatively, the graph reflects an offset between the channel currents for all three circuits in the weak, moderate, and strong inversion regions of transistor operation. Because Figure 5 is plotted with the y-axis on a log scale, a constant offset implies both the series and parallel circuits are directly proportional to the single transistor with a constant value of proportionality. When $V_G$ is below approximately $0.3V$, or the approximate lower bound of the voltages that constitute weak inversion, however, the behavior of the transistors is unpredictable and do not reflect the offset we see in weak, moderate, and strong inversion.

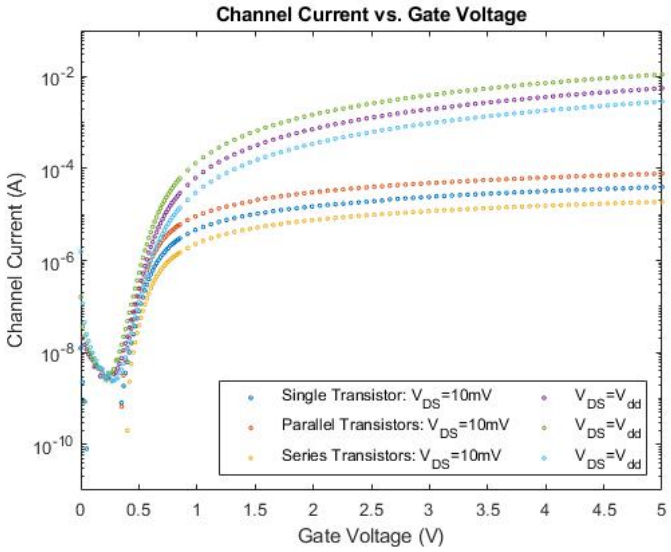


Figure 5: Plot showing the channel current for three different configurations of nMOS transistors at two values of $V_{DS}$.

To better understand the channel current relationship between the parallel circuit and a single transistor, we plotted the ratio of their respective currents as a function of their gate voltage in Figure 6. For both values of $V_{dd}$, the ratio $(\frac{I_{parallel}}{I_{single}})$ quickly approaches 2 as $V_g$ increases: a ratio we expected from the prelab assignment. Similar to our qualitative analysis for Figure 5, we can observe that the proportionality value is practically constant across weak, moderate, and strong inversion.

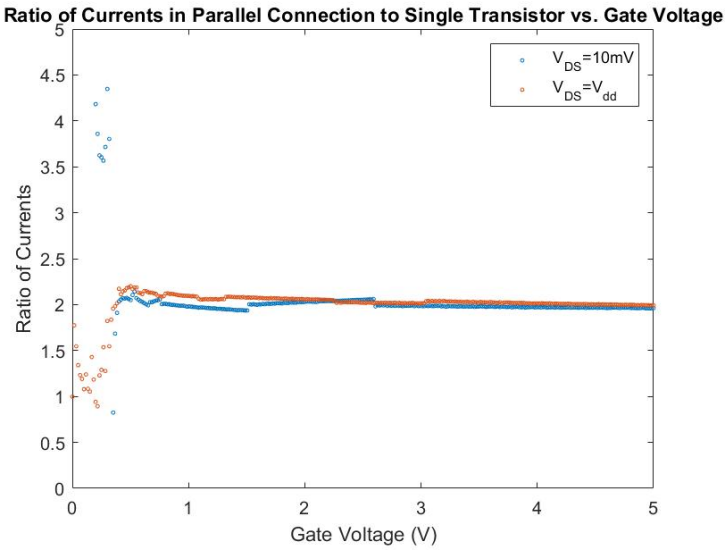


Figure 6: Plot showing the ratio of currents when the nMOS transistors were in the parallel configuration to the single transistor configuration as a function of gate voltage.

Similar to the parallel configuration, we plotted the ratio between $I$ of the single transistor and $I$ of the two transistors in series, or $\frac{I_{single}}{I_{series}}$, as a function of $V_g$ in Figure 7. Again, the ratio of currents quickly approaches 2 for both values of $V_{dd}$. This indicates that adding a nMOS transistor in series with another nMOS transistor results in half the current flowing through the circuit, as we expected from the prelab assignment. As before, the ratio is practically constant in all regions of operation once $V_G$ is high enough for the transistor to be in at least weak inversion.

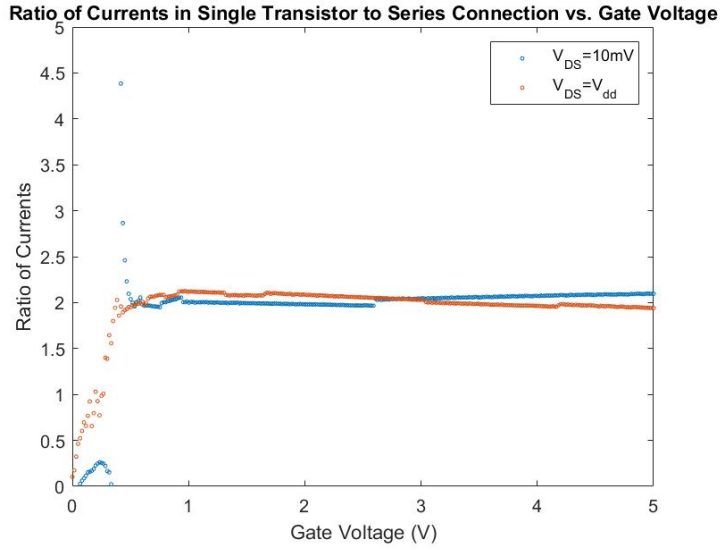


Figure 7: Plot showing the ratio of currents in the single nMOS transistor configuration to the series configuration of transistors as a function of gate voltage.

# 3 Experiment 3: MOS Current Dividers

Our goal in experiment three was to observe and analyze the current transfer characteristics of two different circuits each containing two matched transistors in parallel.

## 3.1 Circuit

The circuit schematic used to create these two current dividers is shown in Figure 8. The main parallel structure of the two circuits is the same, however, in the first circuit we are pulling current from the source of the transistors while the second circuit pushes current through the drain.

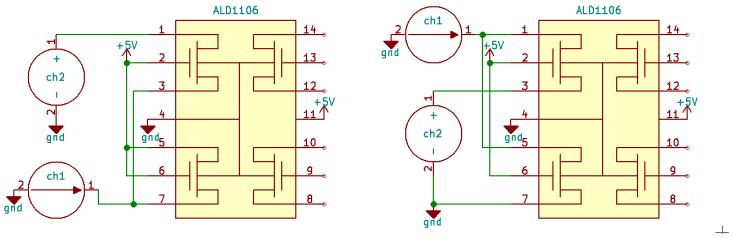


Figure 8: Circuit schematics for measuring the current transfer characteristics of the two two-way current dividers we tested.

## 3.2 Observations

Figure 9 displays the current transfer characteristic for the source driven current divider we tested. Because the SMU was pulling current out of the circuit, we supplied negative currents as our input and measured the current at one of the output nodes. As the plot shows, the magnitude of the output current increases as the magnitude of the input current increases, as expected from the prelab assignment. Since the circuit has two matched transistors in parallel, the current should be evenly divided into both channels. This means the theoretical equation is simply:

$$|I_{out}| = |\frac{I_{in}}{2}| \tag{3}$$

Given that the slope of best-fit ($-.498$), obtained using Matlab's polyfit function, is practically the same as the theoretical slope of $-.500$, the two lines are nearly indiscernible in Figure 9.

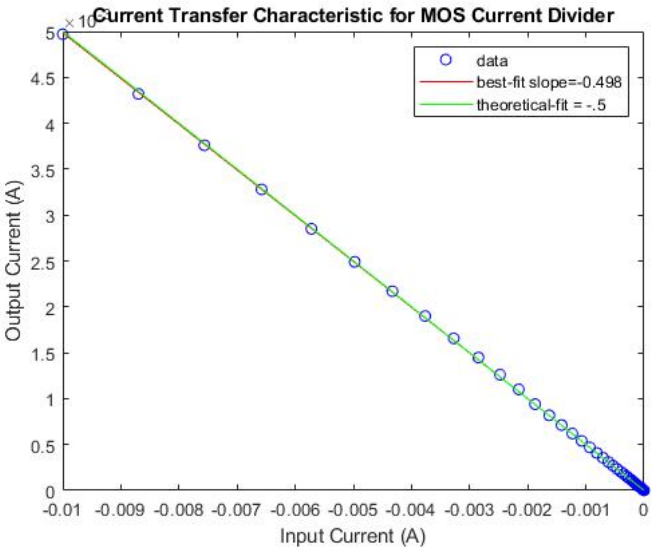


Figure 9: Graph of input versus output current of a source-driven current divider.

Figure 10 shows the current transfer characteristic for the drain driven current divider. This time, we needed the SMU to push current into the divider, so we supplied positive input currents. Again, as the magnitude of the input current increases, the magnitude of the output current increases as well. Similar to the first circuit, the two matched transistors in parallel should split the current equally between the two transistors. The equation for the output current is also the same, as shown in Equation 3.

The slope of best fit for the drain driven current divider is further away from the theoretical fit than the source driven divider with a ratio of .493. This is more discernible at a higher input current where the larger current value produces a larger error.

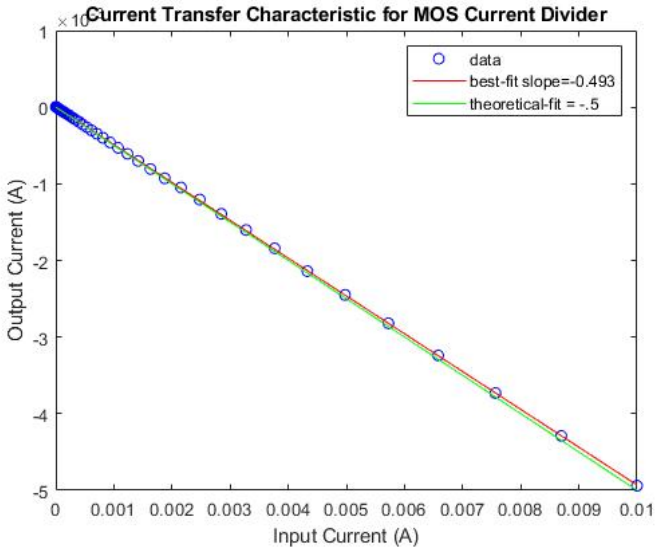


Figure 10: Graph of input versus output current of a drain-driven current divider.