Circuits Lab 7

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April 15, 2019

1 Experiment 1: Differential Pair Current-Voltage Characteristics

The purpose of this experiment is to collect data from a MOS differential pair and analyze the voltage-current characteristics of different nodes within the differential pair.

1.1 Circuit

While the general circuit for this experiment was a nMOS differential pair, we had three iterations of the circuit to measure different nodes in the circuit. Figure 1 is setup to allow us to change the differential-mode input voltage (V_{dm}) with channel 1 of the SMU and measure the current flowing through the channel current of the first transistor (I_1).

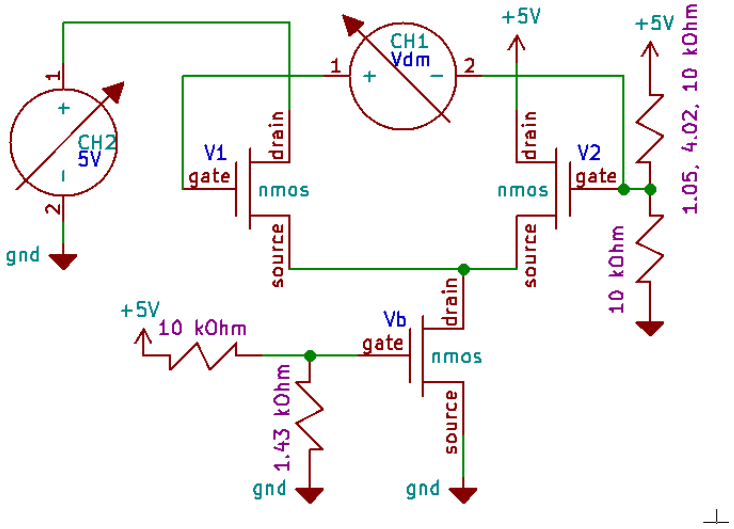

Figure 1: Circuit used to measure I_1 while varying V_{dm}.

The next circuit, shown in Figure 2, was also setup to change V_{dm} with channel 1 but now channel 2 of the SMU measures the current flowing through the second transistor (I_2).

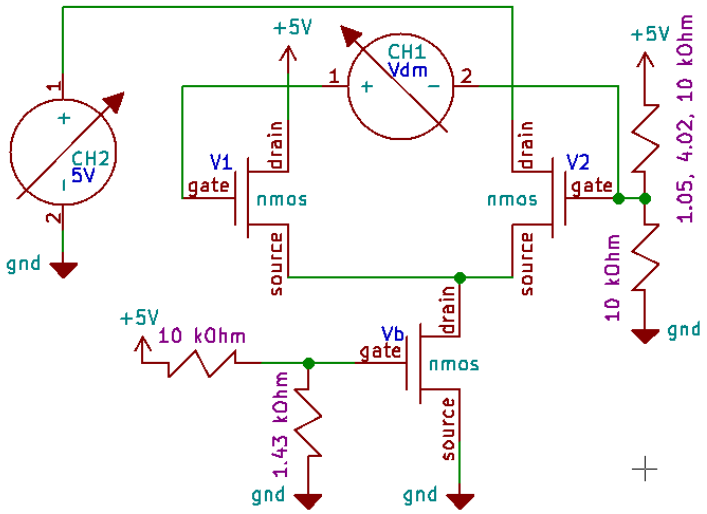

Figure 2: Circuit used to measure I_2 while varying V_{dm}.

Our third setup used channel 1, again, to change the voltage across V_{dm}, however, channel 2 was used to measure the voltage at the source of the top two transistors; this voltage is known as the common-source node voltage (V). For all three setups, we changed the base common-mode voltages (V_1 and V_2) with a simple voltage divider that output $2.5V, 3.5V$, and $4.5V$. The bias voltag e was also set by a voltage divider that output $.628V$ and $1.11V$.

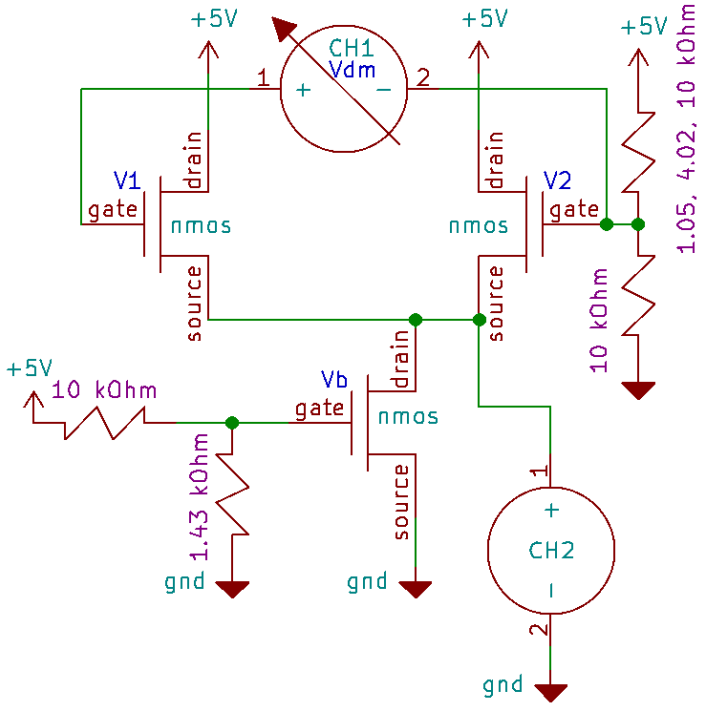

Figure 3: Circuit used to measure V while varying V_{dm}.

1.2 Observations

Initially, we set V_b to be approximately at threshold ($0.628V$) and varied V_2 to investigate how the I-V characteristics and voltage transfer characteristics change with V_2. In Figure 4, we see that for all three values of V_2 spanning from $2.5V$ to $4.5V$, the I-V characteristics are nearly identical. For all three values of V_2, I_1 and I_2 behave exactly as we expected from the prelab assignment. When $V_1 = V_2 = V_{cm}$, $I_1 = I_2 = \frac{I_b}{2}$. This demonstrates that when the differential-mode input voltage is equal to zero, the output currents are equal to one another. In contrast, when V_1 exceeds V_2 by a few tenths of a volt, in this case approximately two tenths of a volt, I_2 is practically zero, while I_1 is approximately I_b. In the graph, this manifests itself on the right, when V_{dm}, which equals $V_1 - V_2$, is positive. The reverse is true when V_2 exceeds V_1 by a few tenths of a volt: as I_1 drops to nearly zero and I_2 rises to I_b. Additionally, we see that $I_1 + I_2$ remains a constant value throughout the range of values for V_{dm} for all values of V_2, while $I_1 - I_2$ takes the form of an odd symmetric function. From further study in class, we observed that this odd symmetric function is actually a hyperbolic tangent of the form $I_1 - I_2 = I_b \tanh \frac{\kappa V_{dm}}{2U_T}$.

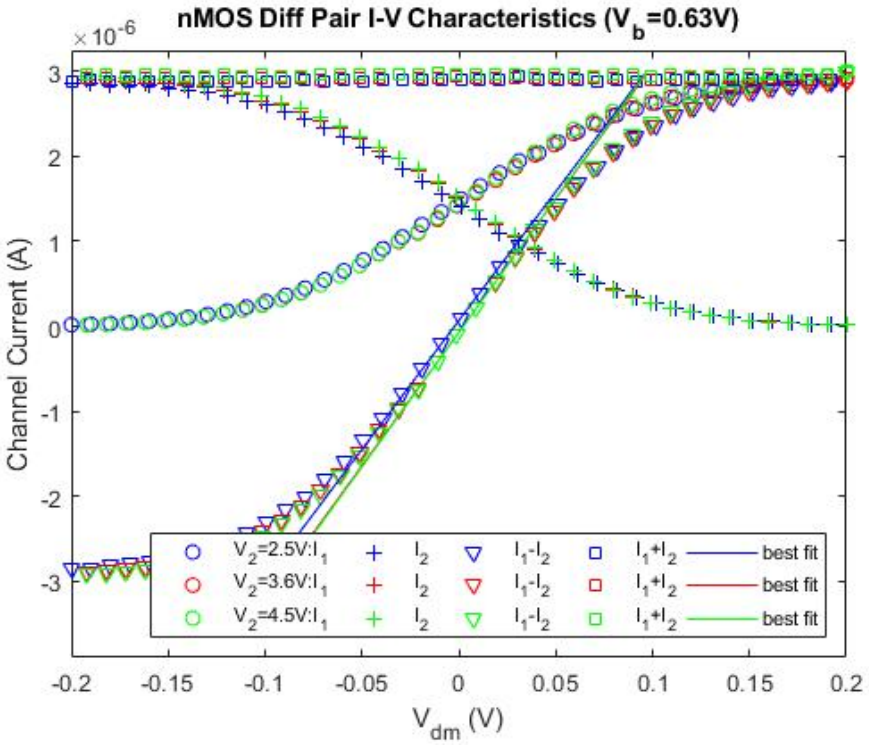

Figure 4: Plot showing the channel current of each transistor in the differential pair, the common-mode output current, and the differential-mode output current as a function of the differential-mode input voltage for each value of V_2.

Figure 5 shows the common-node source voltage (V) of the differential pair as a function of the differential-mode input voltage for all three values of V_2. Each time we increment V_2 by approximately $1V$, V increases by slightly less than one $1V$. When $V_2 > V_1$ by a few tenths of a volts, the plot demonstrates that $V \approx \kappa(V_2 - V_b)$. Since both V and V_2 are held constant in this case, it makes sense that the voltage transfer characteristic is a horizontal line. As the absolute value of V_{dm} decreases, however, this model becomes less and less accurate, since M_1, which was effectively off in the region around $V_{dm} \approx -0.2$, begins to turn on. As we move into the region

where $V_1 > V_2$ by a few tenths of a volt, the common-source node voltage takes the form of a line with a positive slope. Again, this follows from our predictions in the prelab assignment, as $V \approx \kappa(V_1 - V_b)$ in this region. In other words, since V_2 is constant and V_{dm} is increasing, V_1, and thus V, is also increasing. We note, as well, that the plots in Figure 5, however, take the form of a soft-max function, as there is a transition region in which the common source node voltage moves smoothly from relying mostly on V_2 to mostly on V_1, as we expected from our analysis in class.

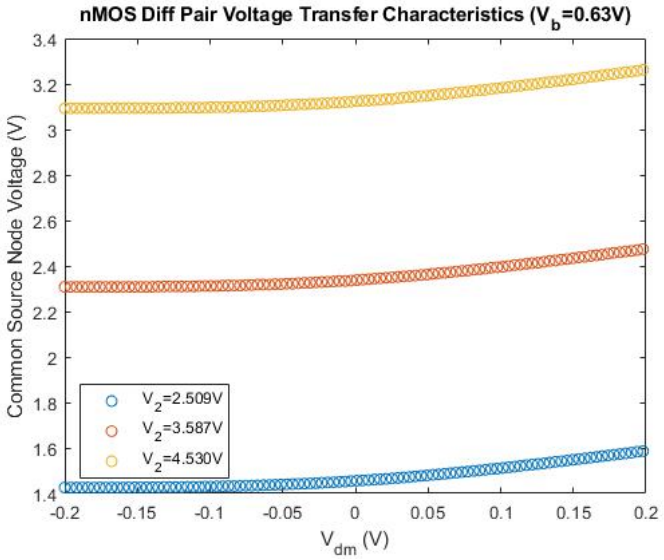

Figure 5: Plot showing the common-source node voltage, V, as a function of $V_1 - V_2$ for three values of V_2.

In Figure 4, we used Matlab's polyfit function to fit a straight line to the plot of $I_1 - I_2$ in the region around $V_{dm} = 0$, or where $V_1 = V_2$, to find the approximate differential-mode transconductance gain of the differential pair. This gain is given, more precisely, by Equation 1.

$$G_{dm} = \frac{\partial I_{dm}}{\partial V_{dm}}\bigg|_{V_1=V_2} = \frac{\partial(I_1 - I_2)}{\partial(V_1 - V_2)}\bigg|_{V_1=V_2} \tag{1}$$

From our lines of best fit, we obtained the values of G_{dm} shown in Table 1. As we can see, the change in the transconductance gain as V_2 changes is nearly negligible, and the slight increase in G_{dm} that occurs as V_2 increases is likely due to the Early Effect.

V_2	G_{dm}
2.509V	3.0349x10^{-5}℧
3.587V	3.1443x10^{-5}℧
4.530V	3.1646x10^{-5}℧

Table 1: The three values that we extracted for the differential-mode transconductance gain of the differential pair.

In order to see how the circuit behaves for other values of the bias voltage(V_b), we set our bias voltage to be above threshold, or at $V_b = 1.11V$ in this case. In Figure 6, we see that the circuit behaves quite similarly to when V_b is around threshold. However, the output currents are now two orders of magnitude greater than they were when the V_b was around threshold. Additionally, the

width of the differential-mode region around $V_1 = V_2 = V_{cm}$ has increased. This change in width is due to the relationship between the gate voltage(V_g) and channel current(I) when the transistors are in weak and strong inversion. In weak inversion, the channel current of a MOS transistor increases exponentially with gate voltage, while in strong inversion, the channel current increases only with the square root of the gate voltage. In strong inversion, $|V_{dm}|$ must be higher, around $0.4V$, in order for the $I_1 - I_2$ to approach I_b as compared to weak inversion where $|V_{dm}|$ only needs to be around $0.2V$.

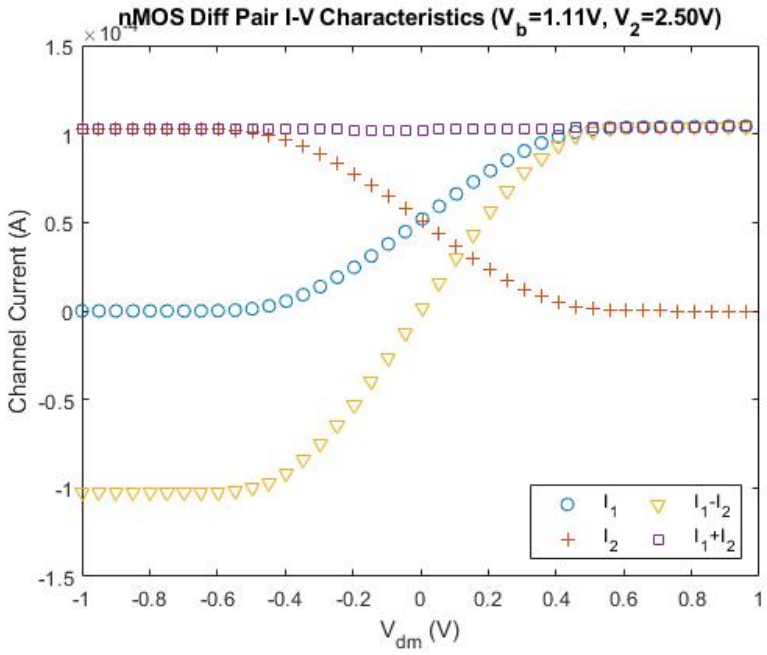

Figure 6: Plot showing the channel current of each transistor in the differential pair, the common-mode output current, and the differential-mode output current as a function of the differential-mode input voltage for one value of V_2 when the bias transistor is in strong inversion.

Finally, Figure 7 shows the voltage transfer characteristic of the differential pair in strong inversion with $V_2 = 2.5V$. Again, when $V_{dm} < 0V$ by a few tenths of a volt, the common-source node voltage depends almost exclusively on V_2. Since V_2 is being held constant at 2.5V, it makes sense that the node voltage is constant as well. When $V_{dm} > 0$ by a few tenths of a volt, the node voltage depends nearly exclusively on V_1, which is increasing linearly with V_{dm}. As a result, the common-source node voltage should increase linearly, as it does in the figure below. As mentioned when discussing the differential pair's I-V characteristic, the width of the differential mode region has increased, which manifests itself as the strong inversion source node voltage remaining constant when $V_{dm} < -0.4V$ and increasing linearly when $V_{dm} > 0.4V$. In contrast, the differential mode region of the moderate inversion voltage transfer characteristic that we observed in Figure 5 only stretches from around $V_{dm} = -0.2V$ to $V_{dm} = 0.2V$.

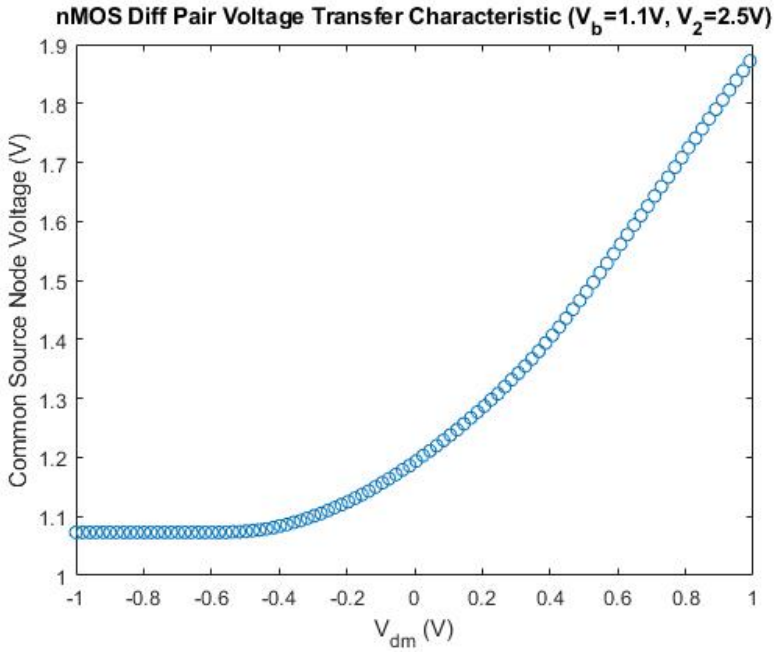

Figure 7: Plot showing the common-source node voltage, V, as a function of $V_1 - V_2$ for three values of V_2.