Circuits Lab 5

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1 Experiment 1: Gate Characteristics

Our goal for experiment 1 was to characterize the behavior of an ALD1106 nMOS transistor array and an ALD1107 pMOS transistor array by measuring the channel current of one transistor on each array as we swept the gate voltage over a range of values.

1.1 Circuit

On both chips, we connected pins 4 and 11 of the transistor array to ground and V_{dd}, respectively, to establish the bulk voltage. In order to characterize the nMOS transistor specifically, we connected the drain to V_{dd}, or 5V in this case, the source to channel 2 of the SMU, which we set to 0V and used to measure the channel current, and the gate to channel 1. We then swept the gate voltage from 0V to 5V.

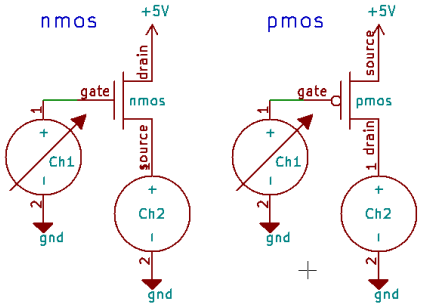

Figure 1: Circuits setup used to measure the source current with sweeping values for the gate voltage.

1.2 Observations

After collecting our data, we used the Matlab ekvfit script on the data we collected in order to obtain the values for κ, I_s, and V_{T0} shown in Table 1. In order to utilize the ekvfit script for the pmos transistor, we reflected the data by setting $V_{G,pmos,ekvfit} = 5 - V_{G,pmos,collect}$. To obtain an accurate zero-bias threshold voltage for the pmos transistor, then, we simply subtracted $5 - V_{T0,pmos,ekvfit}$. Additionally, note that we utilized $25.6mV$ for the thermal voltages U_T of both transistors.

Q	κ	I_s	V_{T0}
nmos	0.6560	1.8388x$10^{-6}A$	0.6457V
pmos	0.7168	8.1279x$10^{-7}A$	4.2237V

Table 1: The values of κ, I_s, and V_{T0} for each of the nmos and pmos transistors we tested on the ALD1106 and ALD1107 transistor arrays, respectively.

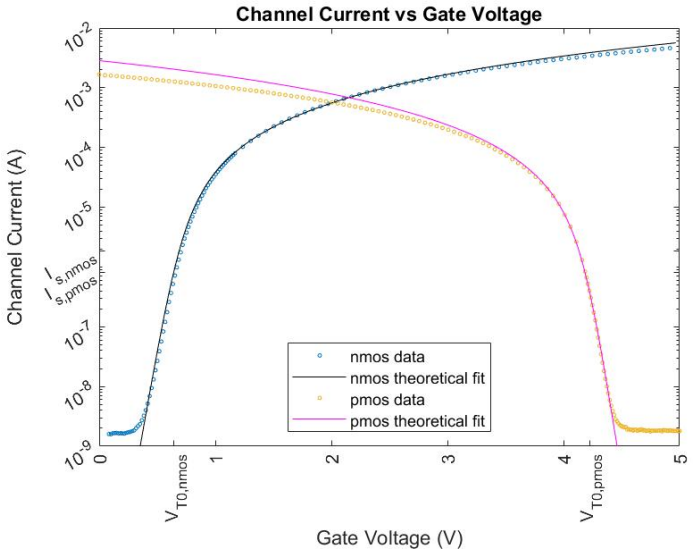

Figure 2: Semilog-y plot showing the channel current as a function of gate voltage for both the nmos and pmos transistors.

As the plot in Figure 2 displays, the nmos and pmos characteristics are quite similar, except that as the gate voltage increases, the nmos transistor's channel current increases while the pmos transistor's channel current decreases. We used Equations 1 and 2 to fit the EKV model to our data over the entire range of voltages as the transistors shifted between weak and strong inversion. For the nmos transistor, the EKV model matches our data remarkably well in all stages of inversion. In contrast, for the pmos transistor, while the EKV model matches our data perfectly in weak inversion, it diverges slightly from the data in strong inversion.

$$I_{sat,nmos} = I_s log^2(1 + e^{(\kappa(V_{GB} - V_{T0}) - V_{SB})/2U_T}) \tag{1}$$

$$I_{sat,pmos} = I_s log^2(1 + e^{(\kappa(V_{BG} - V_{T0}) - V_{BS})/2U_T}) \tag{2}$$

Additionally, Figure 3 shows the incremental transconductance gains of the transistors as a function of channel current. We utilized Matlabs diff command and dot-divide operator in order to compute a finite difference approximation to the partial derivative of the channel current with respect to the gate voltage and extract the data points, as such in Equation 3.

$$g_m = \frac{\text{diff}(I_c)}{\text{diff}(V_G)} \tag{3}$$

$$g_{m,weak} = \kappa \frac{I_{sat}}{U_T} \tag{4}$$

$$g_{m,strong} = \kappa \frac{\sqrt{I_{sat} I_s}}{U_T} \tag{5}$$

We then fit the EKV model to the regions of weak and strong inversion for both the nmos and pmos transistor using Equations 4 and 5. As exhibited in Figure 3, the EKV model fits the data for both the nmos and pmos transistors quite well in weak inversion and in strong inversion for the nmos transistor. However, the strong inversion fit for the pmos transistor only matches the data over a small range of values.

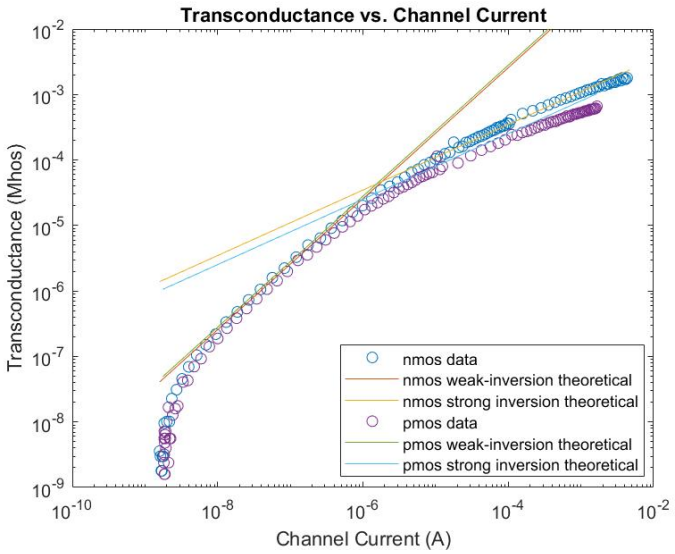

Figure 3: Log-log plot showing the incremental transconductance gain as a function of channel current for both the nmos and pmos transistors.

2 Experiment 2: Source Characteristics

Our goal for experiment 2 was to characterize the source behavior of the nmos and pmos transistors.

2.1 Circuit

To measure the effect of the source voltage(V_s) on the channel current(I), we tied both the gate voltage(V_g) and drain voltage(V_d) to a constant value and applied a varying voltage to V_s while measuring the current through V_d. In the case of the nmos transistor, V_g and V_d were set to $5V$. For our pmos setup, V_g and V_d were set to $0V$ or what we considered ground.

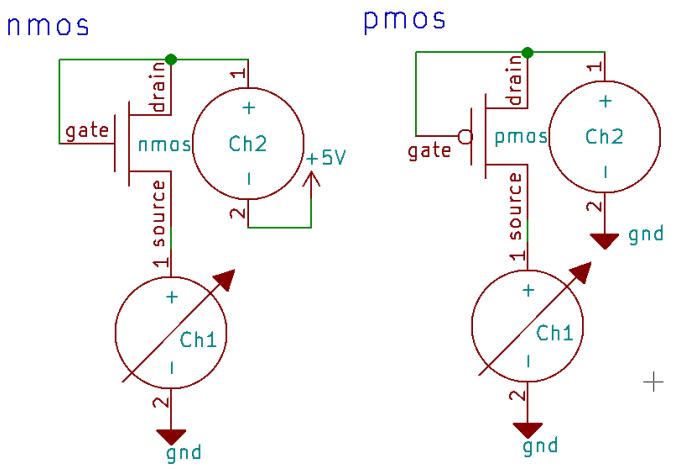

Figure 4: Circuits setup used to measure the drain current while sweeping values for the source voltage.

2.2 Observations

The graph below shows the I versus V_s characteristics of a nmos transistor. The line of best fit is located along the segment of weak inversion. The slope of this line is equal to $-29.21A/V$. Compared to the nmos data in figure 2, this graph generally follows the same pattern with two distinct saturation and ohmic regions. However, the transition from saturation to ohmic is more shallow in figure 5 with a threshold voltage roughly equal to $1.5V_{ds}$ compared to a threshold voltage of $.645V_g$ for the I-V_g characteristics of the same nmos transistor.

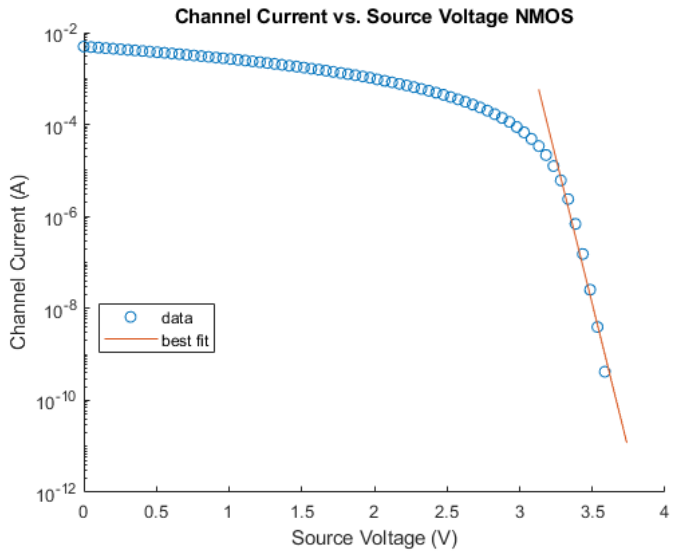

Figure 5: Semilog-y plot showing I with respect to V_s of a nmos transistor. The best fit line is placed in the ohmic region of the transistor where it is exhibiting weak inversion.

The next graph shows the same I-V_s characteristics but for a pmos transistor. The data within the weak inversion region is fitted with a line of best fit with a slope of $26.74A/V$. The I-V_s for

the pmos transistor is very similar to the I-V_g relationship of the pmos transistor shown in figure 2. The V_t for this graph (around $3.8V_{ds}$) is smaller than the threshold voltage in figure 2 ($4.2V$).

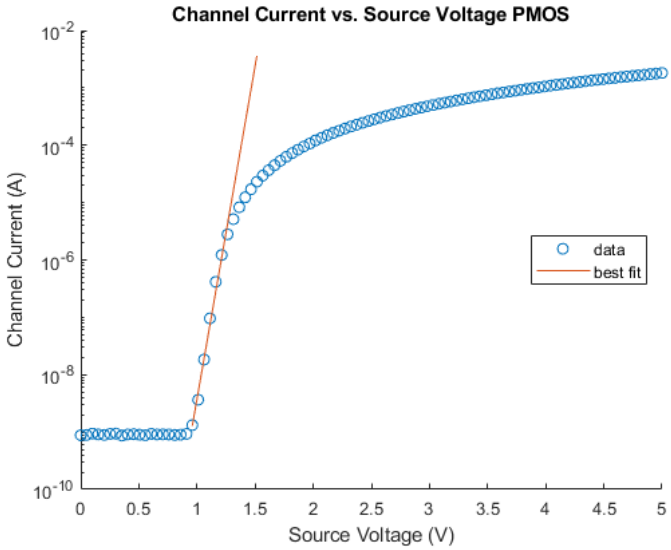

Figure 6: Semilog-y plot showing I with respect to V_s of a pmos transistor. The best fit line is attached to the weak inversion segment of the graph.

The incremental source conductance (g_s) of a transistor describes the relationship between a small change in I and a small change in V_s: represented as $g_s = \frac{\delta I}{\delta V_s}$. To find g_s for our nmos and pmos transistors, we simply have to apply the following equation to our I-V_s data: $g_s = \frac{diff(I)}{diff(V_s)}$.

The values for g_s can also be simulated in both the weak and strong inversion regions of the pmos and nmos transistors. The same set of equations to model the weak and strong regions apply to both pmos and nmos transistors.

$$\begin{aligned} &\text{Weak Inversion:} \\ &\qquad g_s = \frac{I_{sat}}{U_T} \\ &\text{Strong Inversion} \\ &\qquad g_s = \frac{sqrtI_{sat} * I_s}{U_T} \end{aligned} \tag{6}$$

In this case we are approximating I_{sat} as the measured current(I). U_T has also been approximated throughout this experiment as $U_T = .0256V$. The value for specific current was found using the ekvfit function and was determined to be $8.13e-7A$ for the pmos transistor. Figure 7 shows the log-log plot of the absolute value of the g_s compared to I. Because I decreases when V_s increases, the incremental source conductance is negative. However, we plotted the absolute value of g_s to fit the data inside of a log-log plot. Both the weak and strong inversion models of g_s fit the general pattern of the data. However, the weak inversion model is noticeably offset from the data. This is most likely be due to our approximation that $I_{sat} = I$ but could also be caused by our approximation of U_T and the use of the diff() commands in matlab to calculate g_s.

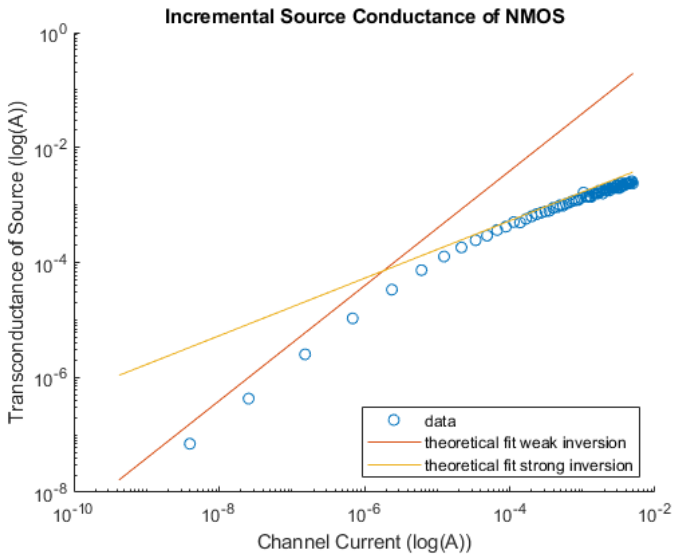

Figure 7: Incremental source conductance of a nmos transistor. Theoretical fits are applied to bot the weak and strong inversion regions.

Figure 8 is a plot of g_s compared to I for a pmos transistor. Because the current increases with a rise in V_s for a pmos transistor, g_s is normally positive. However, as in figure 7, we plotted the absolute value of g_s to make a few outlying negative g_s data points positive. As in the previous graph, the weak and strong inversion fits match the shape of the g_s data but are slightly offset. This is again mainly due to the approximation that $I = I_{sat}$ but could be related to the approximations mentioned earlier.

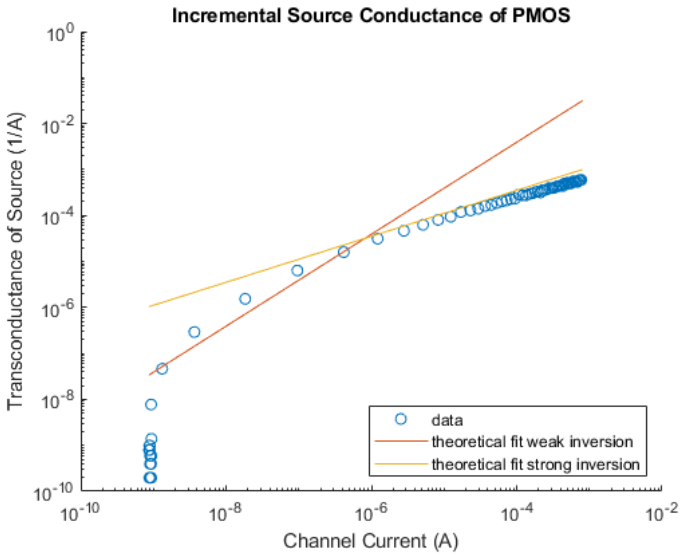

Figure 8: Incremental source conductance of a pmos transistor. Theoretical fits are applied to bot the weak and strong inversion regions.

3 Experiment 3: Drain Characteristics

Our goal for experiment 3 was to characterize the drain behavior of the nmos and pmos transistors.

3.1 Circuit

In order to characterize the drain of the nMOS transistor, we connected the source terminal of the transistor to ground, channel 2 to the gate terminal, and channel 1 to the drain. We then set the gate to a constant voltage during each measurement and swept the drain voltage from 0V to 5V, using channel 1 both to set this drain voltage and measure the channel current in the transistor. For the pMOS transistor, we connected the terminals in much the same way, with exception that the source of the pMOS transistor was set to V_{dd}.

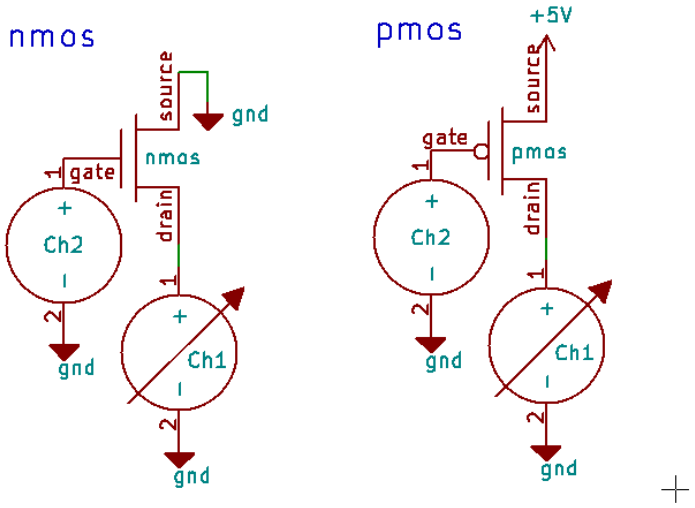

Figure 9: Circuits setup used to measure the drain current while sweeping both the drain voltage and gate voltage.

3.2 Observations

Our first graph, shown in Figure 10, shows channel current as a function of drain voltage for the nMOS transistor on the ALD1106 transistor array at three unique gate voltages. These gate voltages were 100mV below the threshold voltage, at the zero-bias threshold voltage obtained in experiment 1, and at V_{dd}. Respectively, these three voltages represent the nMOS transistor in weak, moderate, and strong inversion. As the plot displays, an increase of 100 mV in the gate voltage corresponds to an increase of an approximately a decade in the channel current when the transistor is in saturation. This observation logically follows from our finding on the prelab that we should increase the gate voltage to increase the channel current.

Moreover, because the nMOS transistor's channel current remains well above 0A except when the drain voltage is extremely close to 0V, we can see that nMOS transistors are able to pass a strong logical 0, a concept we will explore in the postlab.

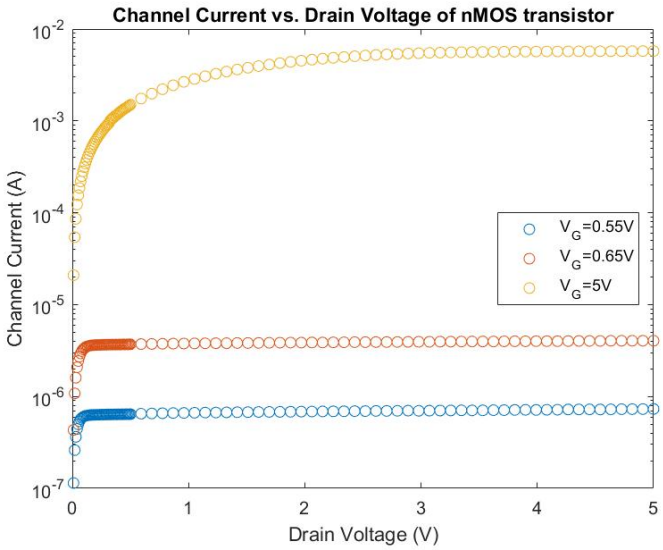

Figure 10: Semilog-y plot showing the channel current as a function of drain voltage for a nMOS transistor when the gate voltage is set at three unique voltage below, at, and above threshold.

Similarly, Figure 11 shows channel current as a function of drain voltage for the pMOS transistor at three gate voltages. These gate voltages were 100mV above threshold voltage, at the zero-bias threshold voltage obtained in experiment 1, and at ground. Respectively, these three voltages represent the nMOS transistor in weak, moderate, and strong inversion. As the plot shows, a decrease of 100 mV in the gate voltage corresponds to a increase of approximately a decade in the channel current when the transistor is in saturation. This observation logically follows from our finding on the prelab that we should decrease the gate voltage to increase the channel current.

Moreover, because the pMOS transistor's channel current remains well above 0A except when the drain voltage is extremely close to V_{dd}, we can see that pMOS transistors are able to pass a strong logical 1, a concept we will explore further in the postlab.

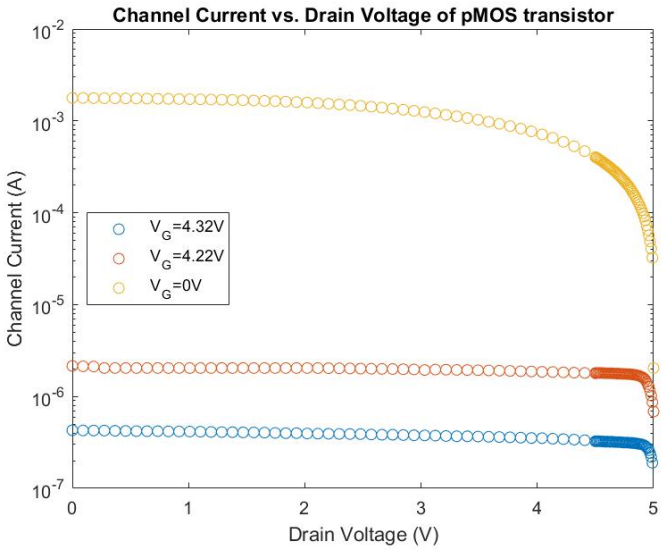

Figure 11: Semilog-y plot showing the channel current as a function of drain voltage for a pMOS transistor when the gate voltage is set at three unique voltage below, at, and above threshold

From the plots in Figures 10 and 11, we were able to extract values for the early voltage, saturation current, and the transistor's intrinsic gain. To find the early voltage and saturation current for the nMOS transistors, we used Matlab's polyfit function to find straight-line fits to each of our data-sets in the saturation region of the drain characteristics on linear scales. The y-intercepts of these line were the saturation currents and the x intercepts were the negative of the early voltages, as given by equation 7, which describes the best-fit lines. The slopes of these lines were also equivalent to $\frac{1}{r_o}$. Similarly, to find the intrinsic gains, we used r_o as well as Matlab's polyfit function to fit straight lines to our data-sets in the ohmic region of the drain characteristics on linear scales. The slopes of these lines are equal to g_s when the drain voltages are equal to zero. We then calculated the intrinsic gain as $g_s r_o$.

$$I = I_{sat}(1 + \frac{V_{DS}}{V_A}) \tag{7}$$

Figure 12 shows early voltage as a function of saturation current for both the nMOS and pMOS transistors below, at, and above threshold gate voltage. For the pMOS transistor, it appears that the early voltage roughly increases as the saturation current increases. For the nMOS transistor, the early voltage spikes when the transistor's gate voltage is at threshold, but otherwise increases from below threshold to above threshold.

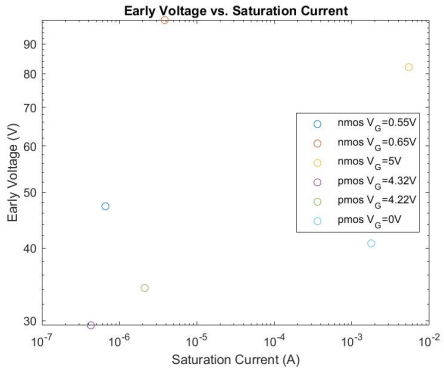

Figure 12: Semilog-x plot showing the early voltage as a function of saturation current for the nMOS and pMOS transistors below, at, and above threshold gate voltage.

Finally, Figure 13 displays the intrinsic gain of the transistor as a function of the saturation current for both the nMOS and pMOS transistors. For both transistors, the intrinsic gain peaks when the transistor is in moderate inversion and is least when the transistor is in strong inversion. Since the intrinsic gains of both transistors in all modes of operation remain well above 10 (between $[10^1,10^3]$), it seems fair to assume that it is generally a good assumption that a transistor's intrinsic gain is much larger than unity. As a result, we know that $g_m r_o$ is also much larger than unity if κ is greater than or equal to 1. If κ is less than 1, $g_m r_o$ may approach or even become less than unity.

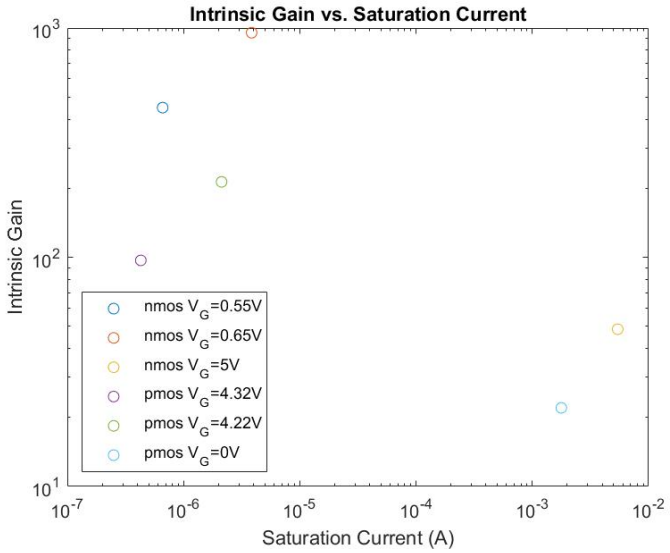

Figure 13: Semilog-x plot showing the intrinsic as a function of saturation current for the nMOS and pMOS transistors below, at, and above threshold gate voltage.