Circuits Lab 9: The Last Hurrah

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1 Experiment 1: Voltage Transfer Characteristics

1.1 Circuit

In this experiment, we measured the voltage transfer characteristics of our current-mirror differential amplifier when holding the inverting input at three unique constant voltages and sweeping the non-inverting input from one rail to the other.

1.2 Observations

Figure 1 shows a voltage transfer characteristic for our current-mirror differential amplifier. Whereas in Lab 8 we observed that the when $V_1 < V_2$, V_{out} increased linearly with V_1, we can now observe that V_{out} remains constant at the negative rail of the circuit when $V_1 < V_2$. Once $V_1 \approx V_2$, V_{out} sharply jumps towards the positive power supply rail, where it remains once $V_1 > V_2$.

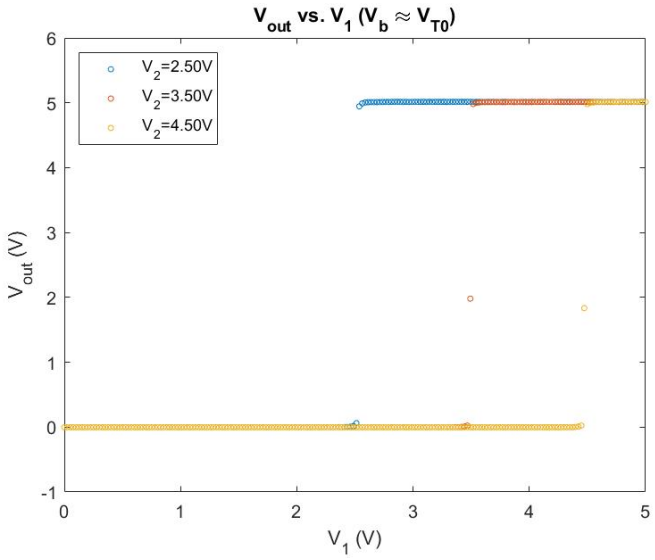

Figure 1: Voltage transfer characteristics for the current-mirror differential amplifier at three different values of V_2 when the bias transistor is held in moderate inversion.

2 Experiment 2: Transconductance, Output Resistance, and Gain

2.1 Circuit

In Experiment 2, we set up our circuit in order to enable us to measure the transconductance, output resistance, and differential-mode voltage gain of the current-mirror differential amplifier.

2.2 Observations

Figure 2 contains a voltage transfer characteristic for the circuit obtained by sweeping the non-inverting input voltage, V_1, around the inverting input and measuring V_{out}. We fit a straight line to the steep region of the curve using Matlab's polyfit function to obtain a differential-mode voltage gain of 377.21.

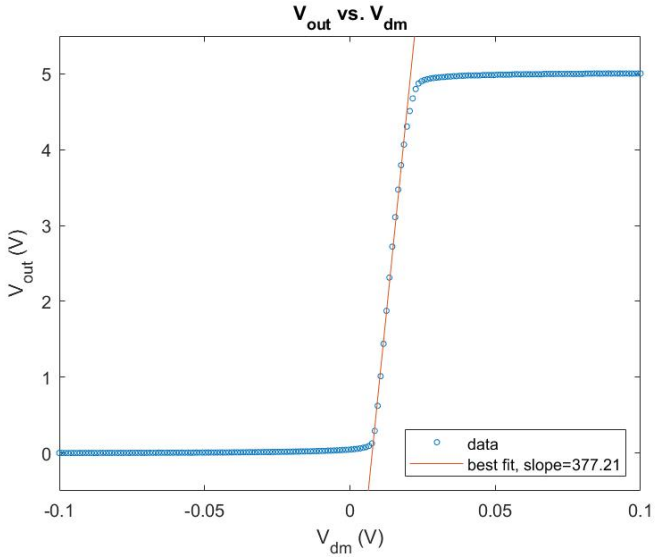

Figure 2: Plot showing V_{out} as a function of V_{dm} in the current-mirror differential amplifier around the region of high gain where V_{dm} is close to zero with the bias transistor held in moderate inversion.

Figure 3 shows an I-V characteristic for the circuit with V_{dm} held at zero. Using Matlab's polyfit function, we fit a straight line to the shallow part of this curve. From the reciprocal of this line of best fit, we found the incremental output resistance of the circuit to be $5.253\text{x}10^7\Omega$.

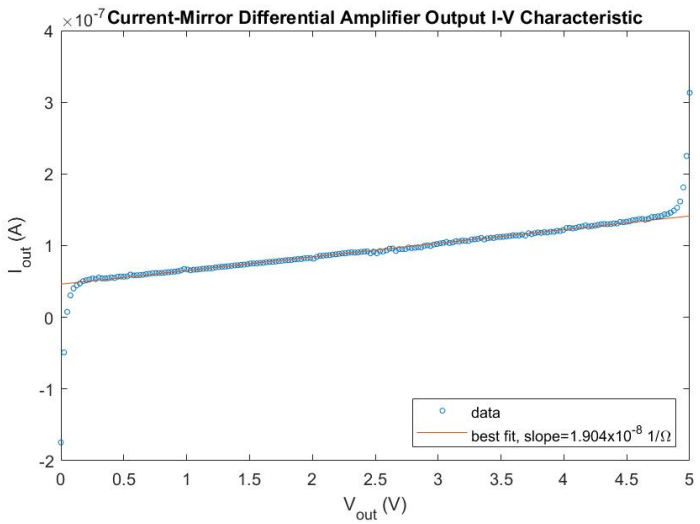

Figure 3: Plot showing I_{out} vs. V_{out} with V_{dm} held at zero.

In Figure 4, we plotted a output current of the circuit as a function of V_{dm} with the output voltage held fixed at $2.50V$, which was approximately the center of the shallow region of Figure 3. We then used Matlab's polyfit function to fit a straight line to the region of the curve around where $V_{dm} = 0$ in order to find the incremental transconductance gain of the circuit, which was $5.413\text{x}10^{-6}\frac{1}{\Omega}$ in this case. By sweeping V_{dm} over a sufficiently large range, we saturated I_{out} and found that its limit when $V_{dm} < 0$ was $-5.04\text{x}10^{-7}A$ and its limit when $V_{dm} > 0$ was $3.98\text{x}10^{-7}A$.

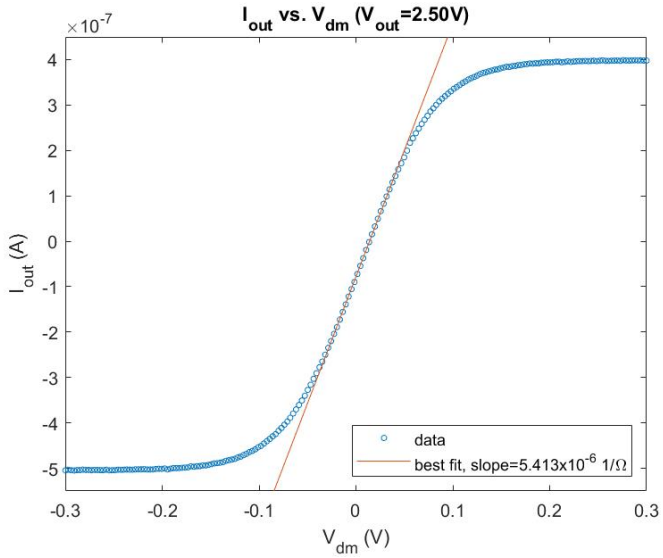

Figure 4: Plot showing I_{out} as a function of V_{dm} with V_{out} held at $2.50V$, which lies in the middle of the high gain region of Figure 3.

Using the incremental output resistance we found in Figure 3 and the incremental transconductance gain we found in Figure 4, we calculated the differential-mode voltage gain of the circuit with Equation 1 to be 292.871. This value was significantly smaller than 377.21 value that we obtained from fitting a straight line directly to the high-gain region of the voltage transfer characteristic in Figure 2. Both of these values, however, remain quite a bit greater than differential-mode gain we

obtained in Lab 8, which was 240.93 according to the voltage transfer characteristic and even less when we calculated it using the output resistance and transconductance gain.

$$A_{dm} = \frac{\partial V_{out}}{\partial V_{in}} = \frac{\partial V_{out}}{\partial I_{out}} \frac{\partial I_{out}}{\partial V_{dm}} = R_{out} G_m \tag{1}$$

3 Experiment 3: Unity-Gain Follower Step Response

The goal of experiment 3 was to observe the behavior of our unity gain amplifier when a small capacitave load ($10nF$) is tied to the output. We were able to record the output of the unity-gain amplifier with both a small and large amplitude square wave. The small amplitude square wave had a frequency of 100Hz, an amplitude of $30mV$, and a dc-offset of $2V$. The large amplitude square wave had a frequency of 50Hz, an amplitude of $2V$ and a dc-offset of $3V$.

3.1 Circuit

Our circuit contains an additional LMC6482 op-amp setup as a unity follower with the input being the output of our unity-gain amplifier. This additional circuit was necessary to isolate the output of our circuit from the load of the scope. The scope we used, an Analog Discovery, has a input resistance of roughly 1 Mega-Ohm and draws roughly $1\mu A$ of current. This additional current affected the voltage transfer characteristic of the circuit and led to unintended results.

3.2 Observations

The following figure (Figure 5) shows the voltage response V_{out} to our unity-gain follower circuit with a small-amplitude square wave as our input voltage V_{in}. In a similar manner to an RC circuit, the V_{out} of the circuit exponentially approaches V_{in} in time when V_{in} changes state. The asymptotic approach of V_{out} towards V_{in} is nearly symmetrical in shape for an up-going and down-going step; however, we extracted different time constants for these two types of steps, which means they are not perfectly symmetrical. The transition of V_{out} to V_{in}(+offset) is an exponential approach in time to V_{in}: a typical characteristic of a linear circuit.

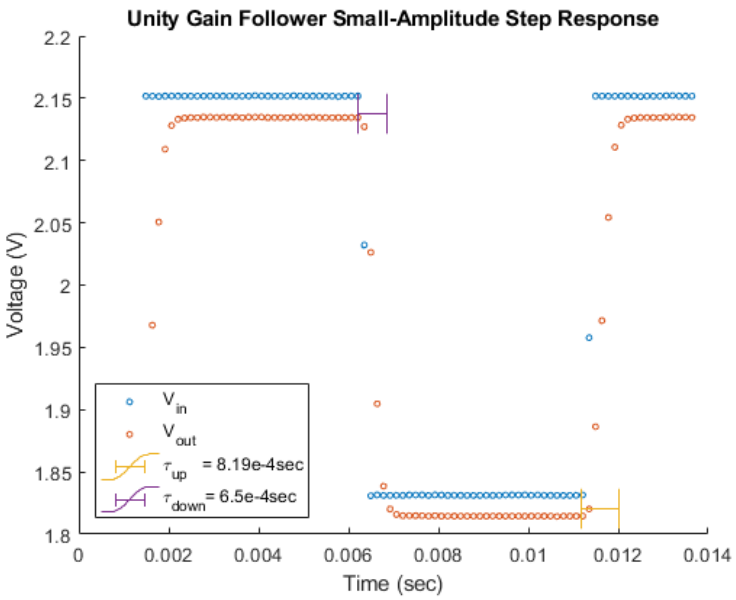

Figure 5: Plot showing V_{out} and V_{in} with labeled time constants for both the up-going and down-going transitions.

The time constant (τ) for an RC circuit can be calculated in a variety of ways. Due to the ability to pick exact data points to mark the start and end of transition periods, we chose to calculate τ as the time it takes for the circuit to transition roughly 63% of the way from the old to new voltage value. This method was extracted from the following equation.

$$\begin{aligned} V_{out} &= V_{in} * (1 - e^{\frac{-t}{\tau}}) \\ \text{When: } t &= \tau \\ V_{out} &= V_{in} * (1 - e^{-1}) \\ V_{out} &= .63 * V_{in} \end{aligned} \tag{2}$$

For an RC circuit, τ is also equal to the resistance multiplied by the capacitance of the circuit: $\tau = R * C$. While we choose an arbitrary value of capacitance for our circuit ($C = 1nF$), we have to extract the resistance value from the transconductance of the circuit(found in experiment 2). With the transconductance, we can calculate τ as $\tau = \frac{C}{G_m}$. The three values of τ calculated for Figure 5 are shown in Table 1. While all three time constants are in the same order of magnitude, they vary significantly from each other. Given that the transconductance and capacitance of our circuit maintains the same value across this range of V_{out}, the time constant for the up-going and down-going portion should be same. The errors in the values of τ are most likely attributed to the scarcity of data points in the transition region of V_{out} or the transistors we used not matching perfectly.

τ_{up}	τ_{down}	$\tau_{experiment2}$
$8.19\text{x}10^{-4}sec$	$6.5\text{x}10^{-}4sec$	$1.79\text{x}10^{-4}sec$

Table 1: Calculated values of τ for V_{out} with a small amplitude wave.

The voltage response of our unity-gain follower circuit to a large-amplitude square wave is shown

below. Compared to the small-amplitude response, V_{out} for Figure 6 is much more linear over a larger region of V_{in}. The slope of the linear regions of V_{out} is referred to as the slew rate of the system. It is important to note that the slew rate is different for the up-going and down-going transitions of V_{out}: making the output circuit asymmetrical.

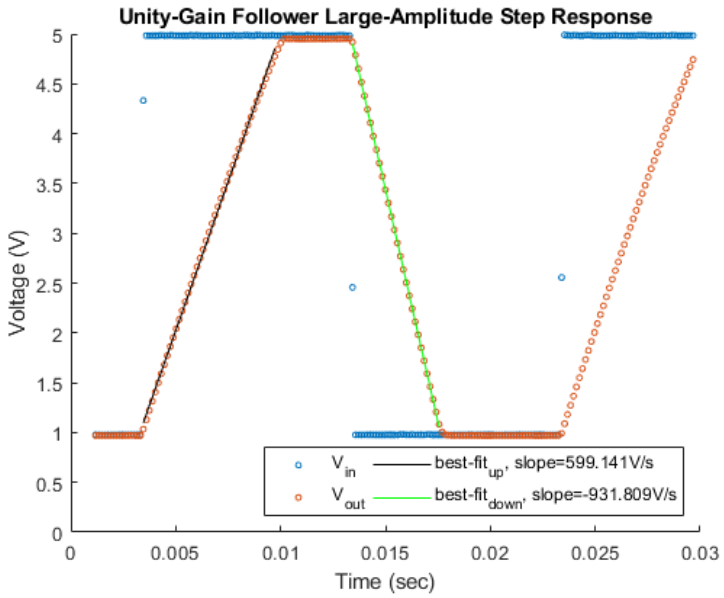

Figure 6: Plot showing V_{out} and V_{in} with labeled slew rates for both the up-going and down-going transitions.

The maximum slew rate of our circuit is limited by the load capacitance and maximum current that can flow out of V_{out}. The maximum slew rate is defined by the following equation:

$$\frac{\partial V}{\partial t} = \frac{I_{max}}{C} \tag{3}$$

Assuming that $I_{max} = I_b$, we found that the maximum slew rate was roughly $1000V/sec$. The difference between the theoretical maximum slew rate and the slew rates shown in Figure 6 could be due to multiple reasons. Given the relatively low capacitance load, there could be additional capacitance that reduced the slew rates observed, the current flowing through V_{out} could also be lower than I_b.