Circuits Final Project Report: Level Shifting

Daniel Connolly
William Fairman

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1 Introduction

For the final project, we chose to explore various types of bi-directional logic-level shifting circuits. These circuits are used to bridge communication traces between components that operate at different voltages. Devices communicating over I2C frequently use bi-directional level shifters to prevent the logic of a device running at higher voltage from destroying other devices with supply lower voltages. For electronic hobbyists, the predominant use case is the transmission of 5V logic from a micro-controller to 3V logic for peripheral devices (sensors, screens, etc.).

In order to better understand how different types of level shifters operate, we decided to analyze five circuits and compare their propagation delays, power consumption, and the relative area they would take up on a silica die. To standardized the testing parameters, we ran a $0-3V$ and $0-5V$ square wave oscillating at 100kHz, the standard operating frequency of I2C[1], through each of our circuits with a 100pF capacitor on the output to mimic a load. All the circuits we used should have theoretically been able to up-shift, convert a $0V-3V$ wave into a $0V-5V$ wave, and down-shift, convert a $0V-3V$ wave into $0V-5V$.

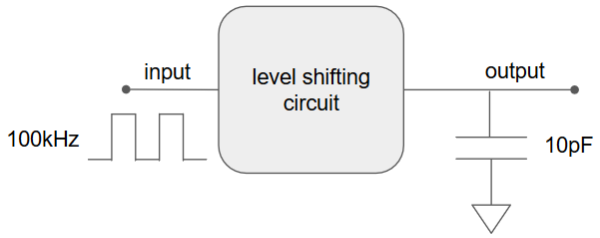

Figure 1: Basic parameters used to test all of our circuits

1.1 Setup

Due to the relatively high frequency of our input signal, we had to rely on equipment that could read and write faster than our standard Analog Discovery. To generate a square wave, we used a Tektronix AFG 3022B Function Generator. We measured the input and output signals of our circuits using a Rigol DS2202 Oscilloscope. To measure the power draw of our circuit, we used two Keithley 2400 SMUs to measure current while supplying $5V$ and $3.3V$ to the high and low side power rails respectively. The equipment used in our setup is shown below.

Figure 2: Equipment and student used to collect data from our various level-shifting circuits.

2 Bipolar-Junction Transistor Level Shifters

The first family of bi-directional circuits we analyzed were made from npn bipolar junction transistors(BJTs). The two schematics we used can be seen in Figures 3 and 5. The first schematic shown in Figure 3 relies on a pair of npn transistors setup to always have an opposite collector to emitter voltage. When the driving signal is coming from the high voltage $(0-5V)$ side, a logic 1 will cause one of the transistors to enter reverse active mode and the other to enter forward active mode. This leads to a net sum of the current to flow from the high side to the low side, increasing the voltage at the low side terminal. The transistors switch modes of operation when the high side signal drops to 0V, draining current from the low side terminal.

The circuit acts slightly different when the low voltage side is driving the signal. When the low side is pulled to $0V$, one of the transistors will be in forward active with the other in reverse active mode. However, unlike the previous situation, both transistors have current flowing from the high-side to low-side: draining the high-side voltage to roughly $0V$. When the low-side voltage is pulled back to $3V$, neither transistor changes state and the net sum of current is still flowing from the high-side to low-side. However, the reduced voltage across both npn transistors allows the pull-up resistor to keep the high-side at $5V$.

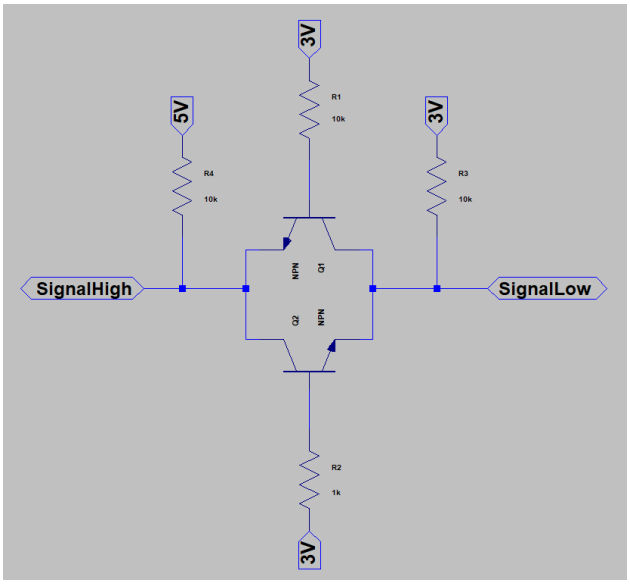

Figure 3: BJT circuit that utilizes the forward active region of each 2N3904 npn transistor to transmit logic level both ways[2].

The circuit in Figure 5 acts in a similar way to Figure 3. When the high-side is driving the signal, the transistor actively switches between reverse and forward active mode when the input signal is $0V$ and $5V$ respectively. However, when the low-side is driving the signal, the current always flows from the high-side to low-side but the changing voltage difference across the npn transistor allows the high-side to be pulled high when the low-side is pulled high.

Both of these BJT style level-shifters are relatively large circuits because the rely on the use of 3 or 4 pull-up resistors. On a silicon chip, the average resistor takes up several orders of magnitude more space than a single transistor: making these circuits dramatically larger than analogous CMOS circuits.

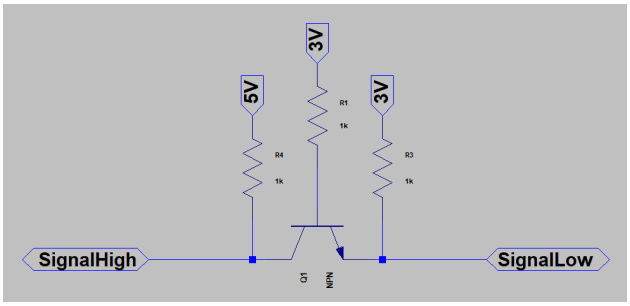

Figure 4: BJT circuit that relies on both the forward active and reverse active region of a single 2N3904 npn transistor[2].

2.1 Propagation Delay

Propagation delay is the measure of how quickly a circuit can transition between two logic states. Mathematically, we calculated the time it took for our output wave to transition half-way between two logic states[3].

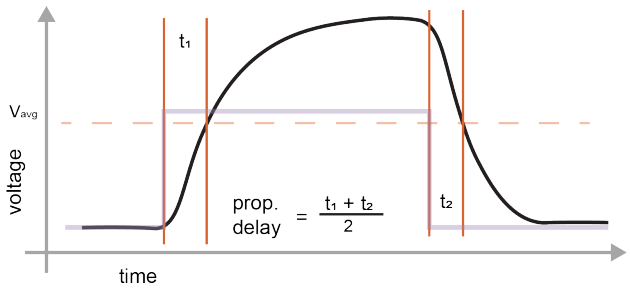

Figure 5: Graph displaying our method for calculating the propagation delay of the output signal.

The following graphs show the output waves of our BJT level-shifting circuits. Each graph has both the up-shifting and down-shifting output waves of the circuit.

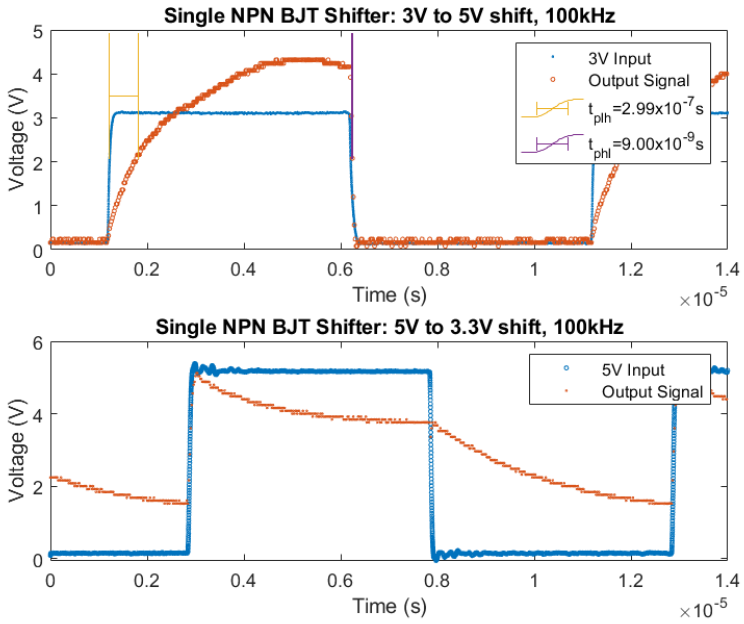

Figure 6: Waveforms from the single NPN level shifter shown in Figure 5 in response to a 100kHz signal. Note that t_{plh} indicates the propagation delay when the input signal changes from low voltage to high voltage and t_{phl} indicates the propagation delay when the input signal moves from high to low.

In Figure 6, we see the results of a test with a single NPN transistor and three resistors being used as a level shifter, per the schematic shown in Figure 5. During an up-shift, or when the positive input voltage rail is at 3V and the positive output rail is at 5V, the transition from low to high voltage follows a fairly exponential approach towards a logical 1 in the output. The transition from high to low, however, is nearly instantaneous, as the bipolar junction transistor enters forward active mode and quickly drains the high-side voltage. In contrast, the down-shift does not manage to reach a level low enough to be considered a logic 0 in I2C. As a result, we did not consider the propagation delay of this particular setup.

The single npn level shifter fails in multiple ways to create a down-shifted $0V - 3V$ logic signal. The large initial spike of the output voltage when the input wave generates a logic 1 would send

a $5V$ voltage level to a device that could only accept a maximum of $3V$. While the output wave does not maintain a $5V$ output for long, this surge could still potentially jeopardize a device. The output signal also fails to reach $0V$ when the input wave transitions to a logic 0: maintaining a low voltage of around $2V$. For some devices, this may not register as a logic 0: disrupting the ability of the I2C bus to send valid bits.

The cause of the distorted output wave is most likely due to the modes of operation of the single npn transistor. When the input transitions to $5V$, the BJT enters forward active mode and allows a large amount of current to move from the high-side input to the low-side output. The BJT only leaves the forward active region when the low-side voltage is roughly equal to $5V$. At this point, the transistor enters cut-off mode and prevents current from flowing through the transistor. The $5V$ voltage level on the low-side output is then slowly drained through the pull-up resistor which is connected to the $3.3V$ power supply rail.

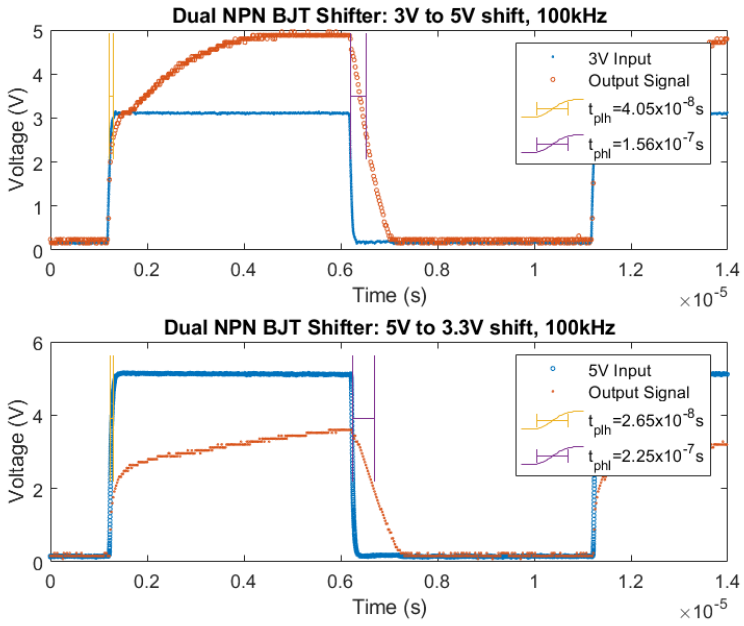

Figure 7: Waveforms from the dual NPN level shifter in Figure 3 in response to a 100kHz signal.

Figure 7 shows the shifted output of our square wave with a dual npn level shifter whose schematic was shown in Figure 3. This particular setup performs fairly well in terms of both up-shifting and downshifting. It is interesting to note that the up-shifting circuit is able to reach a steady state value while the down-shifting circuit is continuously increasing in value while the logic level is still high.

While the single NPN transistor has an average propagation delay of roughly 154 nanoseconds when up-shifting the signal, the average up-shifting propagation delay of the dual NPN shifter is only 98 nanoseconds. The dual npn level shifter also has a valid down-shifting wave that generates an average propagation delay of roughly 126 nanoseconds.

3 CMOS Bi-Directional Level Shifters

The second family of circuits we analyzed were cmos based bi-directional level shifters. One clear benefit of a CMOS level shifter as compared to a BJT shifter is in area cost. In particular, designs that function properly with only CMOS transistors, such as Figure 9, take up significantly less space than level shifters that utilize pull-up and pull-down resistors. The two schematics we used are shown in Figures 8 and 9. The first schematic shown below in Figure 8 takes advantage of the relatively simple states of a nmos transistor. When the high-side is driving the signal high, the transistor is in saturation and supplying a current to the low side. When the signal goes low, the transistor remains in saturation, but the high-side begins to draw a current from the low-side.

When the low-side voltage input is driving the signal, a low input voltage creates a large voltage difference across V_{gs} and V_{ds}, which causes the transistor to act as a closed switch and allows the high-side line to be pulled low. When the low-side input voltage is high, at $3V$, the gate to source voltage, V_{gs}, is close to $0V$ and cuts off the current flowing from the high to low side, allowing the high-side voltage to be pulled to $5V$.

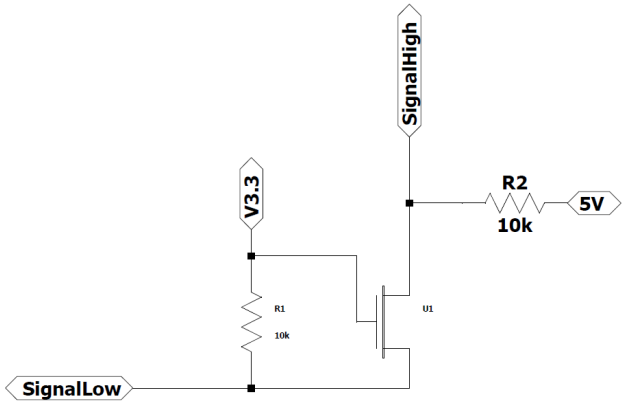

Figure 8: NMOS bi-directional level shifter[4]. We used a transistor on an ALD1106 nMOS transistor array.

Figure 9 shows a cross-coupled CMOS bidirectional level shifter[5]. Essentially, this circuit is two independent unidirectional level shifters cross coupled to enable bidirectional functionality. As a result, when driving one input high, nearly half the circuit is simply statically consuming power while the other adjusts the output voltage level. Taking the left side of the LTSpice schematic, we feed the lower of the two positive power rails, VDDL, into the source of two pMOS transistors in parallel, U1 and U2. The gate of each pMOS is then connected to the drain of the other in order to create an effect similar to that of a bistable element, where a change in the voltage at the drain of one pMOS toggles the gate voltage of the other pMOS. In other words, if the drain voltage of one pMOS decreases, it will "turn up" the drain voltage of the other by way of the gate. Thinking about the input signals, we see that if we set "SignalHigh" - the input signal when the high-side is driving - high, U10 turns on, while U7 is turned off by way of an inverter with a positive rail of VDDH. These two changes turn the gate voltage of the top left pMOS, U1, down and the gate voltage of the top-right pMOS, U2, up, allowing the low power rail voltage VDDL to propagate through to the output node where we measure the "SignalLow." Since this output is connected to the base of U9, which should draw no current, on the right hand level shifter, the output will remain at the power supply rail. When "SignalHigh" is then set low, U10 turns off, while U7 turns on. This effectively cuts off U1 such that the output is held low. We then cross-couple this entire

sub-circuit with a mirrored version of itself in order to achieve the bidirectional effect.

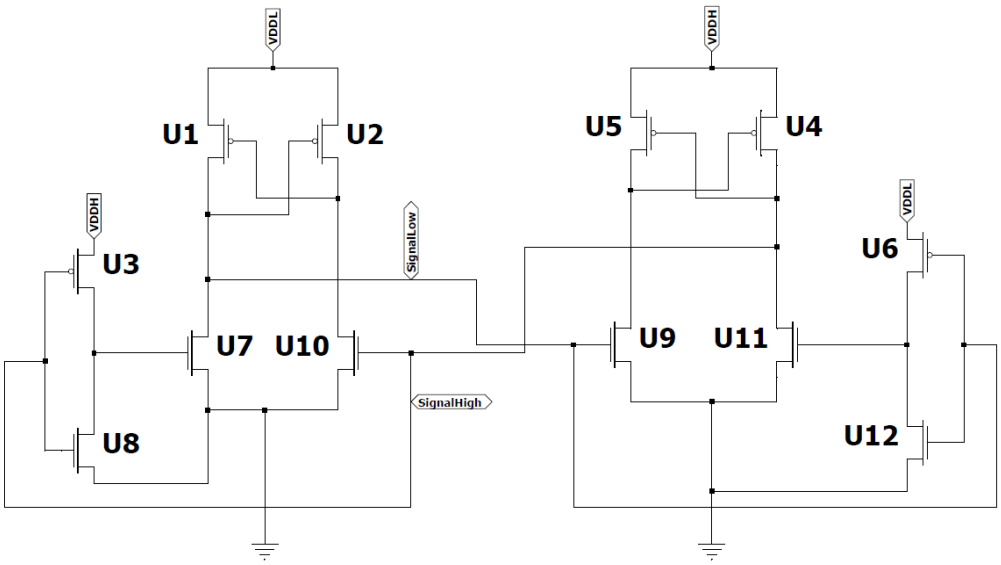

Figure 9: Cross-coupled CMOS bi-directional level shifter that utilizes 6 nmos and pmos transistors from ALD1106 and ALD1107 transistor arrays.

3.1 Propagation Delay

Figure 10 shows the waveforms from running a 100 kHz signal through a level shifter consisting of a single nMOS transistor and two resistors, as shown in Figure 8. This circuit has an average up-shifting propagation delay of 262 nanoseconds and average down-shifting delay of 93 nanoseconds. Interestingly, this circuit has similar but opposite results as the dual npn level shifter, where the up-shifting propagation delay is lower than the down-shifting delay. The output of the nmos also does not have enough time to reach a stable state when the input moves from low to high at 100kHz.

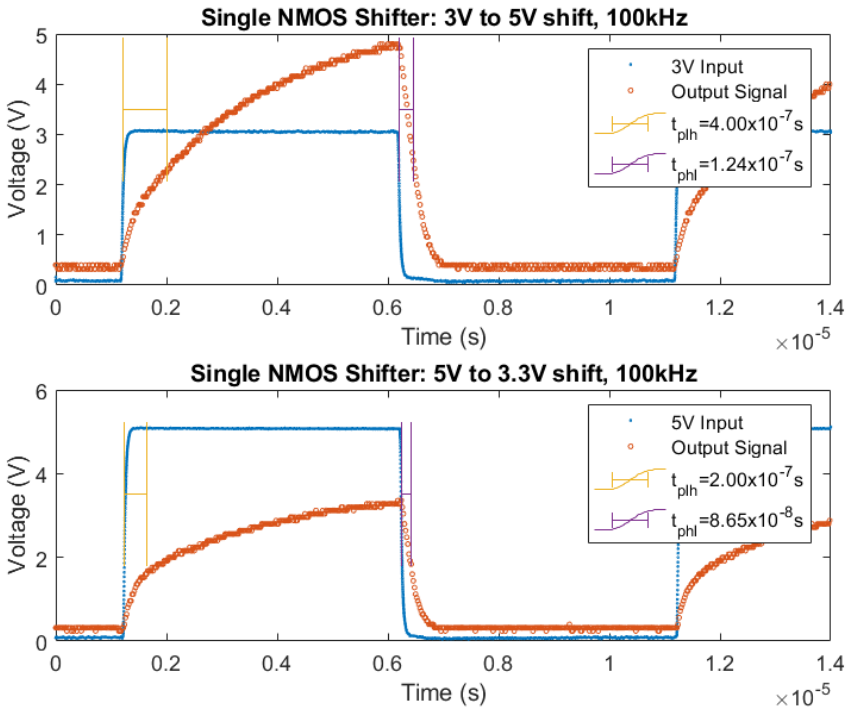

Figure 10: Waveforms generated by a single nMOS transistor level shifter in response to a 100kHz signal.

In Figure 11, we see the results of measuring the input and output voltages as we sent a 100kHz square wave through a bidirectional cross-coupled CMOS level shifter. With the addition of many more CMOS components, the propagation delays of this circuit are greater than those of the previous level shifter we have examined. The up-shifting propagation delay is around 337 nanoseconds while the down-shifting delay is around 112 nanoseconds. This delay may be in part due to the unusual curvature of the square wave that is present in the top subplot of the figure. Nevertheless, this cross-coupled level shifter seems to preserve the shape of the input wave with greater fidelity than the single nMOS transistor.

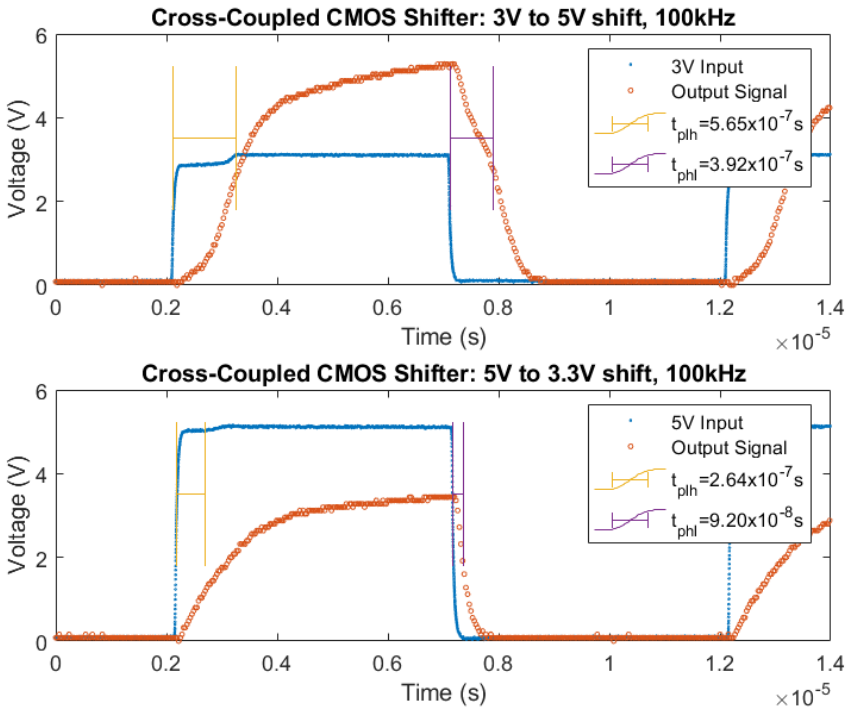

Figure 11: Waveforms from a cross-coupled CMOS level shifter in response to a 100kHz signal.

3.2 Power Consumption

Because level shifters are most prevalent in digital circuitry, where power usage is an increasingly vital consideration, we measured the power consumption of the circuits we created. To do so, we utilized multiple Keithley 2400 SourceMeters in order to both supply the VDDH, or $5V$, and VDDL, or $3.3V$, power rails and measure the power draw of the circuits at those particular nodes. Unfortunately, we were not able to measure the power draw of the circuit at the input signal node, as attempting to measure this with a third Keithley distorted the input signal beyond recognition. Though we could have easily calculated power draw by measuring the current draw and multiplying by the supplied voltage, as in $P = I\text{x}V$, we chose instead to simply utilize the Keithley's ability to determine power draw. The results of these measurements are shown in Table 1.

Circuit Type	$5\text{V}_{up-shifting}$	$3.3\text{V}_{up-shifting}$	$5\text{V}_{down-shifting}$	$3.3\text{V}_{down-shifting}$
Single nMOS	$1.501\text{x}10^{-3}W$	$5.865\text{x}10^{-4}W$	$1.238\text{x}10^{-3}W$	$6.268\text{x}10^{-4}W$
Cross-Coupled CMOS	$1.752\text{x}10^{-3}W$	$5.897\text{x}10^{-4}W$	$4.238\text{x}10^{-4}W$	$4.706\text{x}10^{-4}W$
Single NPN BJT	$1.242\text{x}10^{-3}W$	$4.604\text{x}10^{-4}W$	$1.639\text{x}10^{-3}W$	$1.004\text{x}10^{-3}W$
Dual NPN BJTs	$1.401\text{x}10^{-3}W$	$1.390\text{x}10^{-3}W$	$1.235\text{x}10^{-3}W$	$1.320\text{x}10^{-3}W$

Table 1: Power consumption data, as measured at the node where the power supply rails were being supplied, for each of the level shifting circuits we constructed.

In order to attain a better sense of the meaning of this data, we can look at the percent difference between the level shifters while up-shifting and down-shifting the input signals. We can first sum the power draws of each level shifter during an up-shifting and a down-shifting phase, respectively,

and find the percent difference between these total power consumptions. Using this method, it appears that the single NPN transistor draws the least power during an up-shift, while the dual NPN transistors draw the most. In fact, the single NPN circuit consumes 39% less power than the dual NPN circuit. During a downshift, we found that the single NPN drew the most power, while the cross-coupled CMOS configuration drew 66% less power than the single NPN. We should note, though, that the single NPN performed rather poorly during a downshift, as the output voltage never fell below $1.75V$ in Figure 6.

4 Conclusions

When designing an integrated circuit, we must always keep in mind the trade-offs of various designs in terms of area and performance. While we did not dive too deeply into the specifics of area, we know that resistors on modern ICs are anywhere from hundreds to hundreds of thousands of times larger than MOSFET transistors. Through experimental measurements, we investigated several aspects of the performance of level shifting circuits as well, such as propagation delay and power consumption.

Overall, the CMOS coupled level shifter is the most effective level shifter in terms of power draw, size, and distortion of the signal. This difference in effectiveness becomes more and more pronounced as the scale of the circuit grows, where the smaller sizes of transistors as compared to resistors makes them even better. For hobbyists, or at least those looking to perform level shifting on a more case-by-case basis when working with I2C buses, the nmos level shifter gains an advantage in terms of its ease of prototyping, as it uses only a single transistor and two pull-up resistors and performs reasonably well in terms of power consumption and propagation delay.

References

[1] R. Arora and J. Le. Maximum clock frequency of i2c bus using repeaters. Texas Instruments. [Online]. Available: http://www.ti.com/lit/an/slva695/slva695.pdf

[2] T. G and J. K. Logic level converter using transistors. Electronics Stack Exchange. [Online]. Available: https://electronics.stackexchange.com/questions/296879/logic-level-converter-using-transistors/297092#297092

[3] Lecture 13: Digital circuits (iii). MIT. [Online]. Available: http://web.mit.edu/6.012/www/SP07-L13.pdf

[4] Bi-directional mosfet voltage level converter 3.3v to 5v. Hobby Electronics. [Online]. Available: http://www.hobbytronics.co.uk/mosfet-voltage-level-converter

[5] S. S. Iqbal. Low power robust bidirectional cmos level shifter. Aligarh Muslim University. [Online]. Available: https://www.researchgate.net/publication/316275906_Low_Power_Robust_Bidirectional_CMOS_Level_Shifter