Verifying the Accuracy of the Time Constant in an RC Circuit

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Abstract

The goal of this experiment was to quantitatively observe the voltage decay in a Resistor-Capacitor Circuit. To determine success or failure, we compared the voltage decay with the mathematically derived Time Constant $\left(\frac{1}{R\times C}\right)$ based on the Resistance (R) of a 21kΩ resistor and the Capacitance (C) of a 3.35μF capacitor. Experimentally, we connected a Digital Multimeter (DMM), measuring voltage, in parallel with a resistor. This resistor was placed in series with a charged capacitor and we measured the voltage across the resistor as it changed with time. Our group did three different trials, using one capacitor, using two capacitors in series, and using two capacitors in parallel. Our first two trials went as expected though the graph third trial deviates greatly from the expected results.

Background

An RC circuit is a circuit made up of purely resistors and capacitors. This setup permits the discharging of a capacitor without blowing up or short-circuiting components of the circuit. RC Circuits can be used to filter signals, such as in high-pass filters and low-pass filters. These filters lend protection to DC circuits that may be sensitive to large changes in voltage or non-zero average voltages. Overall, there was not much deviation from the lab procedures [2]. We failed to perform the "Qualitative Demonstration of the RC Circuit" as we did not realize it was a portion of the lab assignment. Additionally, after analyzing the results it appears that we, as a lab group, botched the third trial with two capacitors in parallel. There were only two data points collected between the initial drop in voltage and the final voltage. Additionally, the natural log graph of the values for the third trial dropped off quite rapidly and were not consistent, precise, or accurate.

Theory & Methods

This experiment was run three times. Once with a single charged capacitor in the circuit then twice with two equivalent capacitors. Once with the capacitors connected in series and then again with the capacitors connected in parallel.

Initially the circuit was set up without any power running in it. The capacitor (C) and the resistor (R) were set up in series with each other while the Digital Multimeter (DMM) was set up in parallel with the DC Power source and the capacitor. The Pasco voltmeter was set up in parallel with the resistor as shown in Figure 1 [2].

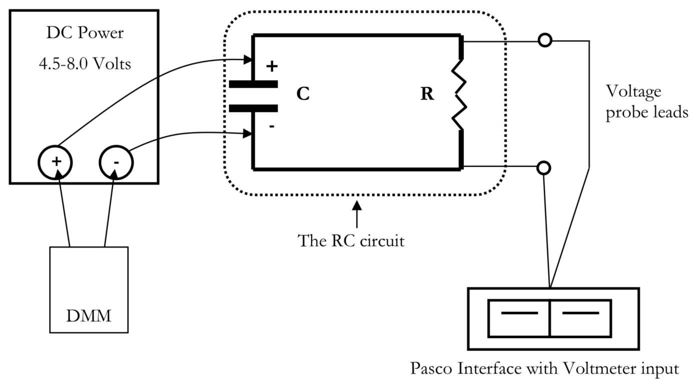


Figure 1: Schematic diagram for charging a capacitor as part of a simple RC circuit. The DMM at the power supply can be used to more precisely monitor the supplied voltage. Once charged the power supply is quickly removed from the circuit leaving the capacitor to discharge across a resistor while a voltage probe monitors and records the decaying electrical potential. [2].

The second trial used a similar circuit design, with a second capacitor in series next to the already existing capacitor (Figure 2).

$$C_T = \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \cdots\right)^{-1} \quad (1)$$

The total capacitance for this trial can be found using Equation 1, and the result is 1.675μF. The capacitances are added in this way because the opposite “sides” of each capacitor are connected to each other decreasing the ‘efficiency’ of all of the capacitors.

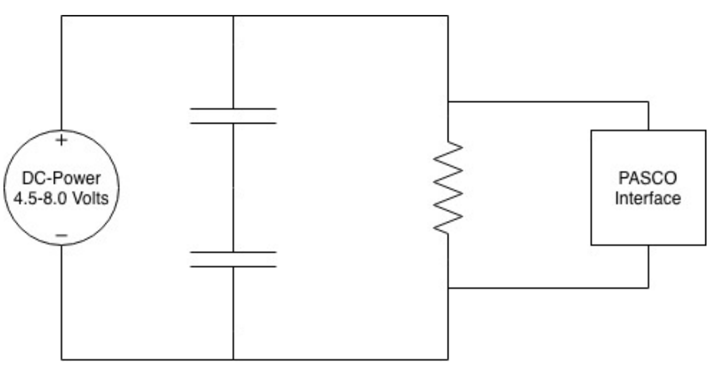


Figure 2: Schematic diagram for charging two capacitors in series as part of a simple RC circuit. The DMM at the power supply can be used to more precisely monitor the supplied voltage. Once charged the power supply is quickly removed from the circuit leaving the capacitor to discharge across a resistor while a voltage probe monitors and records the decaying electrical potential. Each capacitor has a capacitance C equivalent to 3.35μF and the resistor has a resistance R equivalent to 21kΩ.

The third trial used a slightly circuit design, with a second capacitor in parallel next the existing capacitor from the first trial (Figure 3).

$$C_T = C_1 + C_2 + C_3 + \cdots \quad (2)$$

The total capacitance for this trial can be found using Equation 2, and the result is 6.7μF. The capacitances are added in this way because the top plates of the capacitors are connected to each other which is the same as having one capacitor with large plates. This increases the total capacitance.

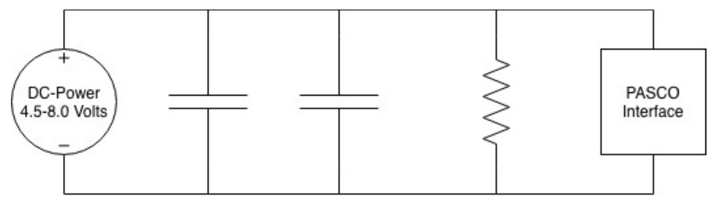


Figure 3: Schematic diagram for charging two capacitors in parallel as part of a simple RC circuit. The DMM at the power supply can be used to more precisely monitor the supplied voltage. Once charged the power supply is quickly removed from the circuit leaving the capacitor to discharge across a resistor while a voltage probe monitors and records the decaying electrical potential. Each capacitor has a capacitance C equivalent to 3.35μF and the resistor has a resistance R equivalent to 21kΩ.

Results

This experiment yielded a large amount of data over the course of all of the trials. The data in Figure 4 is based off of the first trial and is a representation of the voltage as it changed over time in the circuit, after the power source was disconnected. Figures 5, 6, and 7 are the natural logarithm graphs for each trial and compare the voltage for each sample to the starting voltage with the formula $\ln\frac{V}{V_0}$.

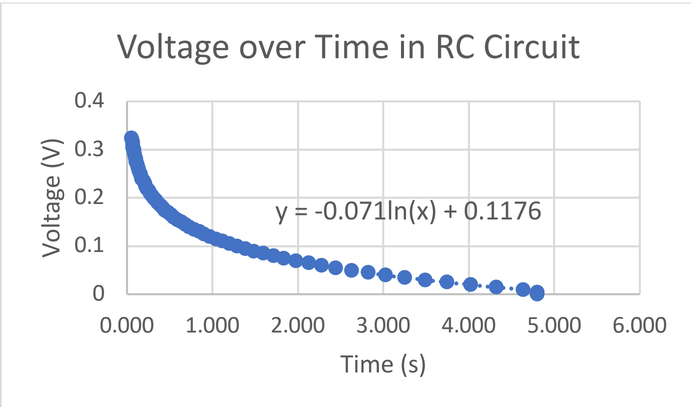


Figure 5: Graph of the voltage as it changed over time in the single-capacitor circuit built for the first trial. As shown, it follows a negative natural logarithm graph [4].

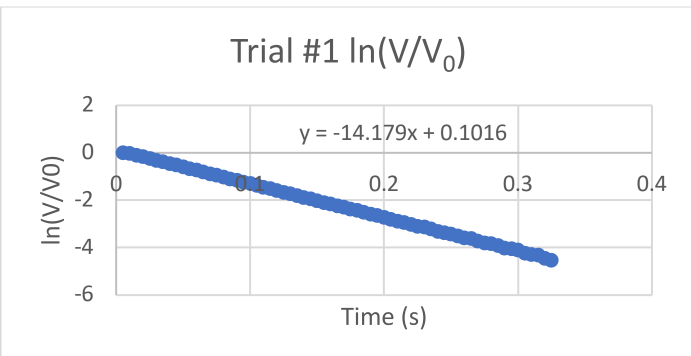


Figure 6: Graph of the natural log of the ratio of the current voltage to the initial voltage as it changed over time in the single-capacitor circuit built for the first trial. As shown, it has a negative linear slope [4].

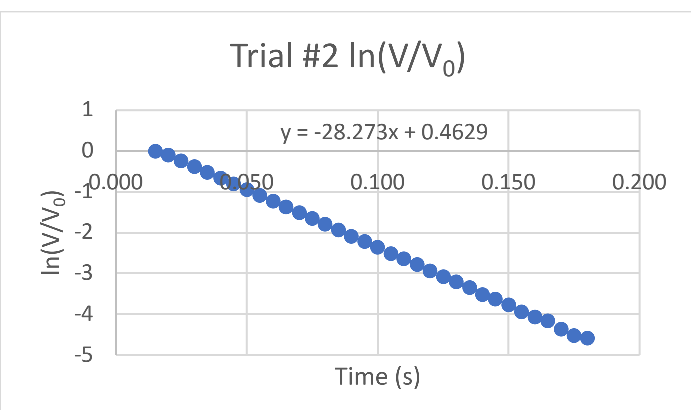


Figure 7: Graph of the natural log of the ratio of the current voltage to the initial voltage as it changed over time in the double-capacitor series circuit built for the second trial. As shown, it has a negative linear slope [4].

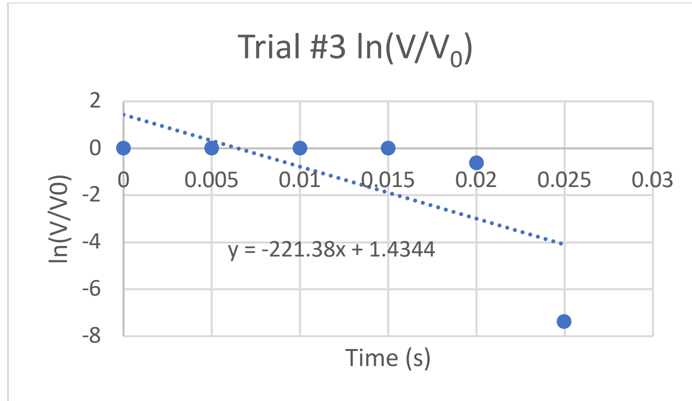


Figure 8: Graph of the natural log of the ratio of the current voltage to the initial voltage as it changed over time in the double-capacitor parallel circuit built for the first trial. As shown, it has a negative linear slope [4].

After graphing the data from each of the trials, we compared the slopes of each of the graphs to the theoretical time constant, τ. For an RC Circuit, τ is found using Equation 3, where R and C are the total resistance and capacitance of the entire circuit.

$$slope = \frac{-1}{RC} \tag{3}$$

$$C = \frac{-1}{R \times slope} \tag{4}$$

Our theoretical and experimental values for τ for each trial can be found in Figure 9. The final row shows the percent difference between each value.

	Theoretical **τ**	Experimental **τ**	Percent Difference
Trial 1 **τ**	0.07303	0.075	2.70
Trial 2 **τ**	0.0365	0.038	4.11
Trial 3 **τ**	0.14606	0.006	95.89
Trial 1 ln Slope	-14.2146411	-14.179	0.25
Trial 2 ln Slope	-28.4292822	-28.273	0.55
Trial 3 ln Slope	-7.10732054	-221.38	3014.82

Figure 9: Table comparing the time constant (τ) for each trial as compared to the theoretical value of τ found by using Equation 3. [4].

"The ultimate check of each test is to compare the slope of the natural log graphs against the theoretical value of $\frac{-1}{RC}$; where R is the value determined from the multimeter ohm measurement and C is based upon the manufacturer's rating (and your calculation if the two were used in series or parallel) [2]. These comparisons can be seen in the bottom 3 rows in

Figure 9. According to the table, the third trial was a failure and we were not able to obtain coherent results. The most probable source of error was Systematic Measurement Uncertainty due to the measurement device (the PASCO and Capstone interfaces) not taking enough samples per second. Another source of error for all of the trials is Random Intrinsic Uncertainty due to the voltage source not being completely constant. Finally, the breadboard and wires used to create the circuit were not an ideal and most likely had a resistance causing a Systematic Measurement Uncertainty.

References

[1] Jefts, David. "Raw Data." ERAU, Daytona Beach, FL, 7 Nov. 2018
[2] Schumacher, Donald. "RC Circuits." ERAU, Daytona Beach, FL, 4 Nov. 2018. Reading.
[3] Tipler, Paul Allen, and Gene Mosca. Physics for Scientists and Engineers. 6th ed., Macmillan, 2007.
[4] Jefts, David. "Plot Data." ERAU, Daytona Beach, FL, 7 Nov. 2018

Calculations

This equation was used in Figure 9 to calculate the percent error between the experiment trials and the expected value.

$$\%\ \mathrm{Error} = \left|\frac{theoretical - experimental}{theoretical}\right| \times 100$$

Equation for adding capacitors in series

$$C_T = \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \cdots\right)^{-1} \qquad (1)$$

Equation for adding capacitors in parallel

$$C_T = C_1 + C_2 + C_3 + \cdots \qquad (2)$$

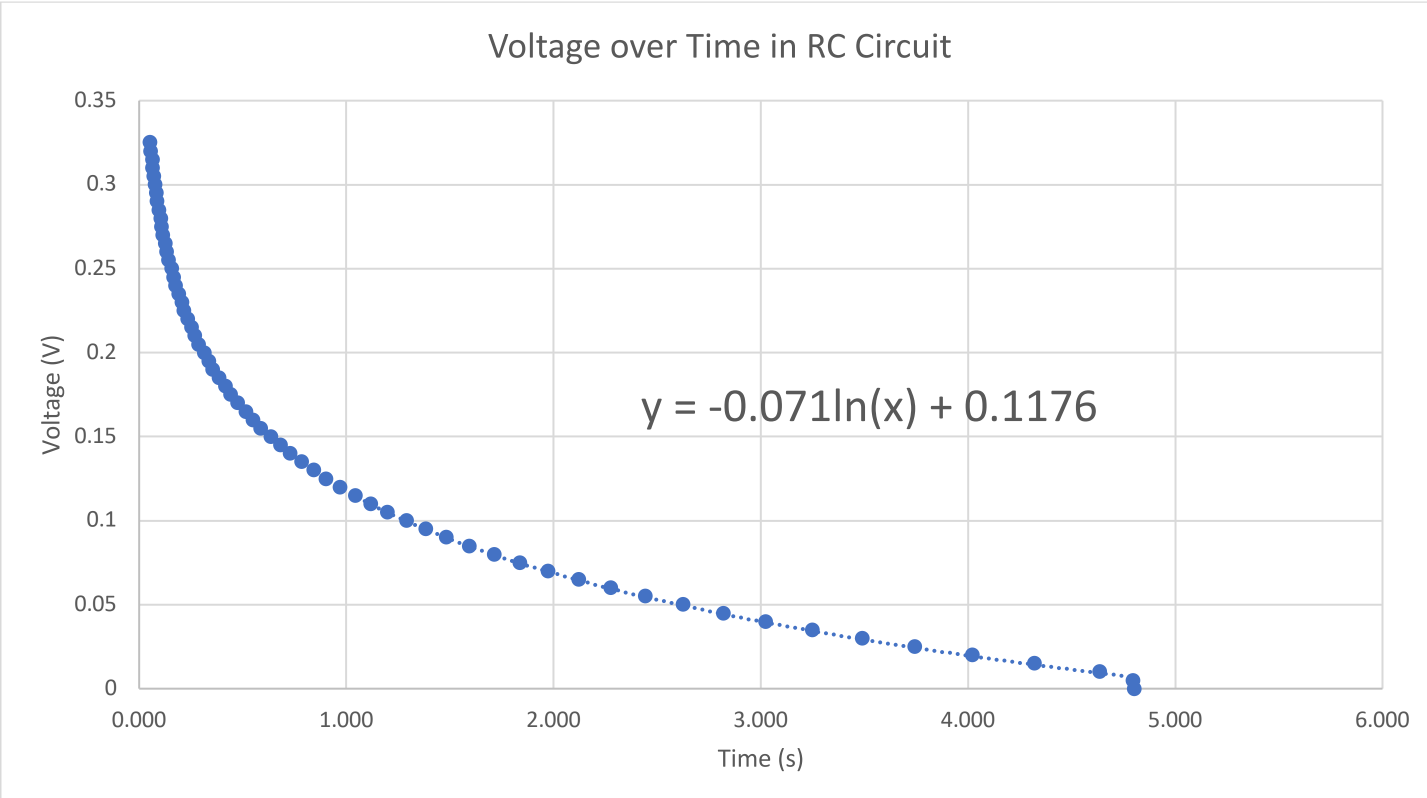
Slope is the slope of the graph $\ln\frac{V}{V_0}$ vs time. R is total resistance and C is total capacitance

$$slope = \frac{-1}{RC} \qquad (3)$$

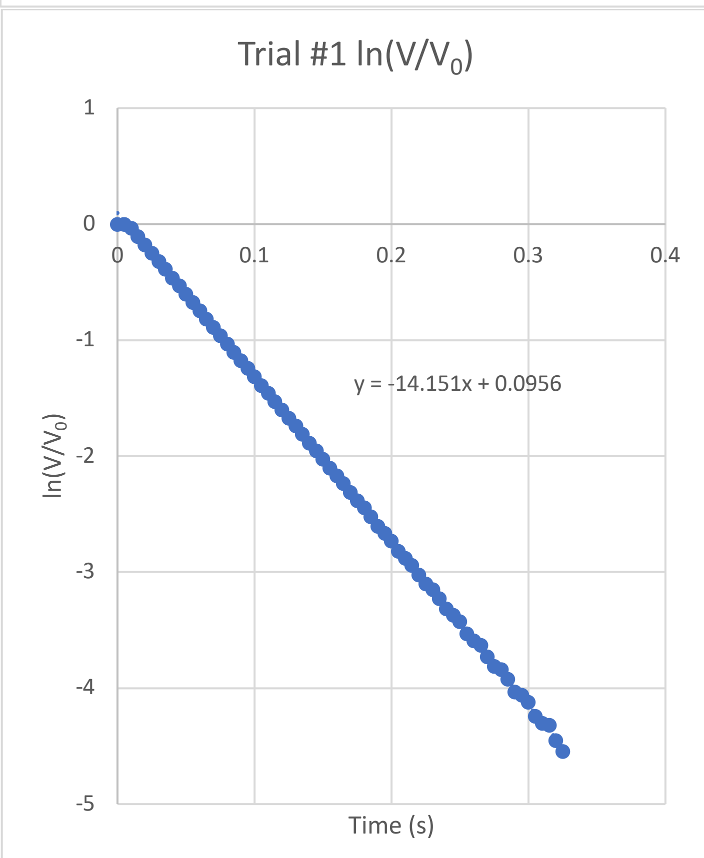
Solve Equation 3 for C to determine experimental capacitance

$$C = \frac{-1}{R \times slope} \qquad (4)$$

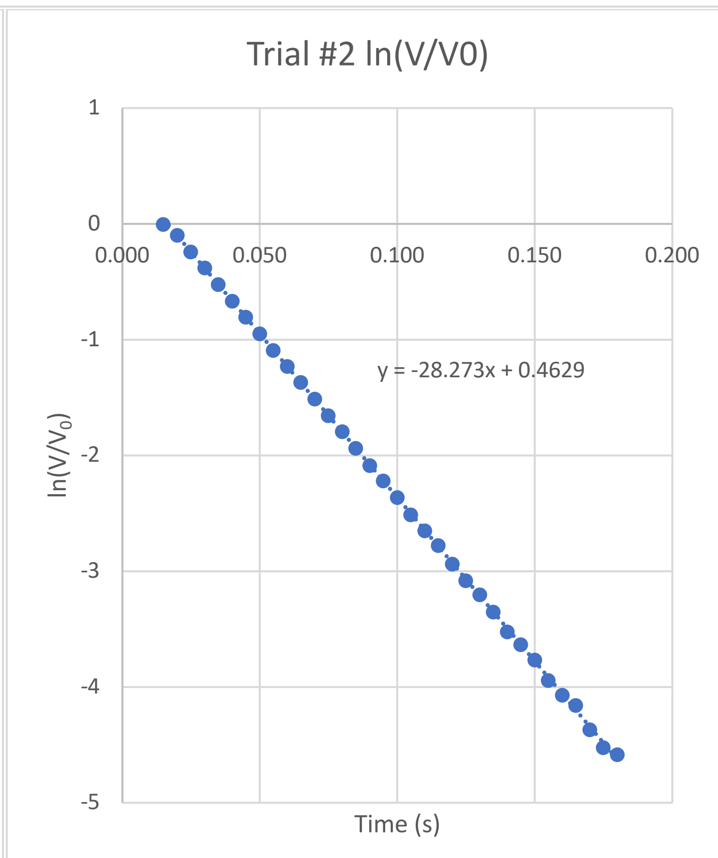
Plot Data



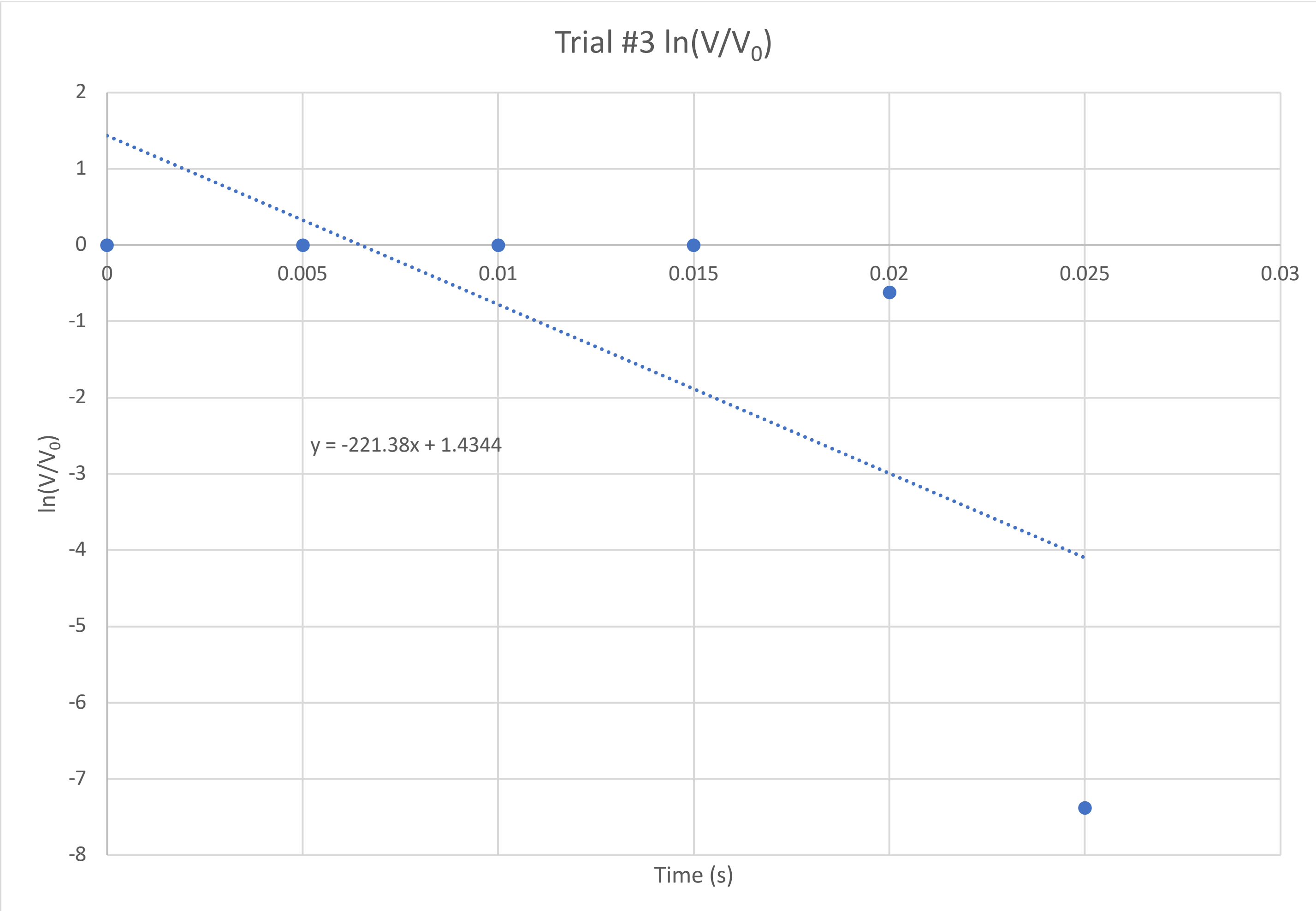
Voltage over Time in RC Circuit
y = -0.071ln(x) + 0.1176
Voltage (V)
Time (s)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0.000
1.000
2.000
3.000
4.000
5.000
6.000



Trial #1 ln(V/V0)
y = -14.151x + 0.0956
ln(V/V0)
Time (s)
1
0
-1
-2
-3
-4
-5
0
0.1
0.2
0.3
0.4



Trial #2 ln(V/V0)
y = -28.273x + 0.4629
ln(V/V0)
Time (s)
1
0
-1
-2
-3
-4
-5
0.000
0.050
0.100
0.150
0.200



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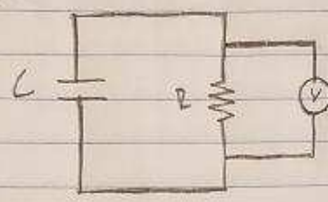
Raw Data

Actual Resistance R_{oa} = 21.8kΩ

$\tau_{ref} = RC = (3.35\times10^{-6})(21.8\times10^{3}\,\Omega) = 0.07303$

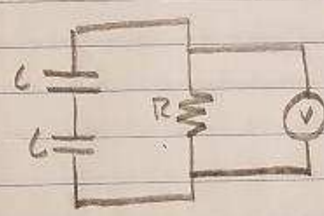
V = 4.8V   disconnected: t = 1.445s
1τ when V = 1.776V   t = 1.52s   } .075s



C = 3.35μF
R = 21.8kΩ

$\tau_{ref} = R\left(\frac{1}{C}+\frac{1}{C}\right)^{-1} = (21.8\times10^{3})\left(\frac{1}{3.35\mu F}+\frac{1}{3.35\mu F}\right)^{-1} = 0.0365$

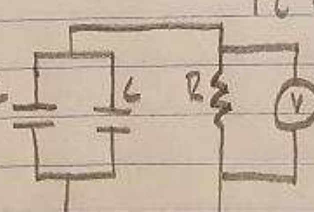
V = 4.8V   disconnected: t = 0.69s
1τ when V = 1.776V   t = 0.728s   } .038s

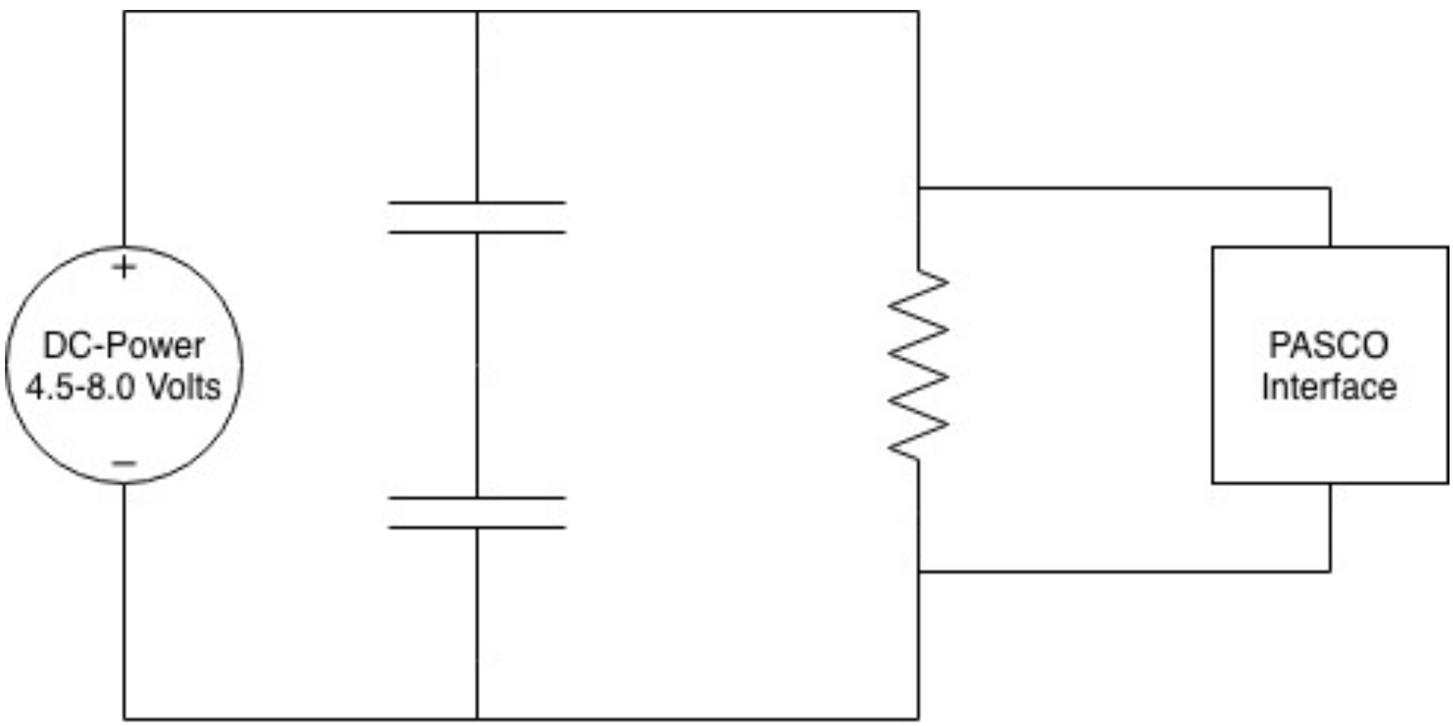


C = 3.35μF
R = 21.8kΩ

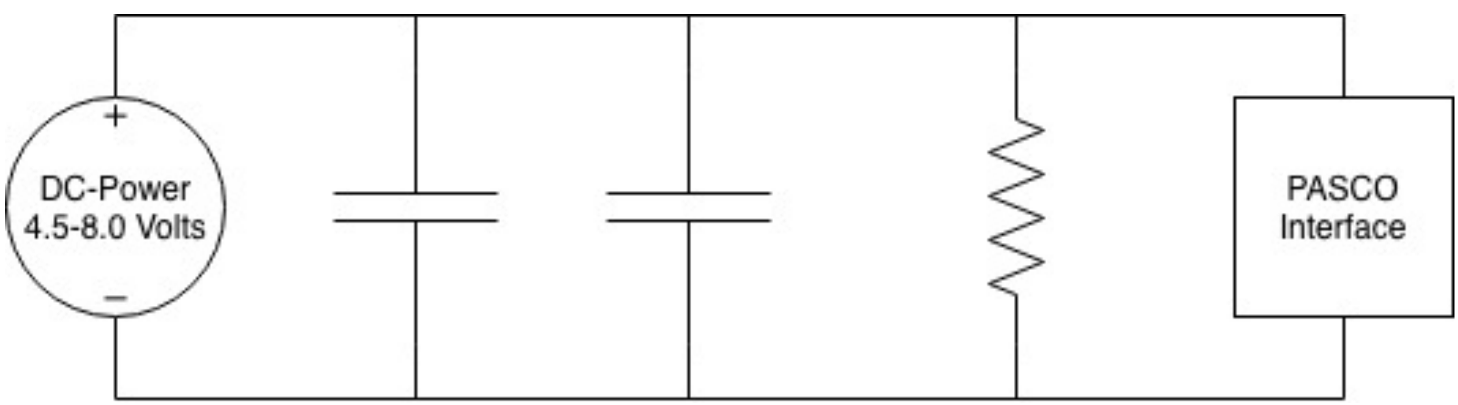
$\tau_{ref} = R(C+C) = (21.8\times10^{3})(3.35\times10^{-6}\cdot 2) = .14606$

V = 4.8   disconnected: t = .74s
1τ when V = 1.776V   t = .7465   } .006





+
DC-Power
4.5-8.0 Volts
–
PASCO
Interface



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DC-Power
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