1. Description

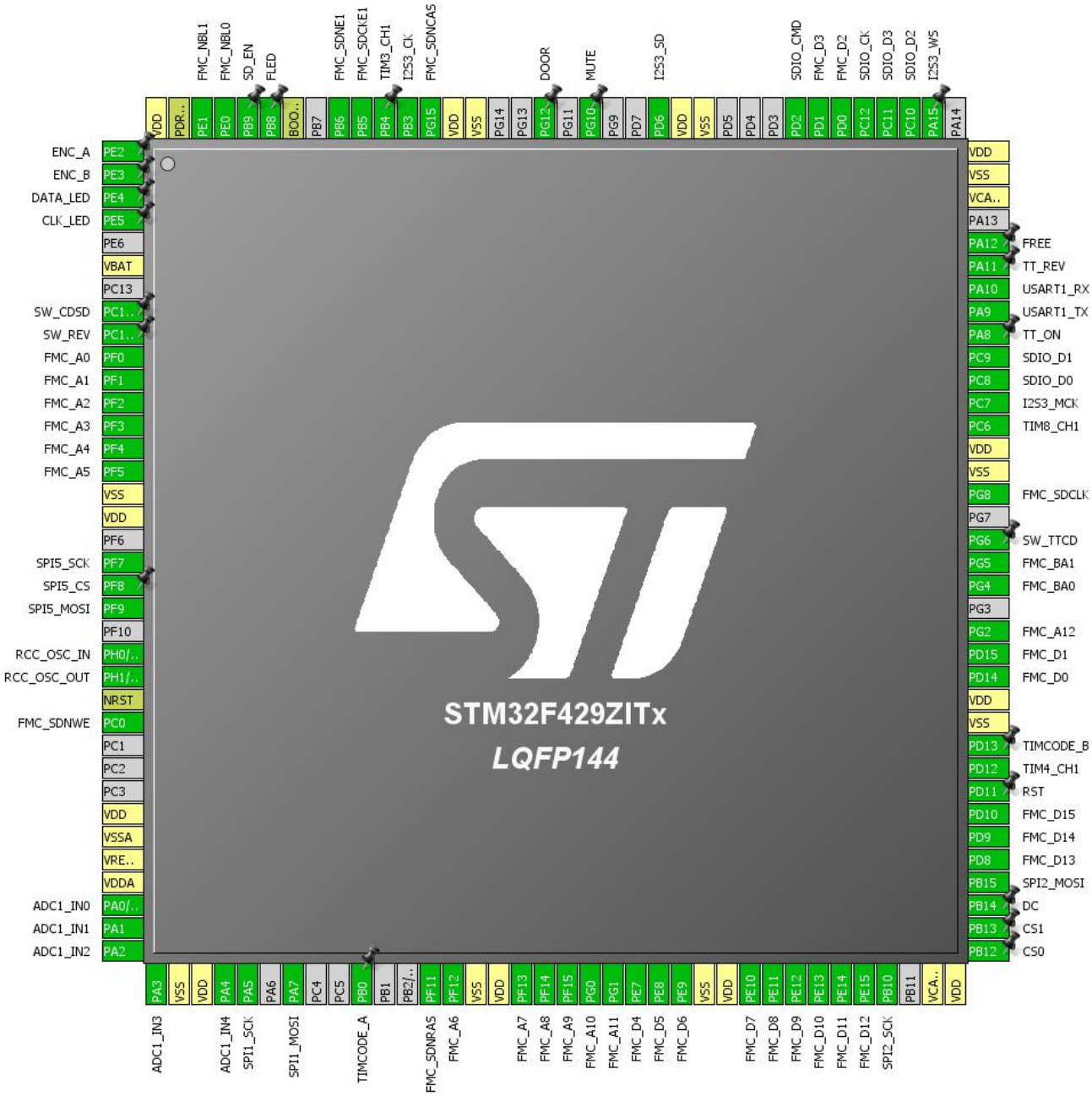
1.1. Project

Project Name	Technics_2000
Board Name	Technics_2000
Generated with:	STM32CubeMX 4.22.0
Date	04/03/2024

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	GPIO_EXTI2	ENC_A
2	PE3 *	I/O	GPIO_Input	ENC_B
3	PE4 *	I/O	GPIO_Output	DATA_LED
4	PE5 *	I/O	GPIO_Output	CLK_LED
6	VBAT	Power		
8	PC14/OSC32_IN *	I/O	GPIO_Input	SW_CDSD
9	PC15/OSC32_OUT *	I/O	GPIO_Input	SW_REV
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	SPI5_SCK	
20	PF8 *	I/O	GPIO_Output	SPI5_CS
21	PF9	I/O	SPI5_MOSI	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	ADC1_IN0	
35	PA1	I/O	ADC1_IN1	
36	PA2	I/O	ADC1_IN2	
37	PA3	I/O	ADC1_IN3	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_IN4	
41	PA5	I/O	SPI1_SCK	
43	PA7	I/O	SPI1_MOSI	
46	PB0	I/O	GPIO_EXTI0	TIMCODE_A

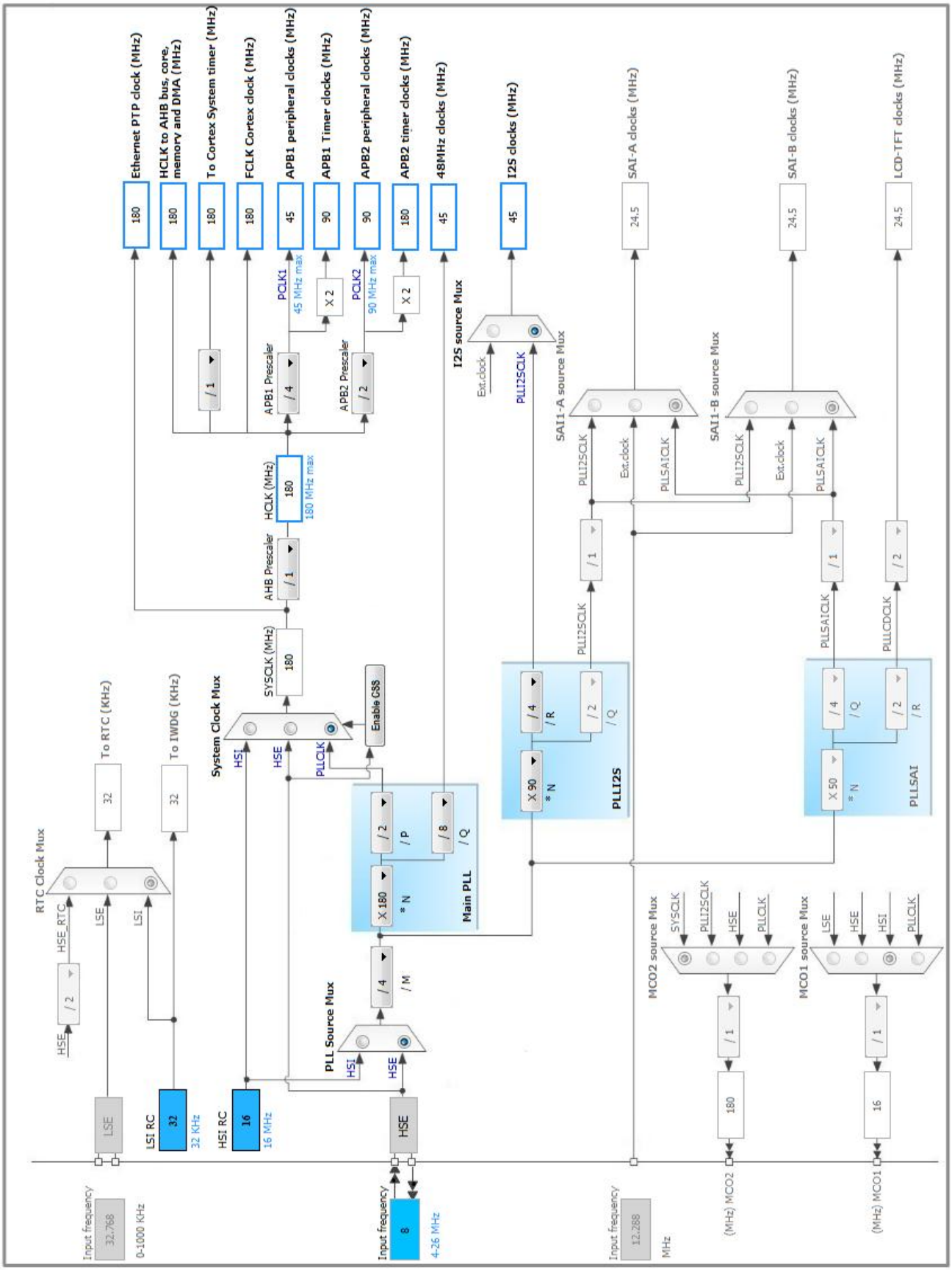
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	SPI2_SCK	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Output	CS0
74	PB13 *	I/O	GPIO_Output	CS1
75	PB14 *	I/O	GPIO_Output	DC
76	PB15	I/O	SPI2_MOSI	
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
80	PD11 *	I/O	GPIO_Output	RST
81	PD12	I/O	TIM4_CH1	
82	PD13 *	I/O	GPIO_Input	TIMCODE_B
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2	I/O	FMC_A12	
89	PG4	I/O	FMC_BA0	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
90	PG5	I/O	FMC_BA1	
91	PG6 *	I/O	GPIO_Input	SW_TTCD
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	I2S3_MCK	
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	SDIO_D1	
100	PA8 *	I/O	GPIO_Output	TT_ON
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11 *	I/O	GPIO_Output	TT_REV
104	PA12 *	I/O	GPIO_Output	FREE
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
110	PA15	I/O	I2S3_WS	
111	PC10	I/O	SDIO_D2	
112	PC11	I/O	SDIO_D3	
113	PC12	I/O	SDIO_CK	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
116	PD2	I/O	SDIO_CMD	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	I2S3_SD	
125	PG10 *	I/O	GPIO_Output	MUTE
127	PG12 *	I/O	GPIO_Input	DOOR
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
133	PB3	I/O	I2S3_CK	
134	PB4	I/O	TIM3_CH1	
135	PB5	I/O	FMC_SDCKE1	
136	PB6	I/O	FMC_SDNE1	
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	FLED
140	PB9 *	I/O	GPIO_Input	SD_EN

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
141	PE0	I/O	FMC_NBL0	
142	PE1	I/O	FMC_NBL1	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

mode: IN1

mode: IN2

mode: IN3

mode: IN4

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. FMC

SDRAM 1

Clock and chip enable: SDCKE1+SDNE1
Internal bank number: 4 banks
Address: 13 bits
Data: 16 bits
Byte enable: set

5.2.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 2
Number of column address bits	**10 bits ***
Number of row address bits	13 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	Disabled
SDRAM common read pipe delay	**1 HCLK clock cycle ***

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**4 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

5.3. I2S3

Mode: Half-Duplex Master
mode: Master Clock Output

5.3.1. Parameter Settings:

Generic Parameters:

Transmission Mode	Mode Master Transmit
Communication Standard	

	LSB First (Right Justified) *
Data and Frame Format	**16 Bits Data on 32 Bits Frame ***
Selected Audio Frequency	**44 KHz ***
Real Audio Frequency	**43.945 KHz ***
Error between Selected and Real	**-0.12 % ***

Clock Parameters:

Clock Source	I2S PLL Clock
Clock Polarity	Low

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

5.5. SDIO

Mode: SD 4 bits Wide bus

5.5.1. Parameter Settings:

SDIO parameters:

SDIOCLK clock divide factor	**4 ***

5.6. SPI1

Mode: Transmit Only Master

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**2.8125 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.7. SPI2

Mode: Transmit Only Master

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**5.625 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.8. SPI5

Mode: Transmit Only Master

5.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**1.40625 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.9. SYS

Timebase Source: SysTick

5.10. TIM1

Clock Source : Internal Clock

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**299 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**179 ***
Internal Clock Division (CKD)	**Division by 4 ***
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.11. TIM2

Clock Source : Internal Clock

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**89 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFFFFFF ***
Internal Clock Division (CKD)	**Division by 4 ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.12. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**359 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1024 ***
Internal Clock Division (CKD)	**Division by 4 ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**10 ***
Fast Mode	Disable
CH Polarity	High

5.13. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**89 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**12499 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**2500 ***
Fast Mode	Disable
CH Polarity	High

5.14. TIM7

mode: Activated

5.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**16483 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.15. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**179 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	**95 ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1 ***
Fast Mode	Disable
CH Polarity	**Low ***
CH Idle State	Reset

5.16. USART1

Mode: Asynchronous

5.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.17. FATFS

mode: SD Card

5.17.1. Set Defines:

Version:

FATFS version	R0.11

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Multilingual Latin 1 (OEM)
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled

FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.17.2. IPs instances:

SDIO/SDMMC:

SDIO instance	SDIO

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB5	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2S3	PC7	I2S3_MCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	I2S3_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	I2S3_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	I2S3_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PE2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ENC_A
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENC_B
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	DATA_LED
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	CLK_LED
	PC14/OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	SW_CDSD
	PC15/OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	SW_REV
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	SPI5_CS
	PB0	GPIO_EXTI0	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	**n/a**	TIMCODE_A
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	CS0
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	CS1
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	DC
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RST
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TIMCODE_B
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW_TTCD
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	TT_ON
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	TT_REV
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	FREE
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MUTE
	PG12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DOOR
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	FLED
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	SD_EN

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA2_Stream3	Memory To Peripheral	Low

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	2	0
EXTI line2 interrupt	true	6	0
TIM1 update interrupt and TIM10 global interrupt	true	5	0
USART1 global interrupt	true	3	0
SPI3 global interrupt	true	0	0
TIM7 global interrupt	true	1	0
DMA2 stream3 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
FMC global interrupt	unused		
SDIO global interrupt	unused		
FPU global interrupt	unused		
SPI5 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	024030_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Technics_2000
Project Folder	C:\Keil_v5\My_Project\SLDZ
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No