
STM32
CubeMX

# 1. Description

## 1.1. Project

| | |
|---|---|
| Project Name | ROTARY_MIXER |
| Board Name | custom |
| Generated with: | STM32CubeMX 6.10.0 |
| Date | 03/08/2025 |

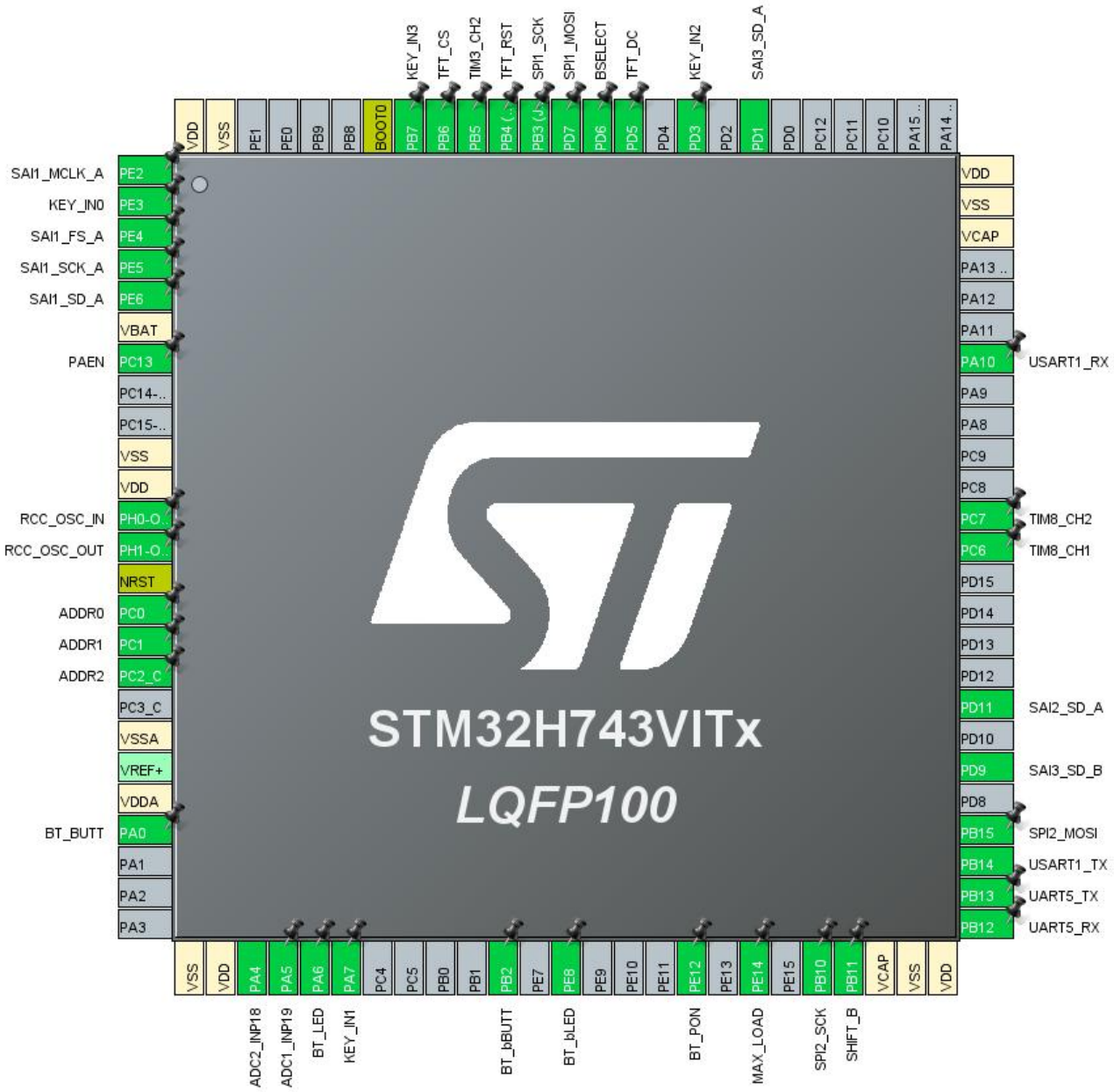
## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32H7 |
| MCU Line | STM32H743/753 |
| MCU name | STM32H743VITx |
| MCU Package | LQFP100 |
| MCU Pin number | 100 |

## 1.3. Core(s) information

| | |
|---|---|
| Core(s) | ARM Cortex-M7 |

## 2. Pinout Configuration



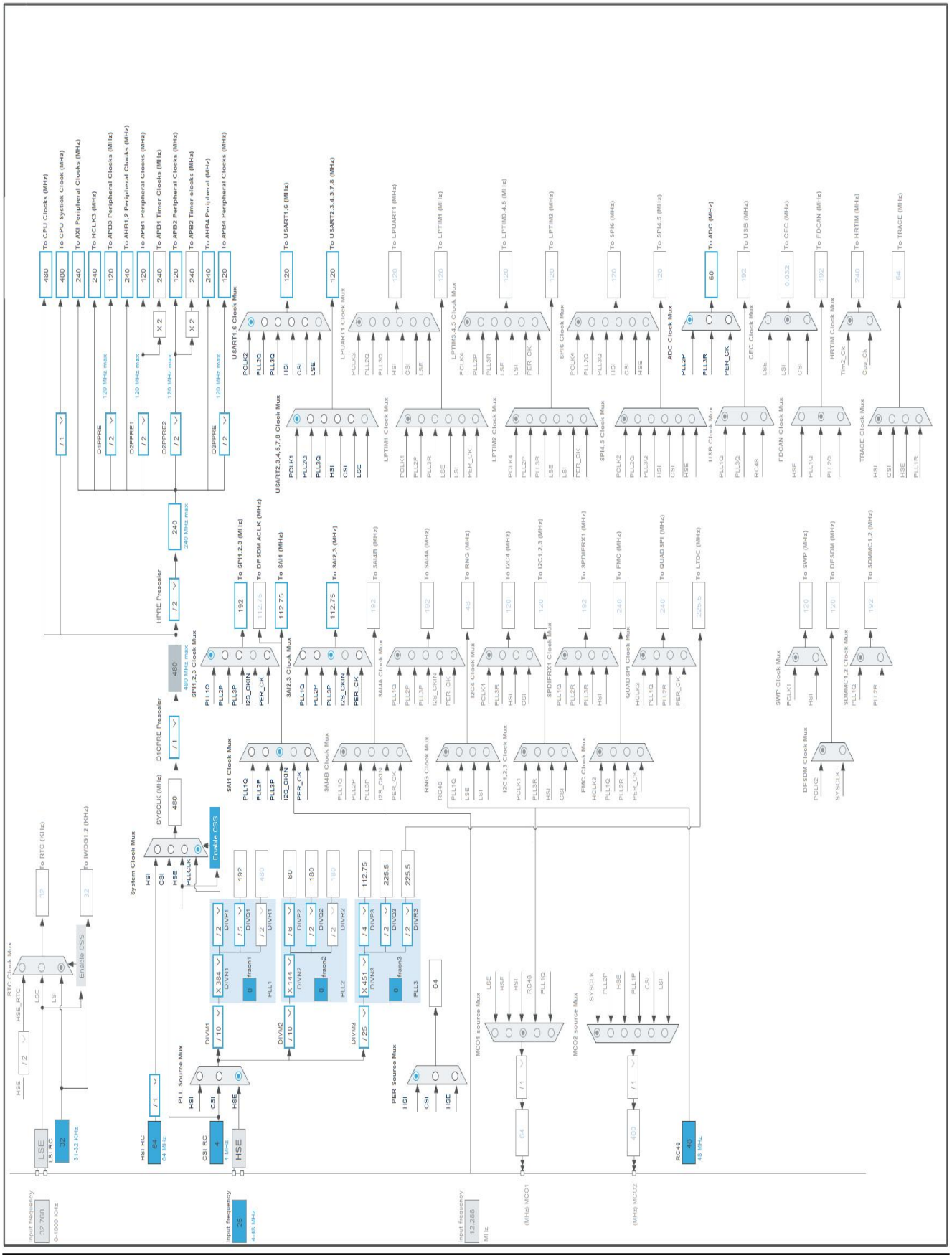
# 3. Pins Configuration

| Pin Number LQFP100 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | PE2 | I/O | SAI1_MCLK_A | |
| 2 | PE3 * | I/O | GPIO_Input | KEY_IN0 |
| 3 | PE4 | I/O | SAI1_FS_A | |
| 4 | PE5 | I/O | SAI1_SCK_A | |
| 5 | PE6 | I/O | SAI1_SD_A | |
| 6 | VBAT | Power | | |
| 7 | PC13 * | I/O | GPIO_Output | PAEN |
| 10 | VSS | Power | | |
| 11 | VDD | Power | | |
| 12 | PH0-OSC_IN (PH0) | I/O | RCC_OSC_IN | |
| 13 | PH1-OSC_OUT (PH1) | I/O | RCC_OSC_OUT | |
| 14 | NRST | Reset | | |
| 15 | PC0 * | I/O | GPIO_Output | ADDR0 |
| 16 | PC1 * | I/O | GPIO_Output | ADDR1 |
| 17 | PC2_C * | I/O | GPIO_Output | ADDR2 |
| 19 | VSSA | Power | | |
| 21 | VDDA | Power | | |
| 22 | PA0 * | I/O | GPIO_Output | BT_BUTT |
| 26 | VSS | Power | | |
| 27 | VDD | Power | | |
| 28 | PA4 | I/O | ADC2_INP18 | |
| 29 | PA5 | I/O | ADC1_INP19 | |
| 30 | PA6 * | I/O | GPIO_Input | BT_LED |
| 31 | PA7 * | I/O | GPIO_Input | KEY_IN1 |
| 36 | PB2 * | I/O | GPIO_Input | BT_bBUTT |
| 38 | PE8 * | I/O | GPIO_Output | BT_bLED |
| 42 | PE12 * | I/O | GPIO_Output | BT_PON |
| 44 | PE14 * | I/O | GPIO_Output | MAX_LOAD |
| 46 | PB10 | I/O | SPI2_SCK | |
| 47 | PB11 * | I/O | GPIO_Input | SHIFT_B |
| 48 | VCAP | Power | | |
| 49 | VSS | Power | | |
| 50 | VDD | Power | | |
| 51 | PB12 | I/O | UART5_RX | |
| 52 | PB13 | I/O | UART5_TX | |
| 53 | PB14 | I/O | USART1_TX | |

| Pin Number LQFP100 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 54 | PB15 | I/O | SPI2_MOSI | |
| 56 | PD9 | I/O | SAI3_SD_B | |
| 58 | PD11 | I/O | SAI2_SD_A | |
| 63 | PC6 | I/O | TIM8_CH1 | |
| 64 | PC7 | I/O | TIM8_CH2 | |
| 69 | PA10 | I/O | USART1_RX | |
| 73 | VCAP | Power | | |
| 74 | VSS | Power | | |
| 75 | VDD | Power | | |
| 82 | PD1 | I/O | SAI3_SD_A | |
| 84 | PD3 * | I/O | GPIO_Input | KEY_IN2 |
| 86 | PD5 * | I/O | GPIO_Output | TFT_DC |
| 87 | PD6 * | I/O | GPIO_Output | BSELECT |
| 88 | PD7 | I/O | SPI1_MOSI | |
| 89 | PB3 (JTDO/TRACESWO) | I/O | SPI1_SCK | |
| 90 | PB4 (NJTRST) * | I/O | GPIO_Output | TFT_RST |
| 91 | PB5 | I/O | TIM3_CH2 | |
| 92 | PB6 * | I/O | GPIO_Output | TFT_CS |
| 93 | PB7 * | I/O | GPIO_Input | KEY_IN3 |
| 94 | BOOT0 | Boot | | |
| 99 | VSS | Power | | |
| 100 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | ROTARY_MIXER |
| Project Folder | C:\Keil_v5\My_Project\XDJX_MIXER_ASSY |
| Toolchain / IDE | MDK-ARM V5.32 |
| Firmware Package Name and Version | STM32Cube FW_H7 V1.11.1 |
| Application Structure | Basic |
| Generate Under Root | No |
| Do not generate the main() | No |
| Minimum Heap Size | 0x200 |
| Minimum Stack Size | 0x400 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Keep User Code when re-generating | Yes |
| Delete previously generated files when not re-generated | No |
| Set all free pins as analog (to optimize the power consumption) | No |
| Enable Full Assert | No |

## 5.3. Advanced Settings - Generated Function Calls

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 1 | SystemClock_Config | RCC |
| 2 | MX_GPIO_Init | GPIO |
| 3 | MX_UART5_Init | UART5 |
| 4 | MX_SAI1_Init | SAI1 |
| 5 | MX_SAI2_Init | SAI2 |
| 6 | MX_SAI3_Init | SAI3 |
| 7 | MX_TIM2_Init | TIM2 |
| 8 | MX_ADC1_Init | ADC1 |
| 9 | MX_ADC2_Init | ADC2 |
| 10 | MX_SPI1_Init | SPI1 |
| 11 | MX_SPI2_Init | SPI2 |

| Rank | Function Name | Peripheral Instance Name |
|---|---|---|
| 12 | MX_TIM8_Init | TIM8 |
| 13 | MX_USART1_UART_Init | USART1 |
| 14 | MX_TIM3_Init | TIM3 |

# 1. Power Consumption Calculator report

## 1.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32H7 |
| Line | STM32H743/753 |
| MCU | STM32H743VITx |
| Datasheet | DS12110_Rev8 |

## 1.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.0 |

## 1.3. Battery Selection

| | |
|---|---|
| Battery | Alkaline(9V) |
| Capacity | 625.0 mAh |
| Self Discharge | 0.3 %/month |
| Nominal Voltage | 9.0 V |
| Max Cont Current | 200.0 mA |
| Max Pulse Current | 0.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

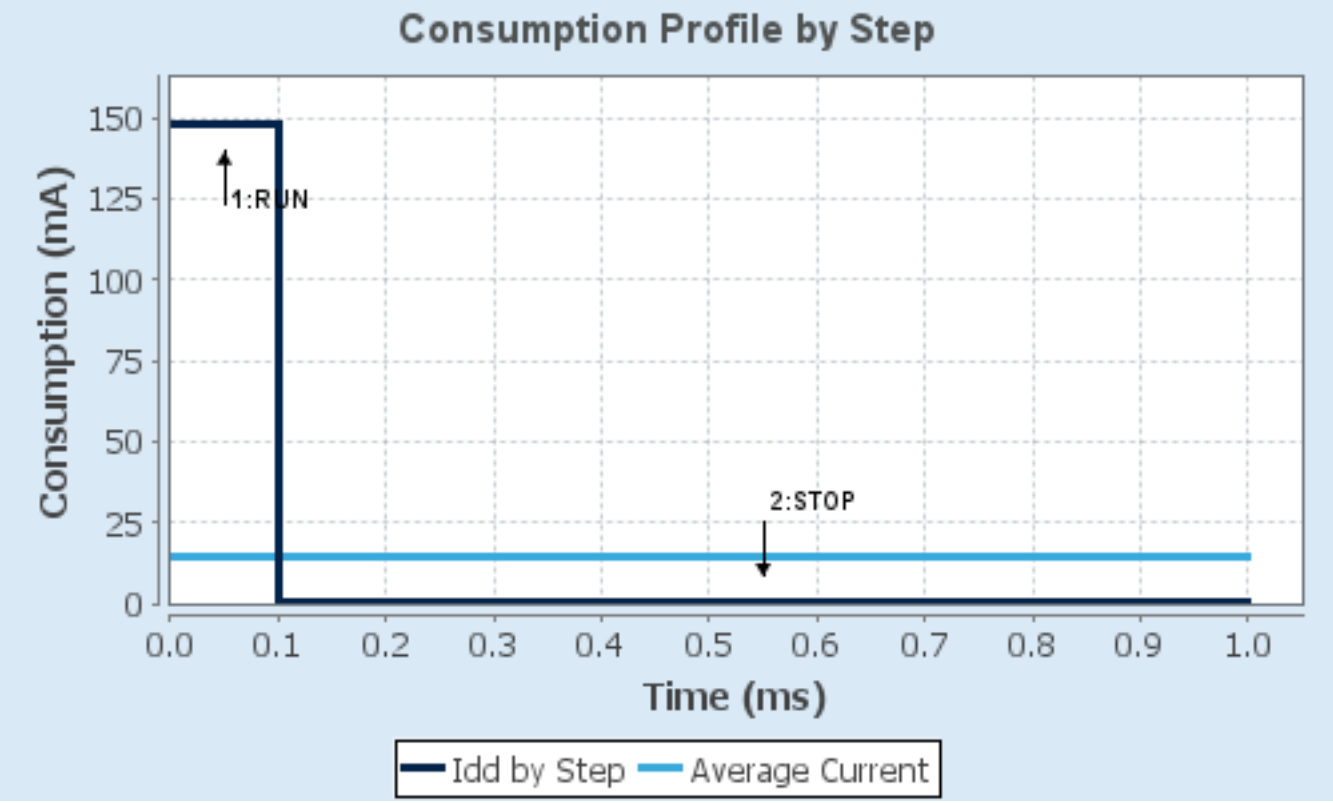
## 1.4. Sequence

| ***Step*** | Step1 | Step2 |
|---|---|---|
| ***Mode*** | RUN | STOP |
| ***Vdd*** | 3.0 | 3.0 |
| ***Voltage Source*** | Battery | Battery |
| ***Range*** | VOS0: Scale0-High | SVOS5: System-Scale5 |
| ***D1 Mode*** | DRUN/CRUN | DSTANDBY |
| ***D2 Mode*** | DRUN | DSTANDBY |
| ***D3 Mode*** | DRUN | DSTOP |
| ***Fetch Type*** | ITCM | NA |
| ***CPU Frequency*** | 480 MHz | 0 Hz |
| ***Clock Configuration*** | HSE BYP PLL | Flash-OFF |
| ***Clock Source Frequency*** | 24 MHz | 0 Hz |
| ***Peripherals*** | | |
| ***Additional Cons.*** | 0 mA | 0 mA |
| ***Average Current*** | 148 mA | 150 µA |
| ***Duration*** | 0.1 ms | 0.9 ms |
| ***DMIPS*** | 1027.0 | 0.0 |
| ***Ta Max*** | 105.02 | 124.98 |
| ***Category*** | In DS Table | In DS Table |

## 1.5. Results

| Sequence Time | 1 ms | Average Current | 14.94 mA |
|---|---|---|---|
| Battery Life | 1 day, 17 hours | Average DMIPS | 1027.2001 DMIPS |

## 1.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

# 2. Peripherals and Middlewares Configuration

## 2.1. ADC1

### mode: IN19

#### 2.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | **ADC 12-bit resolution *** |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| End Of Conversion Selection | End of single conversion |
| Overrun behaviour | Overrun data preserved |
| Left Bit Shift | No bit shift |
| Conversion Data Management Mode | Regular Conversion data stored in DR register only |
| Low Power Auto Wait | Disabled |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Disable |
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 19 |
| Sampling Time | 1.5 Cycles |
| Offset Number | No offset |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Enable Injected Conversions | Disable |

**Analog Watchdog 1:**

| | |
|---|---|
| Enable Analog WatchDog1 Mode | false |

**Analog Watchdog 2:**

| | |
|---|---|
| Enable Analog WatchDog2 Mode | false |

**Analog Watchdog 3:**

| | |
|---|---|
| Enable Analog WatchDog3 Mode | false |

## 2.2. ADC2

## IN18: IN18 Single-ended

### 2.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | **ADC 12-bit resolution *** |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| End Of Conversion Selection | End of single conversion |
| Overrun behaviour | Overrun data preserved |
| Left Bit Shift | No bit shift |
| Conversion Data Management Mode | Regular Conversion data stored in DR register only |
| Low Power Auto Wait | Disabled |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Disable |
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 18 |
| Sampling Time | 1.5 Cycles |
| Offset Number | No offset |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Enable Injected Conversions | Disable |

**Analog Watchdog 1:**

| | |
|---|---|
| Enable Analog WatchDog1 Mode | false |

**Analog Watchdog 2:**

| | |
|---|---|
| Enable Analog WatchDog2 Mode | false |

**Analog Watchdog 3:**

| | |
|---|---|
| Enable Analog WatchDog3 Mode | false |

## 2.3. RCC

## High Speed Clock (HSE): Crystal/Ceramic Resonator

### 2.3.1. Parameter Settings:

**Power Parameters:**

| | |
|---|---|
| SupplySource | PWR_LDO_SUPPLY |
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 0 |

**RCC Parameters:**

| | |
|---|---|
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |
| CSI Calibration Value | 32 |
| HSI Calibration Value | 64 |

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Flash Latency(WS) | 4 WS (5 CPU cycle) |
| Product revision | rev.V |

**PLL range Parameters:**

| | |
|---|---|
| PLL1 clock Input range | Between 2 and 4 MHz |
| PLL2 input frequency range | Between 2 and 4 MHz |
| PLL3 input frequency range | Between 1 and 2 MHz |
| PLL1 clock Output range | Wide VCO range |
| PLL2 clock Output range | Wide VCO range |
| PLL3 clock Output range | Wide VCO range |

## 2.4. SAI1

## Mode: Master with Master Clock Out

## mode: External Synchro Out

### 2.4.1. Parameter Settings:

**SAI A:**

| | |
|---|---|
| Synchronization Inputs | Asynchronous |
| Protocol | Free |
| Audio Mode | Master Transmit |
| Frame Length | **64 bits *** |
| Data Size | **16 Bits *** |
| Slot Size | DataSize |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| First Bit | MSB First |

| | |
|---|---|
| Frame Synchro Active Level Length | **32 *** |
| Frame Synchro Definition | **Channel Identification *** |
| Frame Synchro Polarity | Active Low |
| Frame Synchro Offset | **Before First Bit *** |
| First Bit Offset | 0 |
| Number of Slots (only Even Values) | 2 |
| Slot Active Final Value | **0x00000003 *** |
| Slot Active | **User Setting *** |
| Slot 0 Active | **true *** |
| Slot 1 Active | **true *** |
| Clock Source | SAI PLL Clock |
| Master Clock No Divider | Enabled |
| Audio Frequency | **44.1 KHz *** |
| Real Audio Frequency | **44.042 KHz *** |
| Error between Selected | **0.09 % *** |
| Clock Strobing | **Rising Edge *** |
| Fifo Threshold | Empty |
| Output Drive | **Enabled *** |

**Advanced Parameters:**

| | |
|---|---|
| Synchronization External | **Output SAI A enabled *** |

## 2.5. SAI2

## Mode: Synchronous Slave

### 2.5.1. Parameter Settings:

**SAI A:**

| | |
|---|---|
| Synchronization Inputs | Synchronous with other block of same SAI |
| Protocol | Free |
| Audio Mode | Slave Receive |
| Frame Length (only Even Values) | **32 *** |
| Data Size | **16 Bits *** |
| Slot Size | DataSize |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| First Bit | MSB First |
| Frame Synchro Active Level Length | 1 |

| | |
|---|---|
| Frame Synchro Definition | Start Frame |
| Frame Synchro Polarity | Active Low |
| Frame Synchro Offset | First Bit |
| First Bit Offset | 0 |
| Number of Slots | **2 *** |
| Slot Active Final Value | **0x00000003 *** |
| Slot Active | **User Setting *** |
| Slot 0 Active | **true *** |
| Slot 1 Active | **true *** |
| Clock Strobing | **Rising Edge *** |
| Fifo Threshold | Empty |
| Output Drive | **Enabled *** |

## 2.6. SAI3

## Mode: Synchronous Slave

## Mode: Synchronous Slave

### 2.6.1. Parameter Settings:

**SAI A:**

| | |
|---|---|
| Synchronization Inputs | **Synchronous with other SAI, SAI1 *** |
| Protocol | Free |
| Audio Mode | Slave Receive |
| Frame Length (only Even Values) | **64 *** |
| Data Size | **16 Bits *** |
| Slot Size | DataSize |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| First Bit | MSB First |
| Frame Synchro Active Level Length | **32 *** |
| Frame Synchro Definition | **Channel Identification *** |
| Frame Synchro Polarity | Active Low |
| Frame Synchro Offset | First Bit |
| First Bit Offset | 0 |
| Number of Slots (only Even Values) | 2 |
| Slot Active Final Value | **0x00000003 *** |
| Slot Active | **User Setting *** |
| Slot 0 Active | |

| | |
|---|---|
| | **true *** |
| Slot 1 Active | **true *** |
| Clock Strobing | **Rising Edge *** |
| Fifo Threshold | Empty |
| Output Drive | **Enabled *** |

**SAI B:**

| | |
|---|---|
| Synchronization Inputs | Synchronous with other block of same SAI |
| Protocol | Free |
| Audio Mode | Slave Receive |
| Frame Length (only Even Values) | **64 *** |
| Data Size | **16 Bits *** |
| Slot Size | DataSize |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| First Bit | MSB First |
| Frame Synchro Active Level Length | **32 *** |
| Frame Synchro Definition | **Channel Identification *** |
| Frame Synchro Polarity | Active Low |
| Frame Synchro Offset | First Bit |
| First Bit Offset | 0 |
| Number of Slots (only Even Values) | 2 |
| Slot Active Final Value | **0x00000003 *** |
| Slot Active | **User Setting *** |
| Slot 0 Active | **true *** |
| Slot 1 Active | **true *** |
| Real Audio Frequency | 0 |
| Error between Selected | 0 |
| Clock Strobing | **Rising Edge *** |
| Fifo Threshold | Empty |
| Output Drive | **Enabled *** |

## 2.7. SPI1

## Mode: Transmit Only Master

### 2.7.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |

| | |
|---|---|
| Data Size | **8 Bits *** |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | **8 *** |
| Baud Rate | **24.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |
| Fifo Threshold | Fifo Threshold 01 Data |
| Tx Crc Initialization Pattern | All Zero Pattern |
| Rx Crc Initialization Pattern | All Zero Pattern |
| Nss Polarity | Nss Polarity Low |
| Master Ss Idleness | 00 Cycle |
| Master Inter Data Idleness | 00 Cycle |
| Master Receiver Auto Susp | Disable |
| Master Keep Io State | **Master Keep Io State Enable *** |
| IO Swap | Disabled |

## 2.8. SPI2

## Mode: Transmit Only Master

### 2.8.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | **16 Bits *** |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | **8 *** |
| Baud Rate | **24.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

| | |
|---|---|
| Fifo Threshold | Fifo Threshold 01 Data |
| Tx Crc Initialization Pattern | All Zero Pattern |
| Rx Crc Initialization Pattern | All Zero Pattern |
| Nss Polarity | Nss Polarity Low |
| Master Ss Idleness | 00 Cycle |
| Master Inter Data Idleness | 00 Cycle |
| Master Receiver Auto Susp | Disable |
| Master Keep Io State | **Master Keep Io State Enable *** |
| IO Swap | Disabled |

## 2.9. SYS

**Timebase Source: SysTick**

## 2.10. TIM2

**Clock Source : Internal Clock**

### 2.10.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **99 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **999 *** |
| Internal Clock Division (CKD) | **Division by 2 *** |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

## 2.11. TIM3

**Clock Source : Internal Clock**

**Channel2: PWM Generation CH2**

### 2.11.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **239 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **999 *** |

| | |
|---|---|
| Internal Clock Division (CKD) | **Division by 4 *** |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## 2.12. TIM8

## Combined Channels: Encoder Mode

### 2.12.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 65535 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 16 bits value) | 0 |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

**Encoder:**

| | |
|---|---|
| Encoder Mode | Encoder Mode TI1 |
| ____ Parameters for Channel 1 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter | **5 *** |
| ____ Parameters for Channel 2 ____ | |
| Polarity | Rising Edge |
| IC Selection | Direct |

| | |
|---|---|
| Prescaler Division Ratio | No division |
| Input Filter | **5 *** |

## 2.13. UART5

## Mode: Asynchronous

### 2.13.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |
| ClockPrescaler | 1 |
| Fifo Mode | FIFO mode disable |
| Txfifo Threshold | 1 eighth full configuration |
| Rxfifo Threshold | 1 eighth full configuration |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## 2.14. USART1

## Mode: Asynchronous

### 2.14.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **31250 *** |
| Word Length | 8 Bits (including Parity) |

| | |
|---|---|
| Parity | None |
| Stop Bits | 1 |

### Advanced Parameters:

| | |
|---|---|
| Data Direction | **Receive Only *** |
| Over Sampling | 16 Samples |
| Single Sample | Disable |
| ClockPrescaler | 1 |
| Fifo Mode | Disable |
| Txfifo Threshold | 1 eighth full configuration |
| Rxfifo Threshold | 1 eighth full configuration |

### Advanced Features:

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 3. System Configuration

## 3.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PA5 | ADC1_INP19 | Analog mode | No pull-up and no pull-down | n/a | |
| ADC2 | PA4 | ADC2_INP18 | Analog mode | No pull-up and no pull-down | n/a | |
| RCC | PH0-OSC_IN (PH0) | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1-OSC_OUT (PH1) | RCC_OSC_OUT | n/a | n/a | n/a | |
| SAI1 | PE2 | SAI1_MCLK_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE4 | SAI1_FS_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE5 | SAI1_SCK_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE6 | SAI1_SD_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| SAI2 | PD11 | SAI2_SD_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| SAI3 | PD9 | SAI3_SD_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD1 | SAI3_SD_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| SPI1 | PD7 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PB3 (JTDO/TRACESWO) | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| SPI2 | PB10 | SPI2_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Medium *** | |
| | PB15 | SPI2_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Medium *** | |
| TIM3 | PB5 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM8 | PC6 | TIM8_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC7 | TIM8_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| UART5 | PB12 | UART5_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB13 | UART5_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| USART1 | PB14 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA10 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| GPIO | PE3 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | KEY_IN0 |
| | PC13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PAEN |
| | PC0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | ADDR0 |
| | PC1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | ADDR1 |
| | PC2_C | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | ADDR2 |
| | PA0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Medium *** | BT_BUTT |
| | PA6 | GPIO_Input | Input mode | **Pull-up *** | **n/a** | BT_LED |
| | PA7 | GPIO_Input | Input mode | No pull-up and no pull-down | **n/a** | KEY_IN1 |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PB2 | GPIO_Input | Input mode | **Pull-up *** | **n/a** | BT_bBUTT |
| | PE8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Medium *** | BT_bLED |
| | PE12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Medium *** | BT_PON |
| | PE14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Very High *** | MAX_LOAD |
| | PB11 | GPIO_Input | Input mode | **Pull-up *** | **n/a** | SHIFT_B |
| | PD3 | GPIO_Input | Input mode | No pull-up and no pull-down | **n/a** | KEY_IN2 |
| | PD5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Very High *** | TFT_DC |
| | PD6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Medium *** | BSELECT |
| | PB4 (NJTRST) | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Medium *** | TFT_RST |
| | PB6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **Very High *** | TFT_CS |
| | PB7 | GPIO_Input | Input mode | No pull-up and no pull-down | **n/a** | KEY_IN3 |

### 3.2. DMA configuration

nothing configured in DMA service

### 3.3. BDMA configuration

nothing configured in DMA service

### 3.4. MDMA configuration

nothing configured in DMA service

## 3.5. NVIC configuration

### 3.5.1. NVIC

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 15 | 0 |
| TIM2 global interrupt | true | 3 | 0 |
| USART1 global interrupt | true | 5 | 0 |
| TIM8 update interrupt and TIM13 global interrupt | true | 6 | 0 |
| UART5 global interrupt | true | 3 | 0 |
| SAI1 global interrupt | true | 0 | 0 |
| SAI2 global interrupt | true | 1 | 0 |
| SAI3 global interrupt | true | 2 | 0 |
| PVD and AVD interrupts through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1 and ADC2 global interrupts | unused | | |
| TIM3 global interrupt | unused | | |
| SPI1 global interrupt | unused | | |
| SPI2 global interrupt | unused | | |
| TIM8 break interrupt and TIM12 global interrupt | unused | | |
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | unused | | |
| TIM8 capture compare interrupt | unused | | |
| FPU global interrupt | unused | | |
| HSEM1 global interrupt | unused | | |

### 3.5.2. NVIC Code generation

| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|---|---|---|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| | | | |

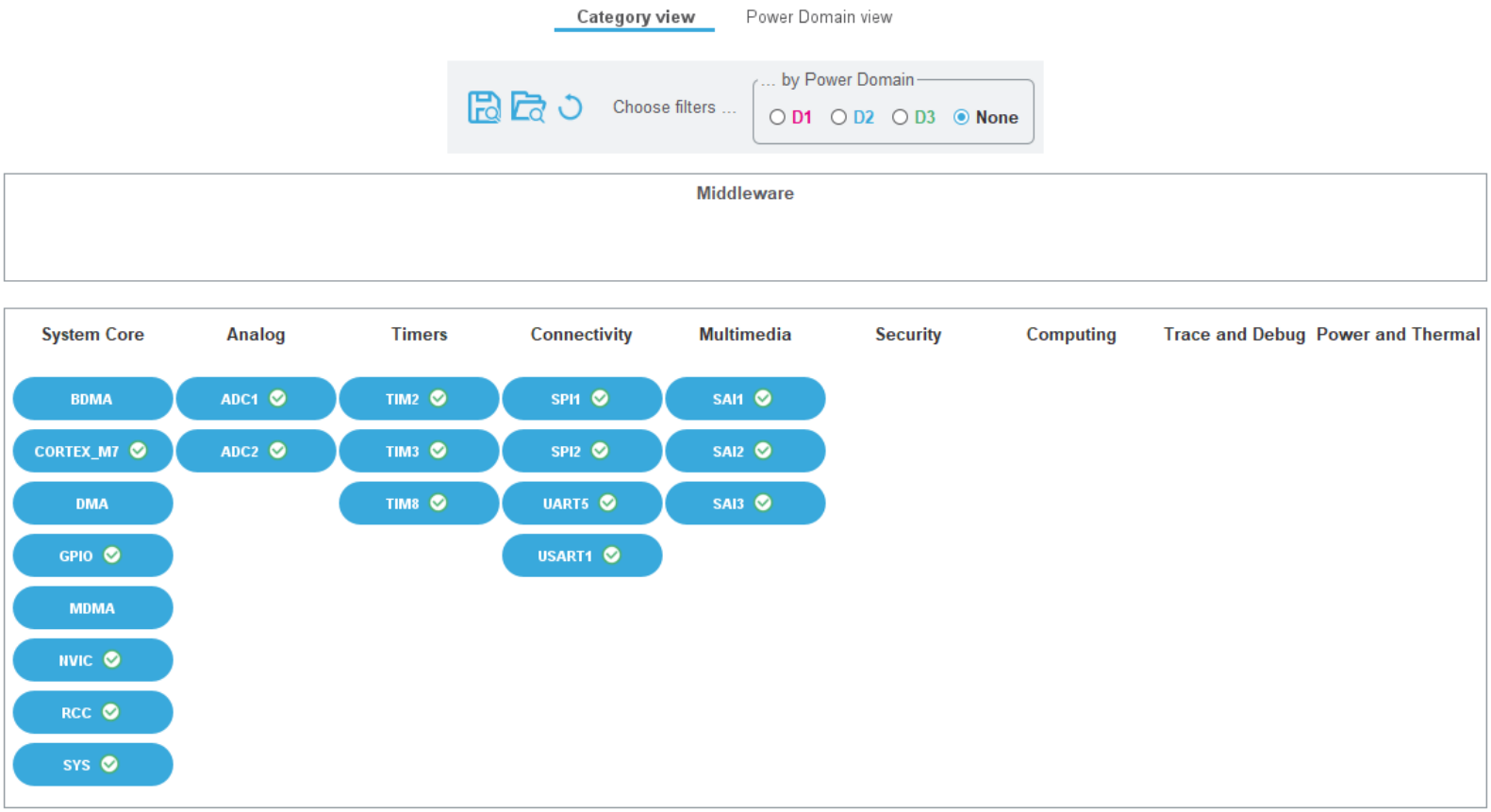
| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|---|---|---|
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | true | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | true | false |
| System tick timer | false | true | true |
| TIM2 global interrupt | false | true | true |
| USART1 global interrupt | false | true | true |
| TIM8 update interrupt and TIM13 global interrupt | false | true | true |
| UART5 global interrupt | false | true | true |
| SAI1 global interrupt | false | true | true |
| SAI2 global interrupt | false | true | true |
| SAI3 global interrupt | false | true | true |

*** User modified value**

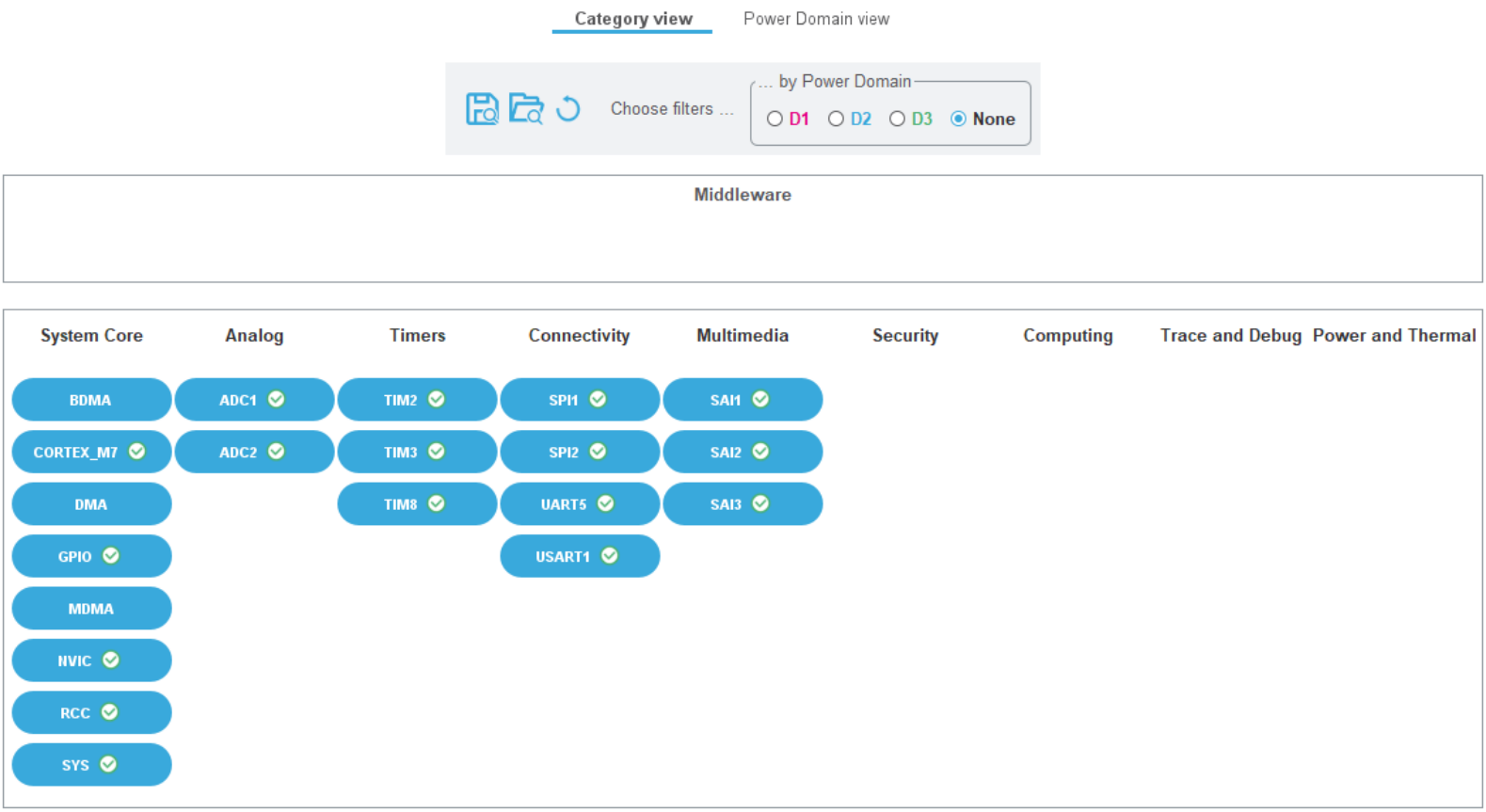
# 4. System Views

## 4.1. Category view

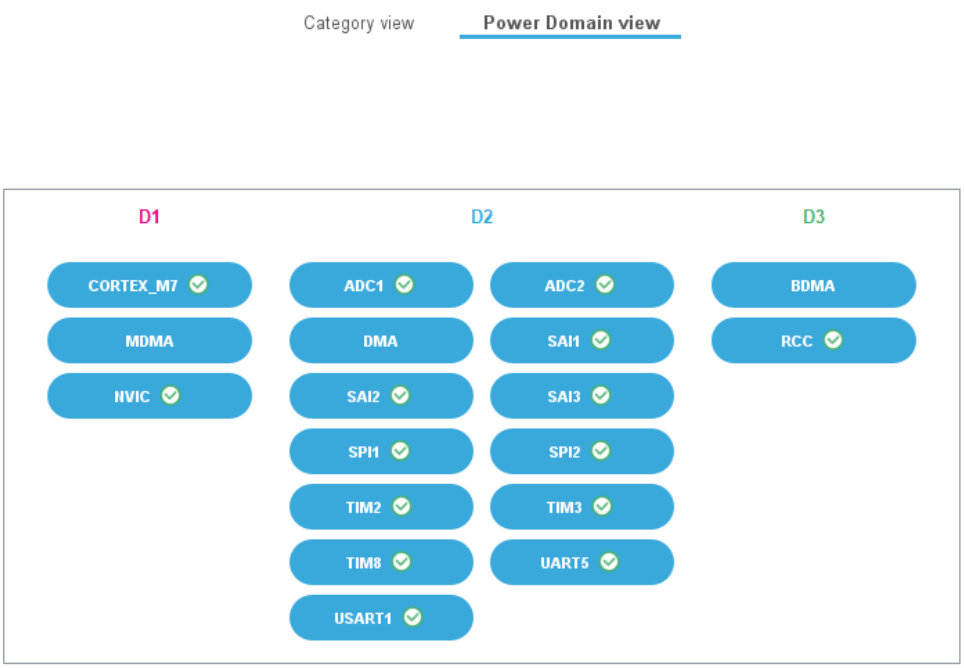
### *4.1.1. Current*



### *4.1.2. Without filters*



## 4.2. Power Domain view



# 5. Docs & Resources

| Type | Link |
|---|---|
| BSDL files | https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip |
| IBIS models | https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip |
| System View Description | https://www.st.com/resource/en/svd/stm32h7-svd.zip |
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| Application Notes for related Tools & Software | https://www.st.com/resource/en/application_note/an4435-guidelines-for-obtaining-ulcsaiec-607301603351-class-b-certification-in-any-stm32-application-stmicroelectronics.pdf |
| Application Notes for related Tools & Software | https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf |
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| Application Notes for related Tools & Software | https://www.st.com/resource/en/application_note/an5361-getting-started-with-projects-based-on-dualcore-stm32h7-microcontrollers-in-stm32cubeide-stmicroelectronics.pdf |
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