

1. Description

1.1. Project

Project Name	XDJX
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	03/17/2025

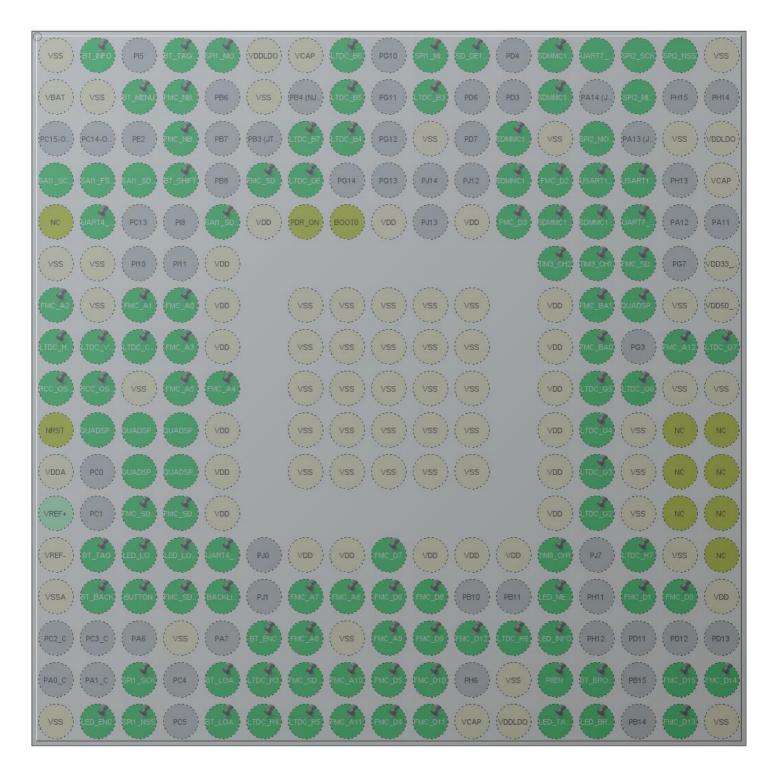
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750XBHx
MCU Package	TFBGA240
MCU Pin number	265

1.3. Core(s) information

Core(s)	ARM Cortex-M7	

2. Pinout Configuration



TFBGA240 +25 (Top view)

3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after reset)		Function(s)	
A1	VSS	Power		
A2	PI6 *	I/O	GPIO_Input	BT_INFO
A4	PI4 *	I/O	GPIO_Input	BT_TAGLIST
A5	PB5	I/O	SPI1_MOSI	
A6	VDDLDO	Power		
A7	VCAP	Power		
A8	PK5	I/O	LTDC_B6	
A10	PG9	I/O	SPI1_MISO	
A11	PD5 *	I/O	GPIO_Input	SD_DETECT
A13	PC10	I/O	SDMMC1_D2	
A14	PA15 (JTDI)	I/O	UART7_TX	
A15	PI1	I/O	SPI2_SCK	
A16	PI0	I/O	SPI2_NSS	
A17	VSS	Power		
B1	VBAT	Power		
B2	VSS	Power		
B3	PI7 *	I/O	GPIO_Input	BT_MENU
B4	PE1	I/O	FMC_NBL1	
B6	VSS	Power		
B8	PK4	I/O	LTDC_B5	
B10	PJ15	I/O	LTDC_B3	
B13	PC11	I/O	SDMMC1_D3	
B15	PI2	I/O	SPI2_MISO	
C4	PE0	I/O	FMC_NBL0	
C7	PK6	I/O	LTDC_B7	
C8	PK3	I/O	LTDC_B4	
C10	VSS	Power		
C12	PC12	I/O	SDMMC1_CK	
C13	VSS	Power		
C14	PI3	I/O	SPI2_MOSI	
C16	VSS	Power		
C17	VDDLDO	Power		
D1	PE5	I/O	SAI1_SCK_A	
D2	PE4	I/O	SAI1_FS_A	
D3	PE3	I/O	SAI1_SD_B	
D4	PB9 *	I/O	GPIO_Input	BT_SHIFT

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)		()	
D6	PG15	I/O	FMC_SDNCAS	
D7	PK7	I/O	LTDC_DE	
D12	PD2	I/O	SDMMC1_CMD	
D13	PD0	I/O	FMC_D2	
D14	PA10	I/O	USART1_RX	
D15	PA9	I/O	USART1_TX	
D17	VCAP	Power		
E1	NC	NC		
E2	PI9	I/O	UART4_RX	
E5	PE6	I/O	SAI1_SD_A	
E6	VDD	Power		
E7	PDR_ON	Reset		
E8	BOOT0	Boot		
E9	VDD	Power		
E11	VDD	Power		
E12	PD1	I/O	FMC_D3	
E13	PC8	I/O	SDMMC1_D0	
E14	PC9	I/O	SDMMC1_D1	
E15	PA8	I/O	UART7_RX	
F1	VSS	Power		
F2	VSS	Power		
F5	VDD	Power		
F13	PC7	I/O	TIM3_CH2	
F14	PC6	I/O	TIM3_CH1	
F15	PG8	I/O	FMC_SDCLK	
F17	VDD33_USB	Power		
G1	PF2	I/O	FMC_A2	
G2	VSS	Power		
G3	PF1	I/O	FMC_A1	
G4	PF0	I/O	FMC_A0	
G5	VDD	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G11	VSS	Power		
G13	VDD	Power		
G14	PG5	I/O	FMC_BA1	
G15	PG6	I/O	QUADSPI_BK1_NCS	
				

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)			
G16	VSS	Power		
G17	VDD50_USB	Power		
H1	PI12	I/O	LTDC_HSYNC	
H2	PI13	I/O	LTDC_VSYNC	
H3	PI14	I/O	LTDC_CLK	
H4	PF3	I/O	FMC_A3	
H5	VDD	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H11	VSS	Power		
H13	VDD	Power		
H14	PG4	I/O	FMC_BA0	
H16	PG2	I/O	FMC_A12	
H17	PK2	I/O	LTDC_G7	
J1	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
J2	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
J3	VSS	Power		
J4	PF5	I/O	FMC_A5	
J5	PF4	I/O	FMC_A4	
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J11	VSS	Power		
J13	VDD	Power		
J14	PK0	I/O	LTDC_G5	
J15	PK1	I/O	LTDC_G6	
J16	VSS	Power		
J17	VSS	Power		
K1	NRST	Reset		
K2	PF6	I/O	QUADSPI_BK1_IO3	
КЗ	PF7	I/O	QUADSPI_BK1_IO2	
K4	PF8	I/O	QUADSPI_BK1_IO0	
K5	VDD	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		

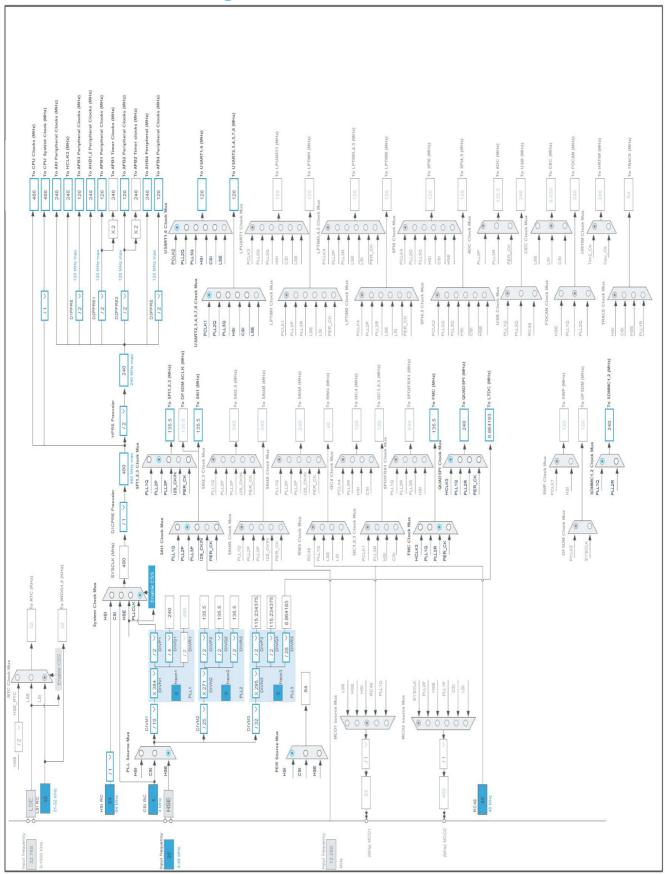
Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)		(0)	
K10	VSS	Power		
K11	VSS	Power		
K13	VDD	Power		
K14	PJ11	I/O	LTDC_G4	
K15	VSS	Power	2100_04	
K16	NC NC	NC NC		
K17	NC	NC NC		
L1	VDDA	Power		
L3	PF10	I/O	QUADSPI_CLK	
L4	PF9	I/O	QUADSPI_BK1_IO1	
L5	VDD	Power		
L7	VSS	Power		
L8	VSS	Power		
L9	VSS	Power		
L10	VSS	Power		
L11	VSS	Power		
L13	VDD	Power		
L14	PJ10	I/O	LTDC_G3	
L15	VSS	Power		
L16	NC	NC		
L17	NC	NC		
M3	PC2	I/O	FMC_SDNE0	
M4	PC3	I/O	FMC_SDCKE0	
M5	VDD	Power		
M13	VDD	Power		
M14	PJ9	I/O	LTDC_G2	
M15	VSS	Power		
M16	NC	NC		
M17	NC	NC		
N1	VREF-	Power		
N2	PH2 *	I/O	GPIO_Input	BT_TAG
N3	PA2 *	I/O	GPIO_Output	LED_LOAD1
N4	PA1 *	I/O	GPIO_Output	LED_LOAD0
N5	PA0	I/O	UART4_TX	
N7	VDD	Power		
N8	VDD	Power		
N9	PE10	I/O	FMC_D7	
N10	VDD	Power		
N11	VDD	Power		
		-		

Pin Number	Pin Name	Pin Type	Alternate	Label
TFBGA240	(function after		Function(s)	
	reset)		, ,	
N12	VDD	Power		
N13	PJ8	I/O	TIM8_CH1	
N15	PJ6	I/O	LTDC_R7	
N16	VSS	Power		
N17	NC	NC		
P1	VSSA	Power		
P2	PH3 *	I/O	GPIO_Input	BT_BACK
P3	PH4 *	I/O	GPIO_Input	BUTTON
P4	PH5	I/O	FMC_SDNWE	
P5	PI15 *	I/O	GPIO_Output	BACKLIGHT_EN
P7	PF13	I/O	FMC_A7	
P8	PF14	I/O	FMC_A8	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P13	PH10 *	I/O	GPIO_Output	LED_MENU
P15	PD15	I/O	FMC_D1	
P16	PD14	I/O	FMC_D0	
P17	VDD	Power		
R4	VSS	Power		
R6	PB2 *	I/O	GPIO_Input	BT_ENC
R7	PF12	I/O	FMC_A6	
R8	VSS	Power		
R9	PF15	I/O	FMC_A9	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PJ5	I/O	LTDC_R6	
R13	PH9 *	I/O	GPIO_Output	LED_INFO
Т3	PA5	I/O	SPI1_SCK	
T5	PB1 *	I/O	GPIO_Input	BT_LOAD1
T6	PJ2	I/O	LTDC_R3	
T7	PF11	I/O	FMC_SDNRAS	
Т8	PG0	I/O	FMC_A10	
Т9	PE8	I/O	FMC_D5	
T10	PE13	I/O	FMC_D10	
T12	VSS	Power		
T13	PH8 *	I/O	GPIO_Output	P8EN
T14	PB12 *	I/O	GPIO_Input	BT_BROWSE
T16	PD10	I/O	FMC_D15	
T17	PD9	I/O	FMC_D14	

Pin Number TFBGA240	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
U1	VSS	Power		
U2	PA3 *	I/O	GPIO_Output	LED_ENC
U3	PA4 *	I/O	GPIO_Output	SPI1_NSS
U5	PB0 *	I/O	GPIO_Input	BT_LOAD0
U6	PJ3	I/O	LTDC_R4	
U7	PJ4	I/O	LTDC_R5	
U8	PG1	I/O	FMC_A11	
U9	PE7	I/O	FMC_D4	
U10	PE14	I/O	FMC_D11	
U11	VCAP	Power		
U12	VDDLDO	Power		
U13	PH7 *	I/O	GPIO_Output	LED_TAGLIST
U14	PB13 *	I/O	GPIO_Output	LED_BROWSE
U16	PD8	I/O	FMC_D13	
U17	VSS	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	XDJX
Project Folder	C:\Keil_v5\My_Project\XDJX
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x800
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_UART4_Init	UART4
5	MX_DMA2D_Init	DMA2D
6	MX_LTDC_Init	LTDC
7	MX_SAI1_Init	SAI1
8	MX_SDMMC1_SD_Init	SDMMC1
9	MX_FATFS_Init	FATFS
10	MX_FMC_Init	FMC
11	MX_TIM8_Init	TIM8

Rank	Function Name	Peripheral Instance Name
12	MX_SPI1_Init	SPI1
13	MX_TIM2_Init	TIM2
14	MX_TIM3_Init	TIM3
15	MX_USART1_UART_Init	USART1
16	MX_QUADSPI_Init	QUADSPI
17	MX_SPI2_Init	SPI2
18	MX_UART7_Init	UART7

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
MCU	STM32H750XBHx
Datasheet	DS12556_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

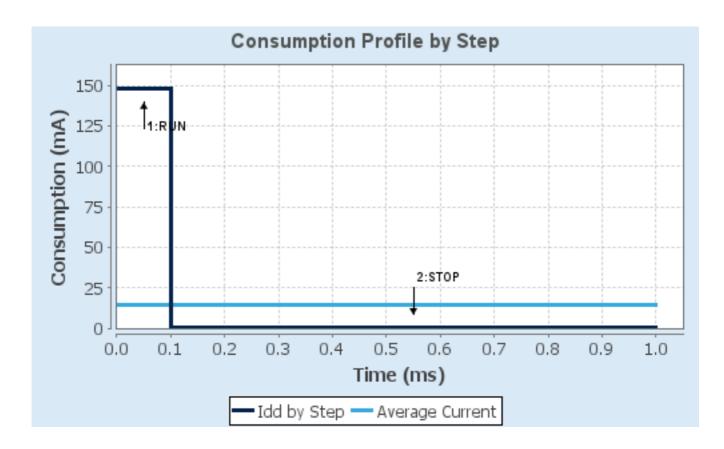
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	108.57	124.98
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001
	-	-	DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. DMA2D

mode: Activated

2.1.1. Parameter Settings:

Basic Parameters:

Transfer Mode Memory to Memory

Color Mode ARGB1555 *

Output Offset 0

Foreground layer Configuration:

DMA2D Input Color Mode ARGB1555

DMA2D ALPHA MODE

No modification of the alpha channel value

Input Alpha 0
Input Offset 0

DMA2D ALPHA Inversion Regular Alpha

DMA2D Red and Blue swap

Regular mode (RGB or ARGB)

DMA2D Chroma Sub-Sampling Mode

No chroma sub-sampling 4:4:4

2.2. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 13 bits

Data: 16 bits

Byte enable: 16-bit byte enable

2.2.1. SDRAM 1:

SDRAM control:

Bank SDRAM bank 1

Number of column address bits

9 bits *

Number of row address bits

13 bits

CAS latency 3 memory clock cycles *

Write protection Disabled

SDRAM common clock 2 HCLK clock cycles *

SDRAM common burst read Enabled *

SDRAM common read pipe delay 1 HCLK clock cycle *

SDRAM timing in memory clock cycles:

Load mode register to active delay

Exit self-refresh delay

7 *

Self-refresh time

4 *

SDRAM common row cycle delay

Write recovery time

4 *

SDRAM common row precharge delay

Row to column delay

2 *

2.2.2. Bank Mapping:

Mapping parameters:

FMC bank mapping Default mapping

2.3. LTDC

Display Type: RGB565 (16 bits)

2.3.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width 94 * Horizontal Back Porch 6 * Active Width 480 * Horizontal Front Porch 41 * **HSync Width** 93 Accumulated Horizontal Back Porch Width 99 Accumulated Active Width 579 Total Width 620

Synchronization for Height:

Vertical Synchronization Height

Vertical Back Porch

2

Active Height

Vertical Front Porch

2

VSync Height

Accumulated Vertical Back Porch Height

Accumulated Active Height

Total Height

17 *

233 *

16

18

251

Total Height

253

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

 Red
 0

 Green
 0

 Blue
 0

2.3.2. Layer Settings:

Layer Default Color:

Layer 0 - Alpha 0 Layer 0 - Blue 0 Layer 0 - Green 0 0 Layer 0 - Red Layer 1 - Alpha 0 Layer 1 - Blue 0 0 Layer 1 - Green Layer 1 - Red 0

Windows Position:

Layer 0 - Window Horizontal Start 0

Layer 0 - Window Horizontal Stop 480 *

Layer 0 - Window Vertical Start 0

Layer 0 - Window Vertical Stop 233 *

Layer 1 - Window Horizontal Start 0

Layer 1 - Window Horizontal Stop 480 *

Layer 1 - Window Vertical Start 0

Layer 1 - Window Vertical Start 0

Layer 1 - Window Vertical Start 233 *

Pixel Parameters:

Layer 0 - Pixel Format

ARGB1555 *

Layer 1 - Pixel Format

ARGB1555 *

Blending:

Layer 0 - Alpha constant for blending 255 *

Layer 0 - Blending Factor1 Alpha constant
Layer 0 - Blending Factor2 Alpha constant

Layer 1 - Alpha constant for blending 255 *

Layer 1 - Blending Factor1 Alpha constant
Layer 1 - Blending Factor2 Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress 0xC0000000 *

Layer 0 - Color Frame Buffer Line Length (Image 480 *

Width)

Layer 0 - Color Frame Buffer Number of Lines (Image 233 *

Height)

Layer 1 - Color Frame Buffer Start Adress 0xC00369C0 *

Layer 1 - Color Frame Buffer Line Length (Image 480 *

Width)

Layer 1 - Color Frame Buffer Number of Lines (Image 233 *

Height)

Number of Layers:

Number of Layers 2 layers

2.4. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

2.4.1. Parameter Settings:

General Parameters:

Clock Prescaler 4 *
Fifo Threshold 4 *

Sample Shifting Half Cycle *

Flash Size 22 *

Chip Select High Time 2 Cycles *

 Clock Mode
 Low

 Flash ID
 Flash ID 1

 Dual Flash
 Disabled

2.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.5.1. Parameter Settings:

Power Parameters:

SupplySource PWR_LDO_SUPPLY

Power Regulator Voltage Scale Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000
CSI Calibration Value 32
HSI Calibration Value 64

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 4 WS (5 CPU cycle)

Product revision rev.V

PLL range Parameters:

PLL1 clock Input range

Between 2 and 4 MHz

PLL2 input frequency range

Between 1 and 2 MHz

PLL3 input frequency range

Between 8 and 16 MHz

PLL1 clock Output range

PLL2 clock Output range

PLL3 clock Output range

PLL3 clock Output range

Wide VCO range

Wide VCO range

2.6. SAI1

Mode: Asynchronous Slave Mode: Synchronous Slave

2.6.1. Parameter Settings:

SAI A:

Synchronization Inputs Asynchronous

Protocol Free

Audio Mode Slave Transmit *

Frame Length (only Even Values) 64 *

Data Size

Slot Size

DataSize

Output Mode

Stereo

Companding Mode No companding mode

SAI SD Line Output Mode Driven
First Bit MSB First
Frame Synchro Active Level Length 32 *

Frame Synchro Definition Channel Identification *

Frame Synchro Polarity Active Low

Frame Synchro Offset Before First Bit *

First Bit Offset 0
Number of Slots (only Even Values) 2

Slot Active Final Value 0x00000003 *

Slot Active

User Setting *

Slot 0 Active true *
Slot 1 Active true *

Clock Strobing Rising Edge *

Fifo Threshold Empty
Output Drive Enabled *

SAI B:

Synchronization Inputs Synchronous with other block of same SAI

Protocol Free

Audio Mode Slave Transmit *

Frame Length (only Even Values) 64 *

Data Size 32 Bits *
Slot Size DataSize
Output Mode Stereo

Companding Mode No companding mode

SAI SD Line Output Mode Driven
First Bit MSB First
Frame Synchro Active Level Length 32 *

Frame Synchro Definition Channel Identification *

Frame Synchro Polarity Active Low

Frame Synchro Offset Before First Bit *

First Bit Offset 0
Number of Slots (only Even Values) 2

Slot Active Final Value 0x00000003 *
Slot Active User Setting *

Slot 0 Active true *
Slot 1 Active true *

Real Audio Frequency 0

Error between Selected 0

Clock Strobing Rising Edge *

Fifo Threshold Empty
Output Drive Enabled *

2.7. SDMMC1

Mode: SD 4 bits Wide bus 2.7.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made

SDMMC Clock output enable when the bus is idle

SDMMC hardware flow control

SDMMC clock divide factor

Is external transceiver present?

Rising transition

Disable the power save for the clock

The hardware control flow is disabled

14 *

no

2.8. SPI1

Mode: Full-Duplex Master

2.8.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 8 *

Baud Rate 16.9375 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

Fifo Threshold 01 Data

 Tx Crc Initialization Pattern
 All Zero Pattern

 Rx Crc Initialization Pattern
 All Zero Pattern

 Nss Polarity
 Nss Polarity Low

Master Ss Idleness 00 Cycle

Master Inter Data Idleness 00 Cycle

Master Receiver Auto Susp Disable

Master Keep lo State Enable *

IO Swap Disabled

2.9. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

2.9.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 32 *

Baud Rate 4.234375 MBits/s *

Clock Polarity (CPOL)

Clock Phase (CPHA)

1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Output Hardware
Fifo Threshold Fifo Threshold 01 Data

Tx Crc Initialization Pattern

Rx Crc Initialization Pattern

All Zero Pattern

All Zero Pattern

Nss Polarity

Nss Polarity Low

Master Ss Idleness00 CycleMaster Inter Data Idleness00 CycleMaster Receiver Auto SuspDisable

Master Keep Io State Enable *

IO Swap Disabled

2.10. SYS

Timebase Source: SysTick

2.11. TIM2

Clock Source : Internal Clock

2.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 239 *
Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) Internal Clock Division (CKD) Division by 2 * Disable auto-reload preload **Trigger Output (TRGO) Parameters:** Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed) Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR) 2.12. TIM3 **Combined Channels: Encoder Mode** 2.12.1. Parameter Settings: **Counter Settings:** Prescaler (PSC - 16 bits value) 0 Counter Mode Up Counter Period (AutoReload Register - 16 bits value) 65535 Internal Clock Division (CKD) No Division Disable auto-reload preload **Trigger Output (TRGO) Parameters:** Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed) Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR) **Encoder: Encoder Mode Encoder Mode TI1** ____ Parameters for Channel 1 ____ Polarity Rising Edge IC Selection Direct Prescaler Division Ratio No division Input Filter 5 * Parameters for Channel 2 ____

2.13. TIM8

Polarity

IC Selection

Input Filter

Prescaler Division Ratio

Clock Source: Internal Clock
Channel1: PWM Generation CH1

Rising Edge

No division

Direct

5 *

2.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 479 *
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 599 *

Internal Clock Division (CKD)

Division by 4 *

Repetition Counter (RCR - 16 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

BRK Sources Configuration

Digital Input
COMP1
Disable
COMP2
Disable
DFSDM
Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State Disable
BRK2 Polarity High
BRK2 Filter (4 bits value) 0

BRK2 Sources Configuration

Digital Input
COMP1
Disable
COMP2
Disable
DFSDM
Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

2.14. UART4

Mode: Asynchronous

2.14.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable **Data Inversion** Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

2.15. UART7

Mode: Asynchronous

2.15.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable Disable TX and RX Pins Swapping Overrun Enable DMA on RX Error Enable MSB First Disable

2.16. USART1

Mode: Asynchronous

2.16.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable

TX Pin Active Level Inversion

RX Pin Active Level Inversion

Disable

Data Inversion

Disable

TX and RX Pins Swapping

Overrun

Enable

DMA on RX Error

MSB First

Disable

2.17. FATFS

mode: SD Card

2.17.1. Set Defines:

Version:

FATFS version R0.12c

Function Parameters:

FS_READONLY (Read-only mode) Disabled
FS_MINIMIZE (Minimization level) Disabled

USE_STRFUNC (String functions) Enabled with LF -> CRLF conversion

USE_FIND (Find functions)

USE_MKFS (Make filesystem function)

USE_FASTSEEK (Fast seek function)

USE_EXPAND (Use f_expand function)

USE_CHMOD (Change attributes function)

USE_LABEL (Volume label functions)

USE_FORWARD (Forward function)

Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target) Latin 1

USE_LFN (Use Long Filename) Enabled with static working buffer on the BSS *

MAX_LFN (Max Long Filename) 255

LFN_UNICODE (Enable Unicode)

STRF_ENCODE (Character encoding)

UTF-8

FS_RPATH (Relative Path)

Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)

MAX_SS (Maximum Sector Size)

MIN_SS (Minimum Sector Size)

512

MULTI_PARTITION (Volume partitions feature)

USE_TRIM (Erase feature)

Disabled

FS_NOFSINFO (Force full FAT scan)

0

System Parameters:

FS_TINY (Tiny mode) Disabled
FS_EXFAT (Support of exFAT file system) Disabled

FS_NORTC (Timestamp feature) Fixed timestamp *

NORTC_YEAR (Year for timestamp) 2024 *

NORTC_MON (Month for timestamp) 5 *

NORTC_MDAY (Day for timestamp) 3 *

FS_REENTRANT (Re-Entrancy)

FS_TIMEOUT (Timeout ticks)

FS_LOCK (Number of files opened simultaneously)

3 *

2.17.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance SDMMC1
Use dma template Disabled
BSP code for SD Generic

2.17.3. Platform Settings:

Detect_SDIO PD5

^{*} User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
LTDC	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
2.50	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK3	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI12	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI13	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ11	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ9	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down		
	PJ6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ5	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ2	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ3	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PG6	QUADSPI_BK1_ NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF6	QUADSPI_BK1_I	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	QUADSPI_BK1_I O2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	QUADSPI_BK1_I O0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	QUADSPI_BK1_I O1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
SAI1	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
	DEO	0.414 .00 .0	Altamata Faratian Bark Bull	down	Speed	
	PE3	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SDMMC1	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low Von High	
SDIVIIVICI	PC10 PC11	SDMMC1_D2 SDMMC1_D3	Alternate Function Push Pull Alternate Function Push Pull	No pull-up and no pull-down No pull-up and no pull-down	Very High Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
	PG9	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PI1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI0	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PJ8	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PI9	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PA15 (JTDI)	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PI6	GPIO_Input	Input mode	Pull-up *	n/a	BT_INFO
	PI4	GPIO_Input	Input mode	Pull-up *	n/a	BT_TAGLIST
	PD5	GPIO_Input	Input mode	Pull-up *	n/a	SD_DETECT
	PI7	GPIO_Input	Input mode	Pull-up *	n/a	BT_MENU
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BT_SHIFT
	PH2	GPIO_Input	Input mode	Pull-up *	n/a	BT_TAG
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LED_LOAD1
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LED_LOAD0
	PH3	GPIO_Input	Input mode	Pull-up *	n/a	BT_BACK
	PH4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTTON
	PI15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	BACKLIGHT_EN
	PH10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LED_MENU
	PB2	GPIO_Input	Input mode	Pull-up *	n/a	BT_ENC
	PH9	GPIO_Output	Output Push Pull	No pull-up and no pull-down		LED_INFO

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					Medium *	
	PB1	GPIO_Input	Input mode	Pull-up *	n/a	BT_LOAD1
	PH8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	P8EN
	PB12	GPIO_Input	Input mode	Pull-up *	n/a	BT_BROWSE
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LED_ENC
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	SPI1_NSS
	PB0	GPIO_Input	Input mode	Pull-up *	n/a	BT_LOAD0
	PH7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LED_TAGLIST
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LED_BROWSE

3.2. DMA configuration

DMA request	Stream	Direction	Priority
MEMTOMEM	DMA1_Stream0	Memory To Memory	Medium *
SPI2_TX	DMA2_Stream0	Memory To Peripheral	Very High *
SPI2_RX	DMA2_Stream1	Peripheral To Memory	Very High *

MEMTOMEM: DMA1_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Enable *

FIFO Threshold: Full

Src Memory Increment: Enable *

Dst Memormy Increment: Enable *

Src Memory Data Width: Word *

Dst Memormy Data Width: Word *

Src Memory Burst Size: Single
Dst Memormy Burst Size: Single

SPI2_TX: DMA2_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte

Memory Data Width: Byte

Byte

SPI2_RX: DMA2_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *

Peripheral Data Width: Byte Memory Data Width: Byte

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
TIM2 global interrupt	true	2	0
TIM3 global interrupt	true	5	0
SPI2 global interrupt	true	2	0
USART1 global interrupt	true	4	0
UART4 global interrupt	true	7	0
DMA2 stream0 global interrupt	true	3	0
DMA2 stream1 global interrupt	true	3	0
UART7 global interrupt	true	6	0
SAI1 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
DMA1 stream0 global interrupt	unused		
SPI1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
FMC global interrupt	unused		
SDMMC1 global interrupt	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		
QUADSPI global interrupt	unused		
HSEM1 global interrupt	unused		

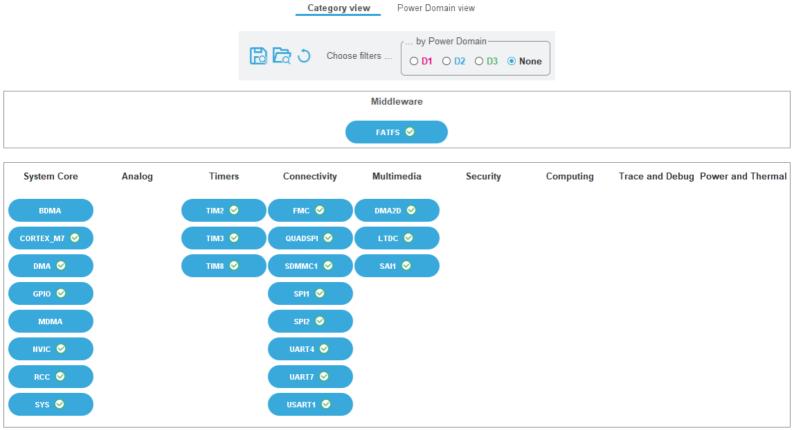
3.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM2 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
USART1 global interrupt	false	true	true
UART4 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream1 global interrupt	false	true	true
UART7 global interrupt	false	true	true
SAI1 global interrupt	false	true	true

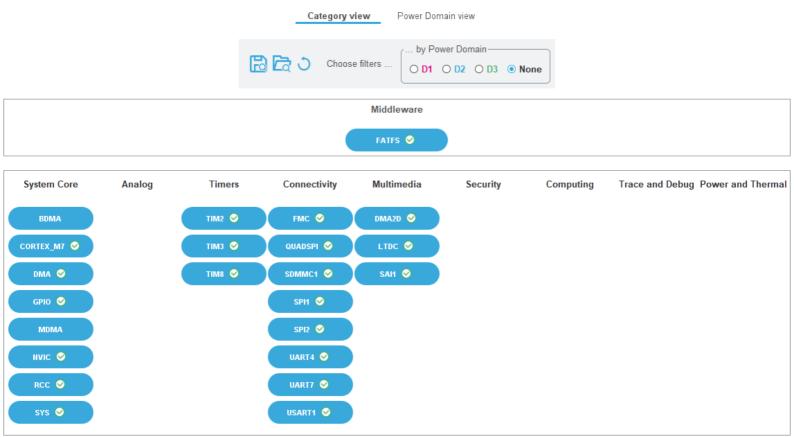
^{*} User modified value

4. System Views

- 4.1. Category view
- 4.1.1. Current



4.1.2. Without filters



4.2. Power Domain view

Category view Power Domain view



5. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip

System View https://www.st.com/resource/en/svd/stm32h7-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers_st

m32h7_series_product_overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_eval-

tools_portfolio.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_stm8_functi

onal-safety-packages.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_software_development_tools.pdf

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers-

stm32-family-overview.pdf

Brochures https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures https://www.st.com/resource/en/brochure/brstm32h7vl.pdf

Brochures https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-

and-smart-i-os.pdf

Flyers https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers https://www.st.com/resource/en/flyer/flstm32f7h7.pdf
Flyers https://www.st.com/resource/en/flyer/flstm32h7vl.pdf

Application Notes https://www.st.com/resource/en/application_note/an1181-electrostatic-

discharge-sensitivity-measurement-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an1709-emc-design-

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

- Application Notes https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf

- Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4891-stm32h72x-stm32h73x-and-singlecore-stm32h74x75x-system-architecture-and-performance-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4992-stm32-mcus-secure-firmware-install-sfi-overview-stmicroelectronics.pdf
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