CS 33: Computer Organization

Dis 1B: Week 10 Discussion

Agenda

Final Review?

or

Forget about the finals and watch NCAA tournament?

Final

- March 20th, Monday: 3PM ~ 6PM
- Kinsey Pavillion 1220B

Things we covered after the midterm

- Buffer overflow
- Optimization
- Cache
- Processes
- Threading
- Multithreading
- Linking
- Virtual Memory

Final

- Most of the questions will be from the materials after the midterm
- The format of the final will be very similar to the midterm

```
Return address of get_line is 0x400776
  Register %rbx will contain 0x0123456789ABCDEF
char *get line()
   char buf[4]:
   char *result;;
   qets(buf);
   result = malloc(strlen(buf));
   strcpy(result, buf);
   return result;
// Our input string is 0123456789012345678901234
0000000000400720 <get_line>:
400720: 53
                            %rbx
                      push
400721: 48 83 ec 10
                      sub
                              $0x10, %rsp
   // Draw a diagram of the stack at this point
400725: 48 89 e7
                      mov
                              %rsp, %rdi
400728: e8 73 ff ff ff callg 4006a0 <gets>
   // Modify diagram to show stack contents at this point
```

Adapted from Bryant and O'Hallaron, Computer Systems: A Programmer's Perspective, Third Edition

Assume the following

- The memory is byte addressable
- Memory accesses are to 1-byte words
- Addresses are 13 bits wide
- The cache is two-way set associative,
 with 4-byte block size and 8 sets

					-							
		L	ine 0	Line 1								
Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	09	1	86	30	3F	10	00	0	_	-	_	-
1	45	1	60	4F	E0	23	38	1	00	BC	0B	37
2	EB	0	_	-	_	_	0B	0	_		_	-
3	06	0	-		-	_	32	1	12	08	7B	AD
4	C7	1	06	78	07	C5	05	1	40	67	C2	3B
5	71	1	0B	DE	18	4B	6E	0	_	_	_	
6	01	1	Δ0	B7	26	2D	FO	0				

2-way set associative cache

The following figure shows the format of an address (one bit per box). Indicate (by labeling the diagram) the fields that would be used to determine the following:

12

37

DE

CO	The cache block offset
CI	The cache set index
CT	The cache tag

	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ													

	2-way set associative cache											
			L	ine 0	Line 1							
Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	09	1	86	30	3F	10	00	0	_	_	_	_
1	45	1	60	4F	E0	23	38	1	00	BC	0B	37
2	EB	0	-	_	-	-	0B	0	_	1	_	-
3	06	0	_	_	-	_	32	1	12	08	7B	AD
4	C7	1	06	78	07	C5	05	1	40	67	C2	3B
5	71	1	0B	DE	18	4B	6E	0	_	_	_	
6	91	1	A0	B 7	26	2D	F0	0	·—	-	-	_
7	46	0		_		_	DE	1	12	C0	88	37

- 0x0E34
- 0x0DD5
- 0x1FE4

			PW.			200	
A	Address	format	one	hit t	er	hox)	١.
1 1.	1 Luci Coo	Torinat	CIIC	OIL I		UUA	, .

12	11	10	9	8	7	6	5	4	3	2	1	0

B. Memory reference:

Parameter	Value
Cache block offset (CO)	0x
Cache set index (CI)	0x
Cache tag (CT)	0x
Cache hit? (Y/N)	
Cache byte returned	0xx

Adapted from Bryant and O'Hallaron, Computer Systems: A Programmer's Perspective Third Edition

```
int main()
    for (int i = 0; i < 3; i++)
        fork();
// How many processes are created by the program?
```

```
int main()
    int foo = fork();
    int bar = fork();
    if (foo != 0 && bar != 0)
        int tricky = fork();
        if (tricky == 0)
            printf("Wow this is tricky!\n");
        else
            printf("What\n");
    else if (foo != 0 && bar == 0)
        printf("Huh?\n");
    else
        printf("Hmm...\n");
   How many processes are created by the program?
```

- P locks the variable passed in as an argument
- V unlocks the variable passed in as an argument
- Will this program deadlock?

Thread 1:	Thread 2:	Thread 3:
P(a);	P(c);	P(c);
P(b);	P(b);	V(c);
V(b);	V(b);	P(b);
P(c);	V(c);	P(a);
V(c);	P(a);	V(a);
V(a);	V(a);	V(b);

- 0x03d4
- 0x03d7
- 0x03a9
- 0x0040

A. Virtual address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	value
VPN	
TLB index	
TLB tag	
TLB hit? (Y/N)	
Page fault? (Y/N)	
PPN	

C. Physical address format

11	10	9	8	7	6	5	4	3	2	1	0

Value

Adapted from Bryant and O'Hallaron, Computer Systems: A Programmer's Perspective, Third Edition

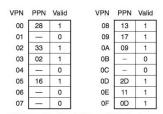
D. Physical memory reference

Parameter	Value
Byte offset	
Cache index	
Cache tag	
Cache hit? (Y/N)	
Cache byte returned	

	4		- TL	BT —		-	+TL	BI →	•					
101-1	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Virtual address														
addi ooo	-			- VPI	J —			-	4		_ v	PO -		

Set	Tag	PPN	Valid									
0	03		0	09	0D	1	00	-	0	07	02	1
1	03	2D	1	02	-	0	04	-	0	0A	-	0
2	02	_	0	08	=	0	06	-	0	03		0
3	07	-	0	03	0D	1	0A	34	1	02	-	0

(a) TLB: Four sets, 16 entries, four-way set associative



(b) Page table: Only the first 16 PTEs are shown



	— PP	N —	•		— PPO —			
ldx	Tag	Valid	Blk 0	Blk 1	Blk 2	Blk 3		
0	19	1	99	11	23	11		
1	15	0	_	_	_			
2	1B	1	00	02	04	08		
3	36	0	_	_	_			
4	32	1	43	6D	8F	09		
5	0D	1	36	72	F0	1D		
6	31	0	_	_	_			
7	16	1	11	C2	DF	03		
8	24	1	ЗА	00	51	89		
9	2D	0	_	_	_	_		
Α	2D	1	93	15	DA	3B		
В	0B	0	_	-	-	-		
C	12	0	_	_	-			
D	16	1	04	96	34	15		
Е	13	1	83	77	1B	D3		
F	14	0	_	_	_	_		

Good luck on your finals!

Thanks!