Department of Electrical Engineering
University of Moratuwa
B.Sc. Eng. Semester 3

EE3024 - Digital Signal Processing

Advanced Light Intensity Indicator (ALII)

Design Report

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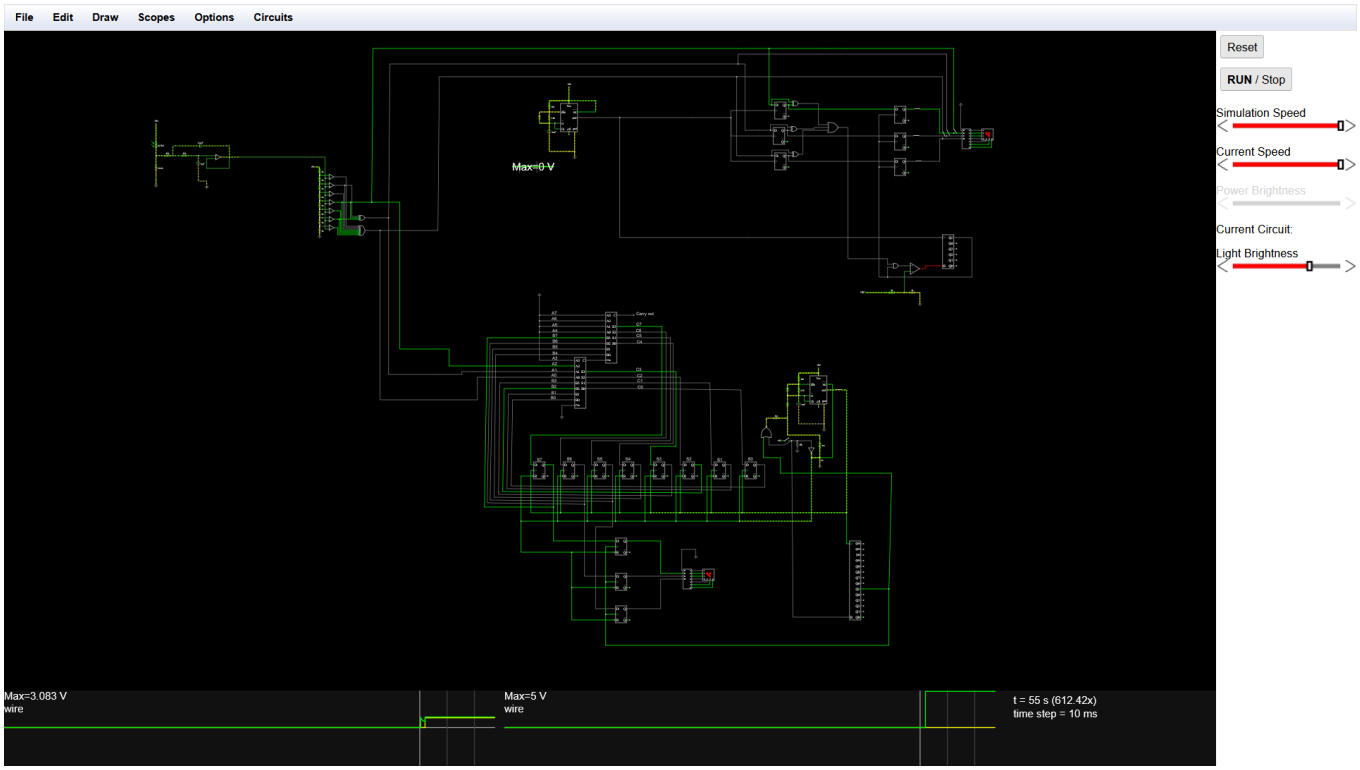
Introduction

The ALII module will sense ambient light by using an LDR. It must filter out noise, prevent false changes in count, and indicate both instantaneous and average light intensity through seven-segment displays. In this design, only analog components can be used, along with logic gates, counters, timers, and flip-flops, but without the use of programmable ICs.

This document explains how each required feature was achieved, the reasoning behind design decisions, key assumptions, and screenshots of relevant circuit sections.

Falstad Simulation



Feature 1 – Analog Noise Filtering

Objective:

Remove unwanted AC noise (mainly 50–100 Hz) from the LDR before sending it to comparators and counters.

A dedicated analog filter is required between the LDR voltage divider and the ADC (comparator) stages to ensure a clean and reliable signal.

Implementation

We used a simple RC low-pass filter to smooth the slowly changing LDR signal. It effectively removes high-frequency noise (50–100 Hz) without affecting the actual light-level signal and fits the project's component constraints.

Initial Filter Implementation;

Reasons to use Sallen Key 2nd order low-pass filter, Butterworth Design

- It removes noise more effectively than a simple RC filter.
- Easy to build with only two resistors, two capacitors, and an op-amp.
- Gives a clean, slow changing signal that matches ambient light changes.

Key decisions

- **Cut-off frequency: 10 Hz**

- The LDR has a slow response time (20–100 ms), so it cannot meaningfully detect light changes above ~10 Hz.
- Natural light variations are very slow and stay well below this range.
- Frequencies above 10 Hz mainly represent electrical noise rather than real light changes.

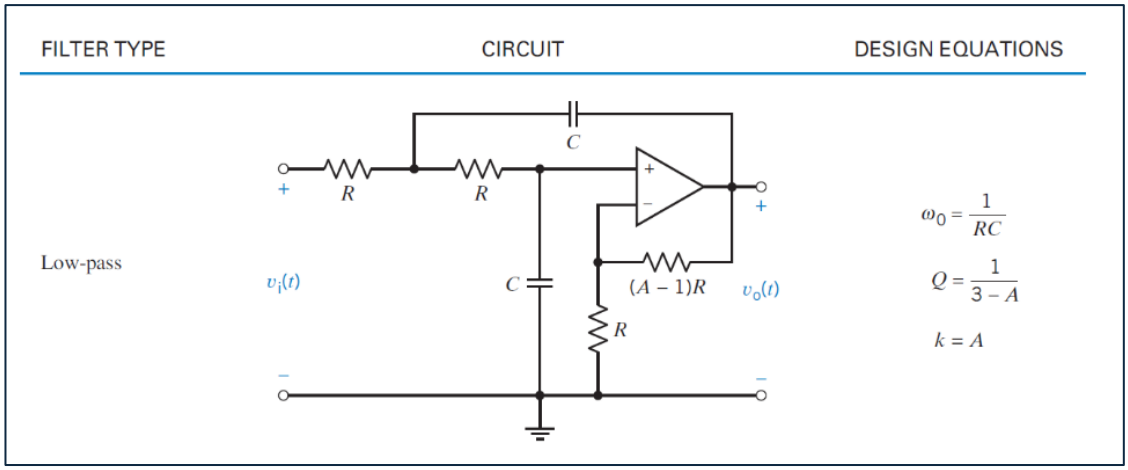
➢ **Stopband frequency: 50 Hz**

- The main interference source in indoor environments is AC mains flicker at 50–100 Hz.
- Designing the filter to suppress frequencies around 50 Hz directly targets this noise.

➢ **Attenuation: 20 dB**

- A 20 dB reduction sufficiently weakens the 50 Hz component, so it does not influence comparator outputs or the seven-segment display.

Filter Parameters



Selection of Low-Pass Filter Design

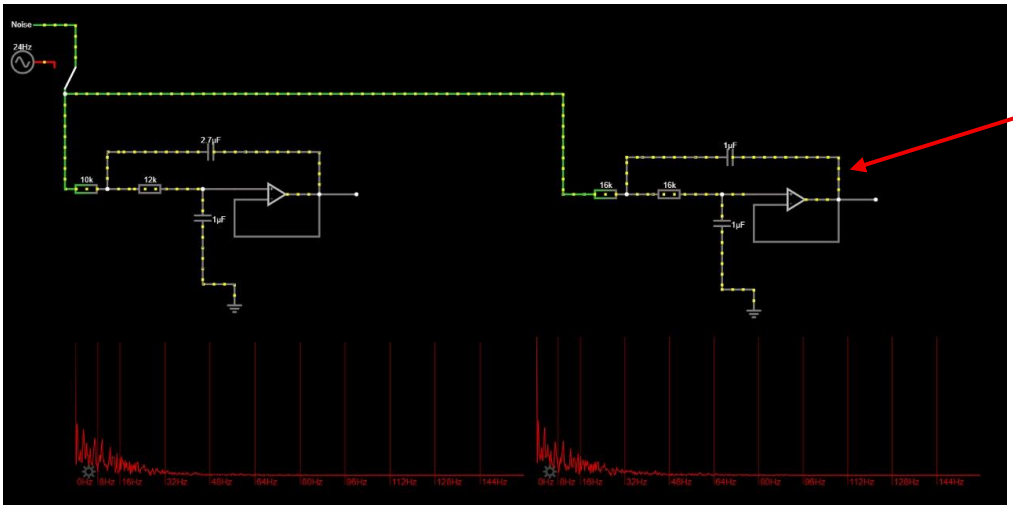
First, a standard second-order Sallen-Key low-pass filter was designed and tested, simulation showed that the variation in output voltage at very low frequencies (below 10 Hz) was limited.

Improved low-frequency performance was obtained by using a modified second-order filter with unequal values for resistor and capacitor. This design changed the damping factor of the filter, enabling a wider and more sensitive range of the output voltage for slow-varying signals. The project focuses on detection of the slowly changing light intensities. Therefore, the modified filter has been chosen for the final implementation

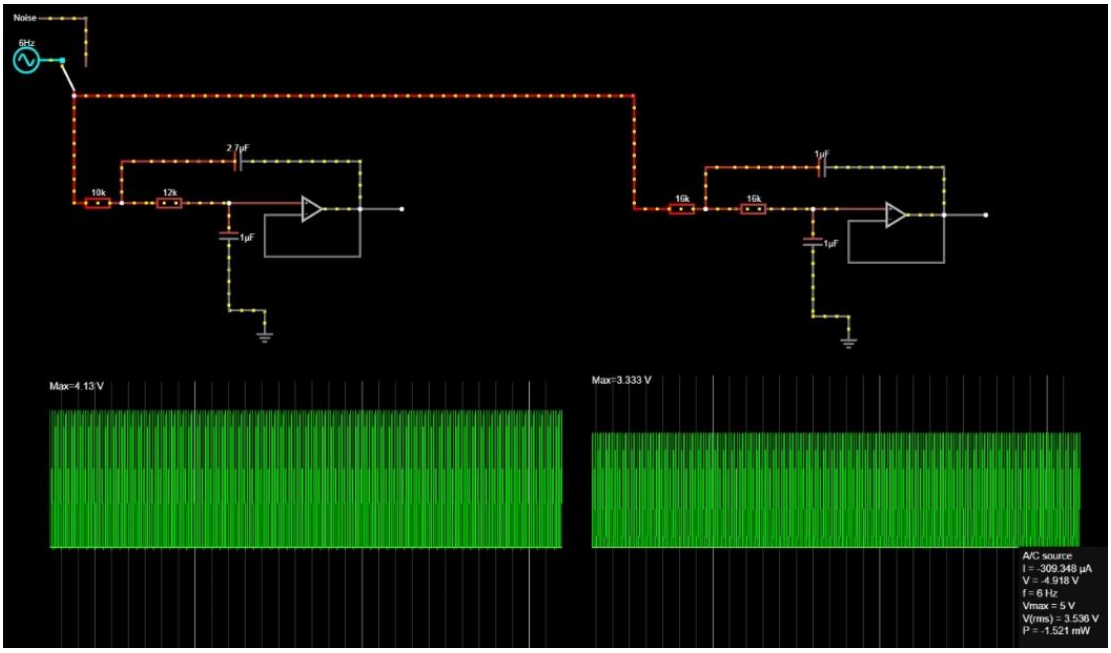
For a unity-gain Butterworth (A = 1):

Component	Value
R_1	10 kΩ
R_2	12 kΩ
C_1	2 µF
C_2	1 µF

Screenshots of comparing two Filters;



Sallen Key 2nd order low pass



Assumptions for Physical Implementation

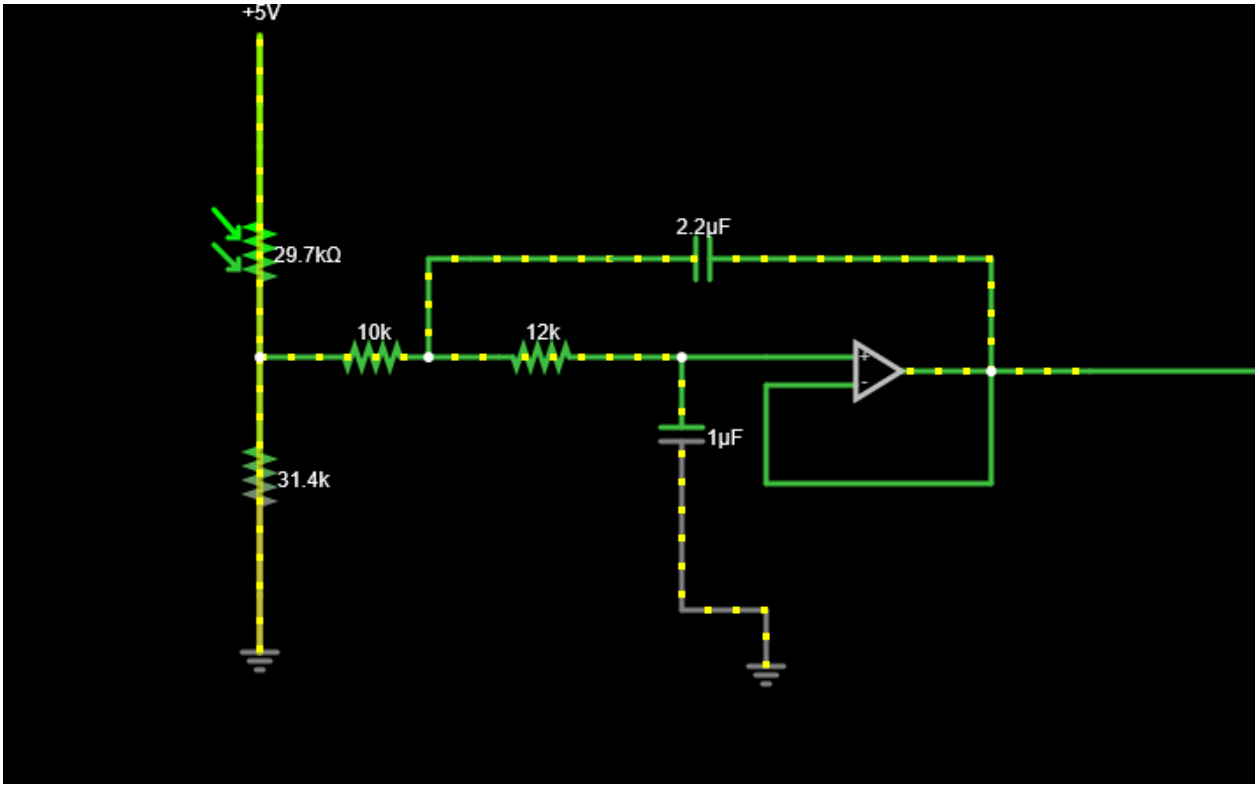
- The op-amp LM339 has been chosen for its ability to operate reliably on a single power supply with reference to its ground.
- Both resistors and capacitors can have a tolerance of (+/- 5%) without affecting the performance of the Butterworth filter.

Simple Physical Implementation

Uses only:

- 2 resistors
- 2 capacitors
- 1 op-amp

Falstad Simulation



Feature 2 – LDR Sensing & 0–7 Level Display

Objective:

Convert the LDR voltage into discrete 3-bit light levels (0–7) and display the result on a seven-segment display.

The filtered LDR output drives 8 comparators in the LM339. Each comparator compares the analog voltage with a unique threshold set by the resistor divider. The comparator outputs feed into an encoder (8-to-3 priority encoder) and the produces a 3-bit value (000–111). A decoder and 7-segment driver that converts this 3-bit light level into the corresponding digit 0–7.

Implementation Steps

(a) Comparators to Generate Thresholds

- We used a resistor ladder made of 1 kΩ resistors to create seven voltage levels.
- Each level is compared with the filtered LDR voltage using 7 comparators from the LM339.
- Each comparator has a 10 kΩ pull-up because LM339 outputs are open-collector.
- The result is seven digital signals showing which light zone the LDR is in.

(b) Priority Encoder (8 → 3)

- The seven comparator outputs are fed into an 8-to-3 priority encoder.
- It converts the multiple comparator signals into a clean 3-bit value (0–7)

(c) 3-bit to Seven-Segment Decoder

- Truth table maps 3-bit input (ABC) → seven-segment outputs (a–g).

(d) Seven-Segment Display

- A common-cathode display **is** used.
- The decoder drives the segments through resistors, showing the current light level (0–7).

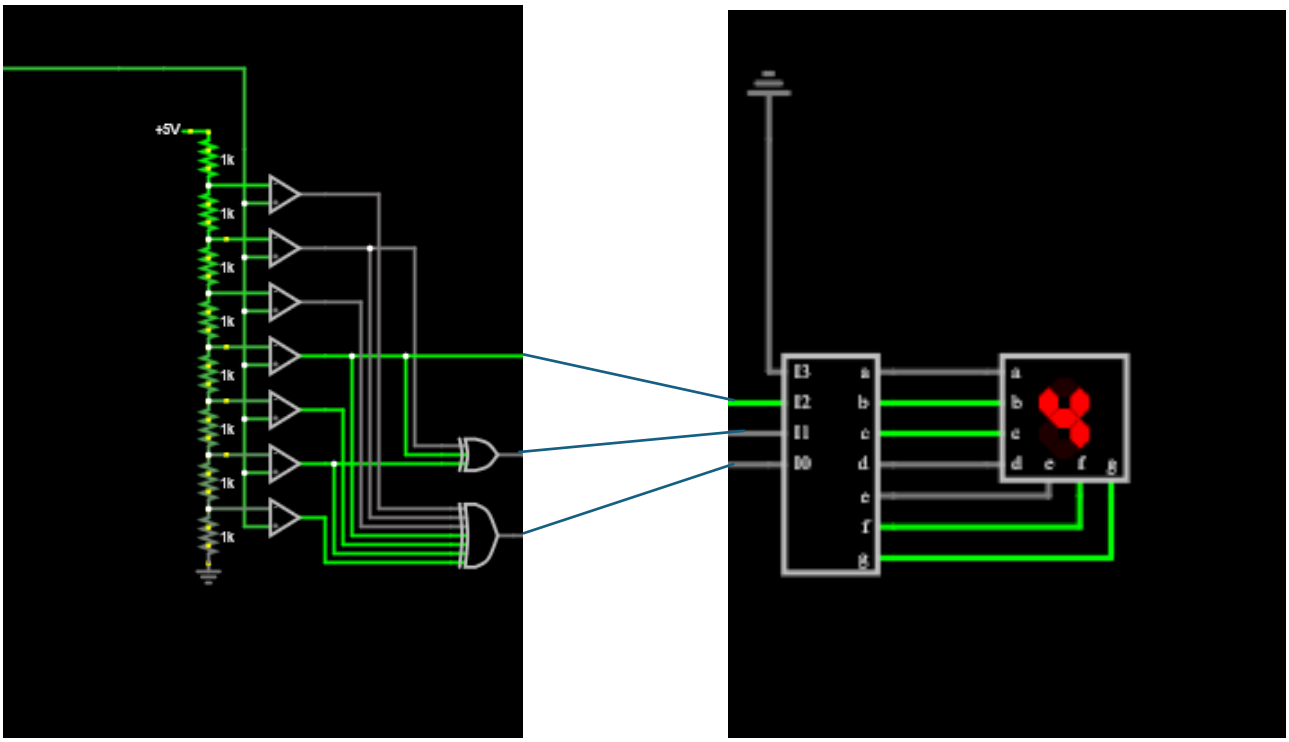
Circuit Design and Component values

Component	Value	Purpose
Ladder resistors	1 kΩ	Create 8 equally spaced voltage steps
Total ladder resistance	8 kΩ	Ladder current: I ≈ 0.693 mA low power, stable nodes
Voltage step	Vstep = 5 V ÷ 8 = 0.625 V	Each comparator triggers at a threshold: $V_{LDR} > V_{threshold}$
Pull-up resistors	10 kΩ	Required for LM339 open collector outputs. Ensures stable logic HIGH and adequate switching speed

Assumptions

- Light varies slowly enough that the comparator output is stable after filtering.
- Seven segment display is common cathode (as used in simulation).

Falstad Simulation



Feature 3 – Stability Timer (Avoid Sudden Light Changes)

Objective:

Update the light level display only when ambient light remains stable for a set period (30–300 s), adjustable via a variable resistor. Enable or disable this feature using a switch.

Process;

Core Operation (Common for Both Modes)

1. Current Value (0–7) is generated by the 3-bit encoder.
2. Stored Value is held inside D flip-flops, which also drive the 7-segment display.
3. Each bit of current is compared with stored using XOR gates.
    - Same bits - XOR = 0
    - Different bits - XOR = 1 (change detected)
4. All XOR outputs are combined using an OR gate.
5. When OR = 1, system detects a new light level. (reset)

Stabilize Mode (DIP 1,2,3 = ON)

1. When OR gate output = 1 , the system immediately resets the 12-bit counter
2. Display stays unchanged . (old stored value holds on the screen.)
3. The counter begins counting again from zero.
4. Only after the counter reaches its preset delay (30–300 sec), the 555 timer output reactivates, the stored value is updated and the display shows the new stable value.
5. Purpose: Prevent rapid fluctuations and show only stable readings.

Real-Time Mode (DIP 5,6,7 = ON)

1. XOR pulses are allowed to pass directly to the D flip-flops clock input.
2. Any detected change (XOR = 1) instantly updates the stored value.
3. Display shows the current encoder output in real time with no delay.
4. The 555 timer runs in the background as a stability window.
5. This forms a matched display and maintains live tracking of light changes.

Design Approach

Component	Function
Op-amp/comparator	detects current brightness
Encoder	produces CURRENT
Decoder	drives actual display bits
XOR gates	detect bit-changes between current and stored values
OR gates	combine bit change signals
12 bit counter	counts time (30–300 seconds)
555 timer	creates timing reference (resettable on sudden change)
D flip-flops (74LS74)	store stable output
DIP switch	user selects real-time or stabilized behaviour

Key decisions

- XOR gates are the best way to detect ANY bit change.
- The 555 timer gives a reliable long delay without microcontroller.
- A 12-bit counter was necessary to produce long timing (up to 300 seconds).
- DIP switch gives user control for each bit (1–3 stability, 5–7 real-time).

Assumptions

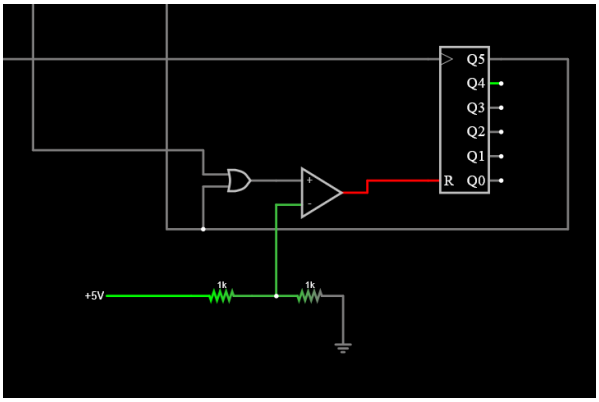
- Long timing values depend on RC accuracy (acceptable for this application).
- User can choose either mode using DIP switches”

Challenge in Stability and Reset Logic

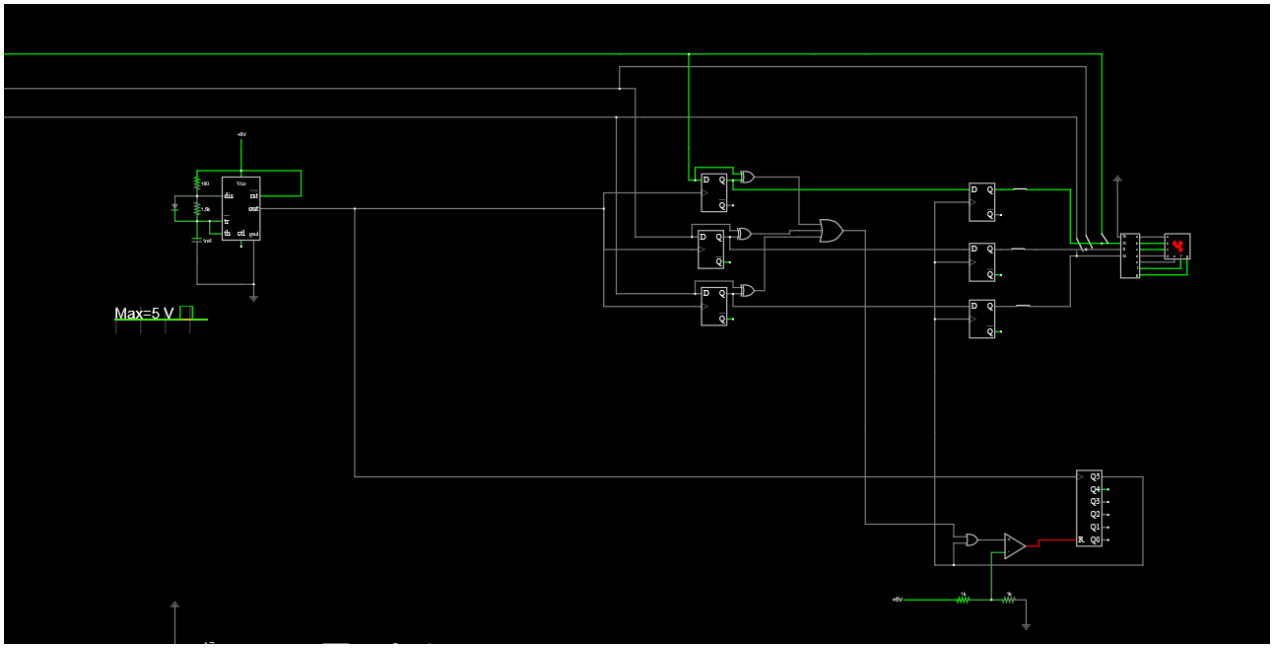
Small voltages at the output of the XORs during the testing, such as ≈0.07–0.08 V instead of a clear logic ‘0’, were interpreted by the XOR gate as logic ‘1’ and continuously triggered the reset through the OR gate.

Solution Implemented

This issue was resolved by adding an op-amp comparator before the reset logic. A 2.5 V reference was developed using a resistor divider from the 5 V supply. The op-amp ensured that only voltages in excess of 2.5 V were treated as logic ‘1’, thereby ensuring immunity to false resets. Stable operation was verified using oscilloscope measurements.



Falstad Simulation



Feature 4 – Average Light Measurement (300–900 s)

Objective:

Display the average light intensity over a long period (adjustable between 300 and 900 seconds) to provide a more complete view of ambient lighting conditions.

The function of this part is,

- Collects light readings over time.
- Calculates average to smooth out short-term fluctuations.
- Displays a stable light level reflecting overall brightness.

Implementation Steps

8-bit adder and accumulator design

Because a dedicated 8-bit adder was unavailable, two 4-bit adders are cascaded to form an 8-bit addition unit. The light intensity uses only 3 bits (0–6), so inputs A0–A2 of the adder are driven by the sensor, and A3–A7 are grounded.

The B-inputs of the adder are connected to the Q-outputs of an octal D-flip-flop array, which stores the current running sum. The output of the adder is looped back to the D inputs of the same flip-flops. Each clock pulse performs:

```
new_sum = previous_sum + sensor_value
```

Reset operation

A single pushbutton resets all storage and counting elements. Because the octal flip-flops and timer have active-LOW resets while the binary counter requires an active-HIGH reset, a NOT gate is used for polarity correction. A diode is added to discharge the 555 timer's capacitor instantly upon reset, ensuring a clean restart.

Average computation

After 32 samples, the total sum is divided by 32 to obtain the average:

average = sum / 32 = sum >> 5

Right-shifting by 5 bits yields a 3-bit result, which is fed into a separate bank of D flip-flops. These flip-flops prevent the output from updating continuously; they latch the average only when the sample count reaches 32.

Sample counter synchronization

A binary counter receives the same clock pulses as the accumulator. When 32 samples have been collected, counter output Q5 becomes HIGH. This Q5 output clocks the 3-bit latch, transferring the computed average to the 7-segment decoder.

Example:

For a total measurement duration of 400 seconds

Timer period = 400 / 32 = 12.5 seconds

After 32 pulses (400 s), the average value is latched and displayed.

The period of the 555 timer is tuned using the variable resistor; increasing its resistance increases the RC time constant and lengthens the sampling interval, while decreasing it shortens the interval.

Key Decisions and Assumptions

- 32 samples selected since it is a power of two, allowing division by simple right-shift instead of a divider circuit.
- Diode added at 555 timer to ensure the averaging cycle always restarts cleanly from zero.

Circuit Design

Component	Purpose
4-bit full adder	Standard fast ripple adder; cascadeable for wider widths.
Octal D-flip-flop	Store accumulator value between cycles
Counter	To count samples
555 timer	Generates the sample clock (adjustable). Its period determines total averaging time .
NOT gate	Logic inversions where needed.
BCD→7-segment decoder	Converts the accumulated sum into a 0–7 display
Reset button	Clears counters and D Flip-Flops for the new averaging period

Falstad Simulation