Department of Electrical Engineering
University of Moratuwa

B.Sc. Eng. Semester 3

EE3024 - Digital Signal Processing

Experiment 6: A/D conversion

Objective: To familiarize with the A/D conversion techniques.

Outcome: After successful completion of this session, you would be able to

a) Use the flash ADC technique effectively to convert Analog signals to Digital.

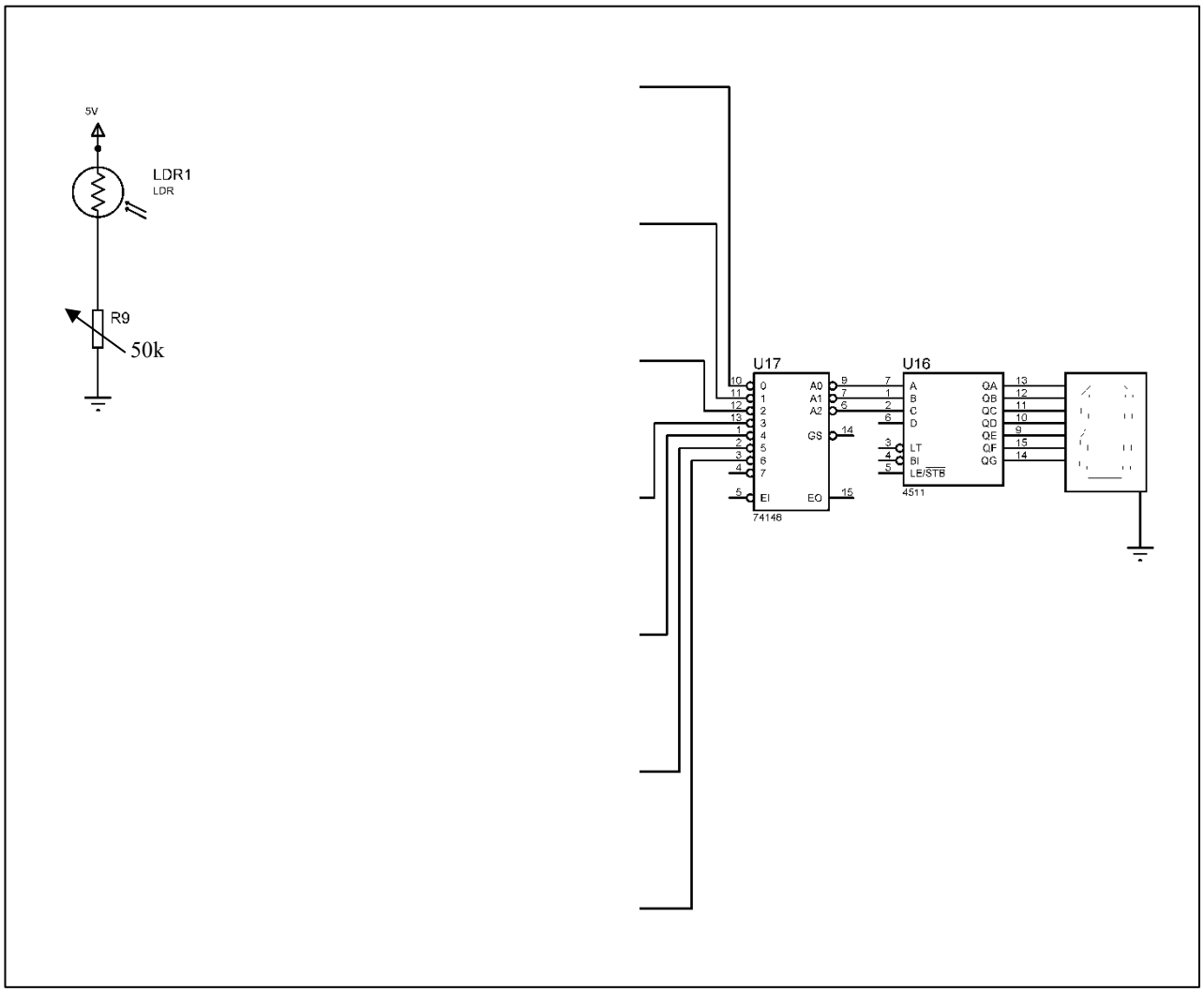
Equipment Required:

Multimeter
Breadboards
Power Supply

Components Required:

OP Amp LM339 x3
8 - 3 priority encoder 74HC148 x2
LDR x1
BCD to 7 Segment 4511 x2
1-Digit 7-Segment x1
Resistor 330Ω,1k,2k, 10K, 50K pot
Jumpers

Task 1: The following circuit is designed to convert the analog output of LDR to digital and display it in the seven-segment display. Complete the missing comparator part of the circuit.



Task 2: Build the circuit in the breadboard and observe the output on the seven-segment by varying the light intensity on the LDR.

5 Pin Configuration and Functions

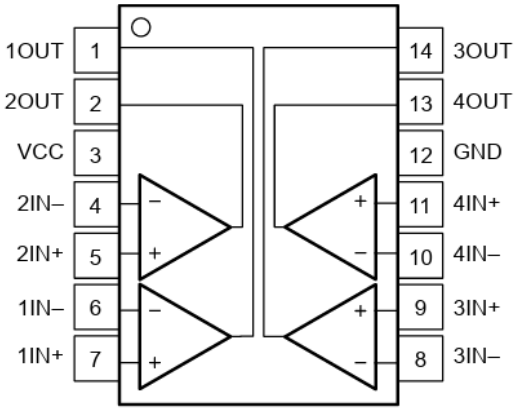
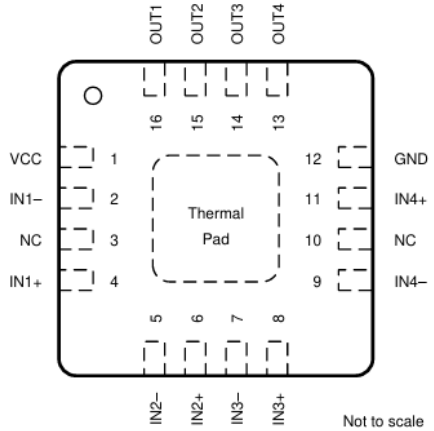
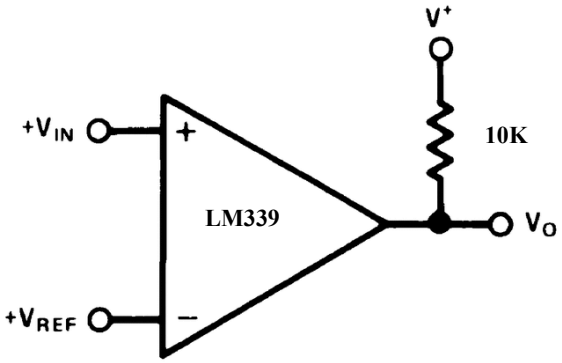


Figure 5-1. D, DB, N, NS, PW Packages
14-Pin SOIC, SSOP, PDIP, SOP, TSSOP
Top View



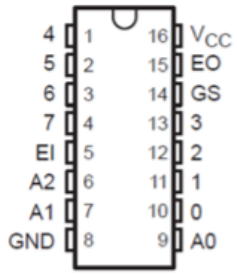
NOTE: Connect exposed thermal pad directly to GND pin.

Figure 5-2. RTE Package
16-Pad WQFN With Exposed Thermal Pad
Top View

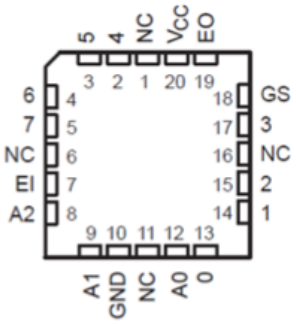


74HC148

5 Pin Configuration and Functions



J, D, N or NS Package
16-Pin CDIP, SOIC, PDIP, SO
Top View



FK Package
20-Pin LCCC
Top View

8.3 Device Functional Modes

Table 8-1. Function Table

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

4511

CDx4HC4511, CD74HCT4511 BCD-to-7 Segment Latch/Decoder/Drivers

1 Features

- 2-V to 6-V V_{CC} operation ('HC4511)
- 4.5-V to 5.5-V V_{CC} operation (CD74HCT4511)
- High-output sourcing capability
  - 7.5 mA at 4.5 V (CD74HCT4511)
  - 10 mA at 6 V ('HC4511)
- Input latches for BCD code storage
- Lamp test and blanking capability
- Balanced propagation delays and transition times
- Significant power reduction compared to LSTTL logic IC's
- 'HC4511
  - High noise immunity, N_{IL} or N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- CD74HCT4511
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V Maximum, V_{IH} = 2 V minimum
  - CMOS input compatibility, $I_I \leq 1_{\mu A}$ at V_{OL}, V_{OH}

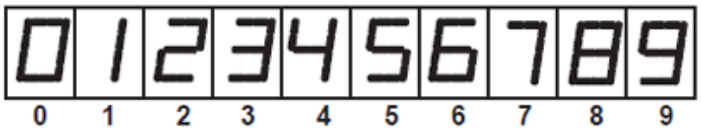
2 Description

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs (D_0–D_3), an active-low blanking ($\overline{BL}$) input, lamp-test ($\overline{LT}$) input, and a latch-enable ($\overline{LE}$) input that, when high, enables the latches to store the BCD inputs. When $\overline{LE}$ is low, the latches are disabled, making the outputs transparent to the BCD inputs.

Device Information

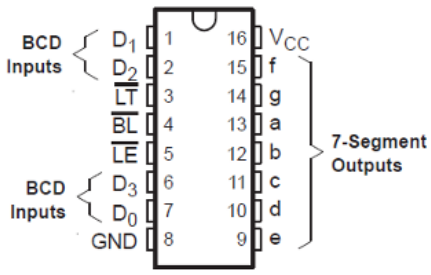
PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC4511	J (CDIP, 16)	24.38 mm × 6.92 mm
CD74HC4511	N (PDIP, 16)	19.31 mm × 6.35 mm
	D (SOIC, 16)	9.90 mm × 3.90 mm
	PW (TSSOP, 16)	5.00 mm × 4.40 mm
CD74HCT4511	N (PDIP, 16)	19.31 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Display

4 Pin Configuration and Functions



J, N, D, PW package
16-Pin CDIP, PDIP, SOIC, TSSOP
Top View

Seven Segment

NOTE: Need a Resistor for LEDs