CALIFORNIA STATE UNIVERSITY

1949

LONG BEACH

CECS 460

Transmit Engine

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1. Introduction

This project consists of two main parts, UART and the Tramel blaze. UART is Universal Asynchronous Receive/Transmit for short; however, only transmit is created for this project. Tramel blaze is an 16 bit emulator for 8 bit picoblaze, a fully embedded 8 bit RISC microcontroller core. The heart of this project is the shift register, where it shifts the inputted data serially to the Tx signal. The input of the shift register is 10 bits and it consists of 7 or 8 bits of data, Mark(1 bit of 1, Inactive), start bit of 0, stop bit of 1. The inactive state of the transmit is when the data is at one, so the when the data is shifted, the data that is shifted in is 1. The speed of the data bits being transferred is set by the baud rate from baud rate decode. Baud rate is also set from the 4 pull up resistors. Baud rate has the slowest rate of 300, where the input is 0000 and the fastest rate of 921600, where the input is 1011. Lastly, in order for the assembly to be connected correctly, the shifting led is implemented in assembly to directly see if the main of the assembly is connected correctly.

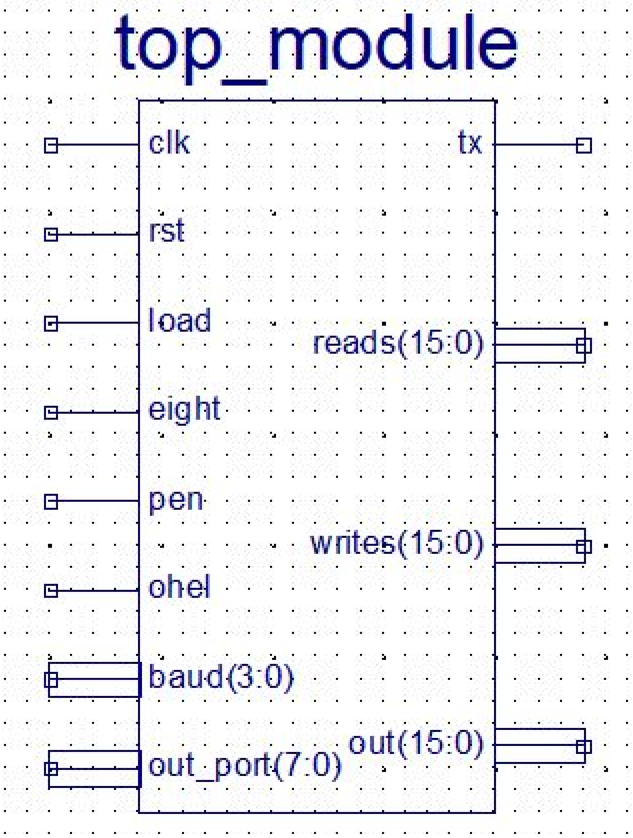
1.1 Purpose

The purpose of this project to understand the concept of the UART by creating the transmit before creating the full UART with transmit and receive.

2. Requirements

When in main loop, walk through the leds to get the immediate feedback from the main loop. When the Tx ready has induced the interrupt, the design must transmit the sequence “CSULB CECS 460 ##### <CR> <LF>”

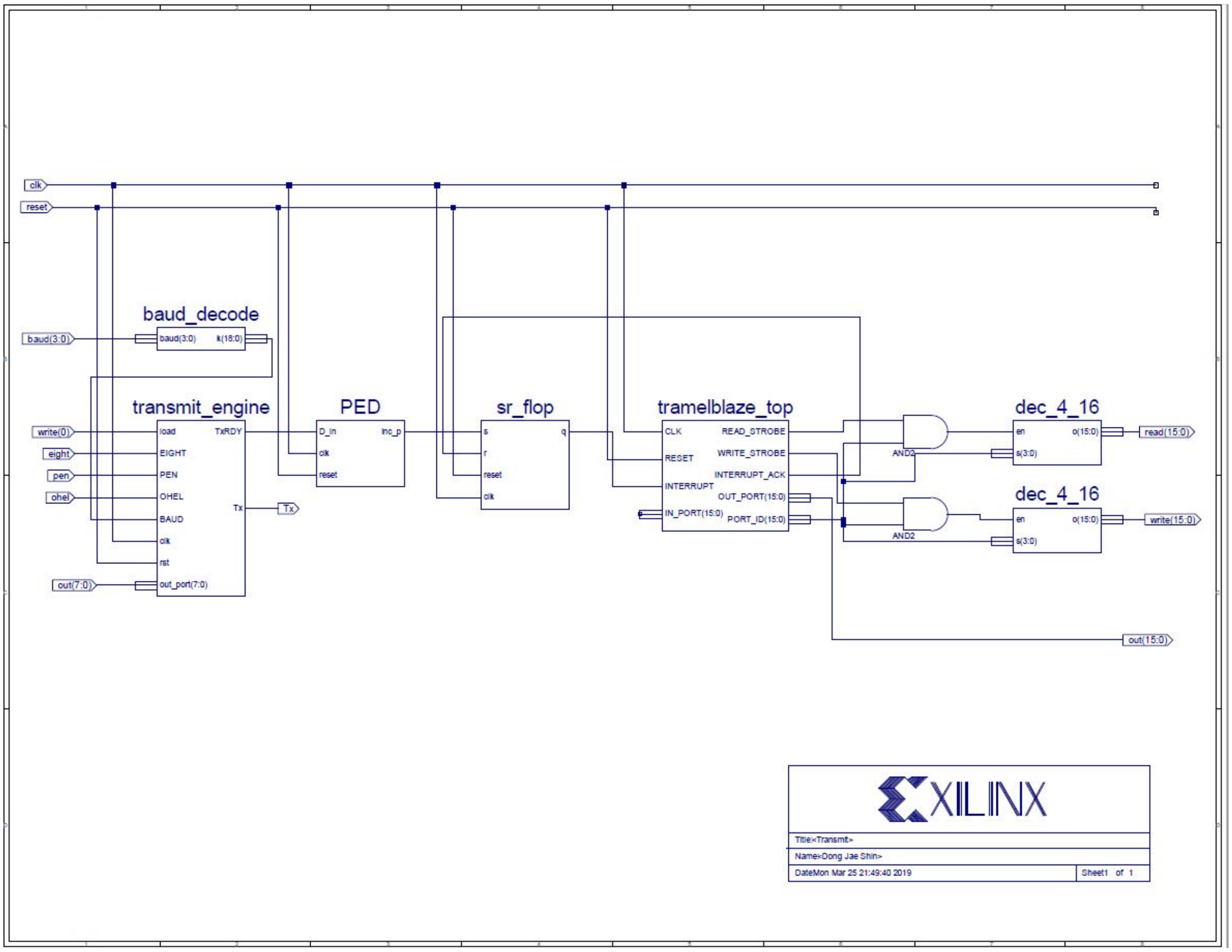
3. Top Level Design



3.1 Description

The purpose of this project was to create a counter in assembly as the transmit engine go through the characters of “CECS 460 ##### <CR> <LF> .” The data is communicated from the FPGA board to the computer using the terminal Real Term. The inputs of this project, eight, pen, and ohel will determine the packets of data that will be transferred serially. This input has to match that of the Real Term in order for the terminal to receive the data correctly. The input, baud, will determine the baud rate of the data being transferred. This also has to match the information that of the Real Term to receive the correct data intended. This project is only a part of the UART protocol. UART protocol usually consists of two main parts, the receive and transmit.

3.2 Block Diagram



3.3 I/O

3.3.1 Signal Names

Inputs	Bit length	Description
baud	4	Determines the rate of data being transferred
eight	1	Changes the size of the data being shifted
pen	1	Enables parity bit for the packets being transferred
ohel	1	Odd high even low. For the parity bit

Outputs	Bit length	Description
led_out	16	Walking the led directly from the assembly to see if the main loop of the main is working
tx	1	Data serially transferred using UART protocol

3.3.2 Pin Assignments

Name	Number	Name	Number	Name	Number
clk	E3	ohel	L16	pen	M13
eight	R15	baud[0]	R17	baud[1]	T18
baud[2]	U18	baud[3]	R13	led_out[0]	H17
led_out[1]	K15	led_out[2]	J13	led_out[3]	N14
led_out[4]	R18	led_out[5]	V17	led_out[6]	U17
led_out[7]	U16	led_out[8]	V16	led_out[9]	T15
led_out[10]	U14	led_out[11]	T16	led_out[12]	V15
led_out[13]	V14	led_out[14]	V12	led_out[15]	V11
rst	M18	tx	D4		

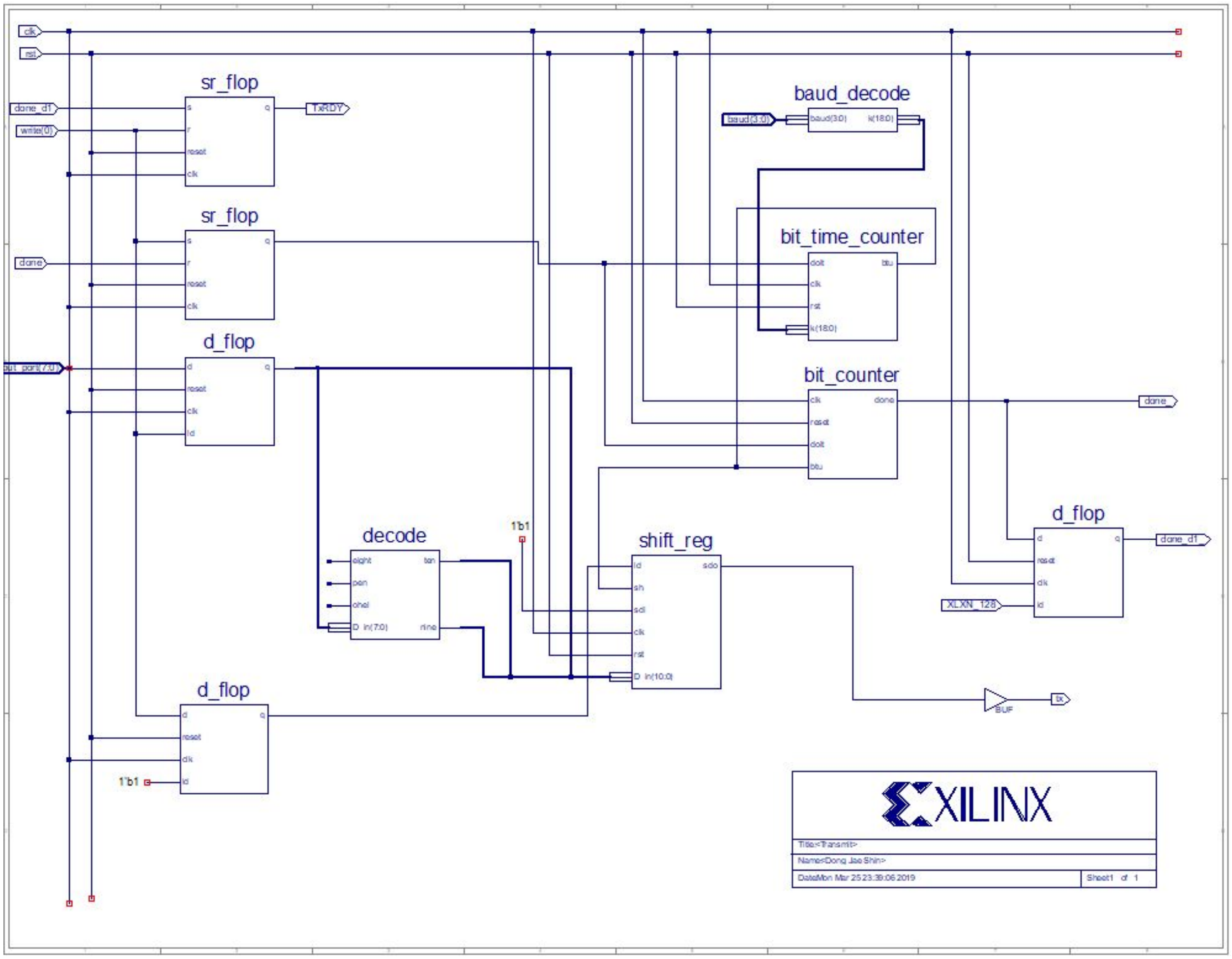
3.4 Clocks

Creates the 100MHz clock.

3.5 Resets

Resets are high active. The AISO(Asynchronous In Synchronous Out) is implemented to have all the registers have reset at the same clock period.

3.6 Transmit Engine



3.6.1 Shift Register

The shift register gets the input of the data in parallel and outputs the data serially. The transmit is off when the data is high. Therefore the filler data for the most significant bit is one bit of 1. Load of the shift register is from a one clock delayed least significant bit of the write. The shift register gets packet of 11 bits, where the 10th and 9th bits are determined by the parity decoder. The decoder logic is stated on table of the 3.6.2.

3.6.2 Parity Decoder

Eight	PEN	OHEL	D[10]	D[9]
0	0	0	1	1
0	0	1	1	1
0	1	0	1	Even Parity
0	1	1	1	Odd Parity
1	0	0	1	Bit 7
1	0	1	1	Bit 7
1	1	0	Even Parity	Bit 7
1	1	1	Odd Parity	Bit 7

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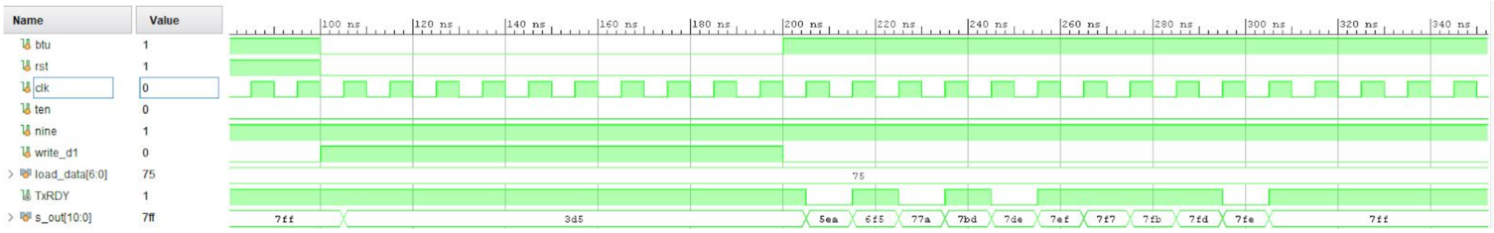
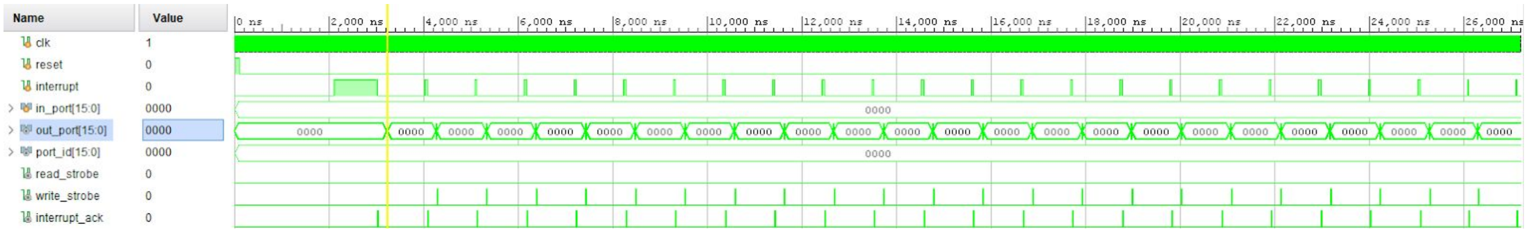
4. Simulation

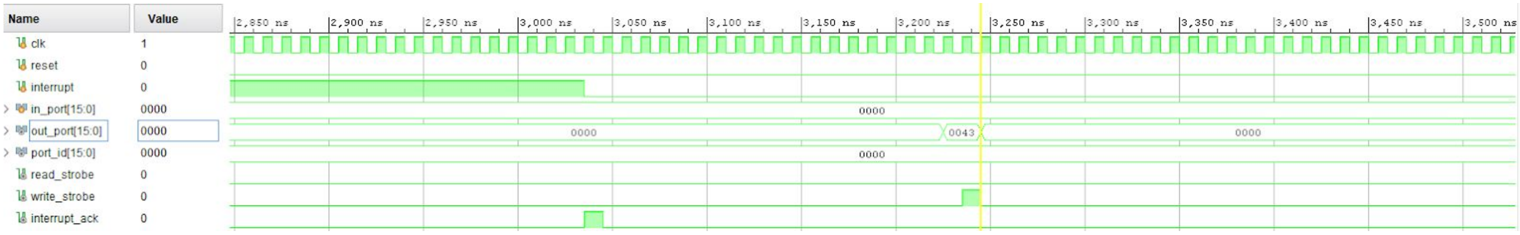
4.1 Shift Register



On the simulation above, the s_out signal is shifted one bit at a time.

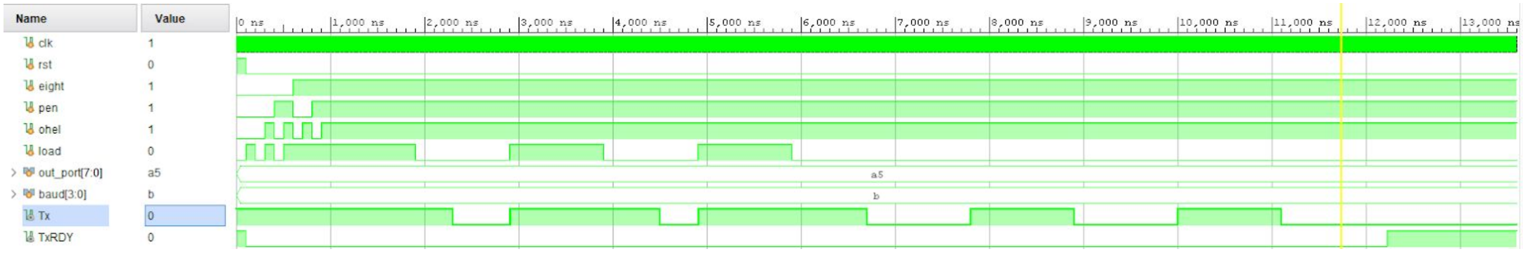
4.2 Tramel Blaze





On the simulation above, the write strobe is high when the out port data is inputted to the Transmit engine.

4.3 Transmit Engine



Name	Value
clk	1
rst	0
eight	1
pen	1
ohel	1
load	0
out_port[7:0]	a5
baud[3:0]	b
Tx	0
TxRDY	0

On the above simulation, the Tx is the least significant bit that is transmitted to the terminal serially.