The Cooper Union

PSET #6: Program Sample Runs

ECE-357

David Guo

Eric Xu

Sample Runs

Test 1: Test and Set Spin Lock

```
: ./2Atest
Expected: 64000000
With spinlock: 64000000
Wihout spinlock: 8661471
:
```

Test 2: Shell Game

```
./shellgame 3 20000
VCPU 0 starting, pid 122
VCPU 3 starting, pid 125
Main process spawned all children, waiting
VCPU 4 starting, pid 126
VCPU 1 starting, pid 123
VCPU 2 starting, pid 124
VCPU 5 starting, pid 127
VCPU 0 done
Child 0 (pid 122) done, sig handler was invoked 3482 times
Child pid 122 exited w/ 0
VCPU 1 done
Child 1 (pid 123) done, sig handler was invoked 3314 times
Child pid 123 exited w/ 0
VCPU 5 done
Child 5 (pid 127) done, sig handler was invoked 3377 times
VCPU 4 done
Child 4 (pid 126) done, sig handler was invoked 3113 times
VCPU 2 done
Child 2 (pid 124) done, sig handler was invoked 3414 times
VCPU 3 done
Child 3 (pid 125) done, sig handler was invoked 3428 times
Child pid 124 exited w/ 0
Child pid 125 exited w/ 0
Child pid 126 exited w/ 0
Child pid 127 exited w/ 0
       val
Sem#
                                   wakes
                     sleeps
 VCPU 0
                       3482
                                    3482
 VCPU 1
                         0
 VCPU 2
                       3414
                                    3414
 VCPU 3
                          0
                                       0
 VCPU 4
                                       0
                          Θ
 VCPU 5
                          0
          3
 VCPU 0
                          Θ
                                       0
 VCPU 1
                       3314
                                    3314
 VCPU 2
                          0
                                       0
 VCPU 3
                                       0
                          0
 VCPU 4
                       3113
                                    3113
 VCPU 5
                          0
                                       0
 VCPU 0
                          0
                                       0
 VCPU 1
                          0
                                       0
 VCPU 2
                                       0
                          Θ
 VCPU 3
                       3428
                                    3428
 VCPU 4
                          0
                                       0
                       3377
 VCPU 5
                                    3377
```