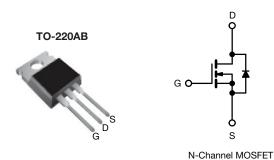
HALOGEN FREE



# **Power MOSFET**



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	100			
$R_{DS(on)}(\Omega)$	V <sub>GS</sub> = 10 V	0.27		
Q <sub>g</sub> max. (nC)	16			
Q <sub>gs</sub> (nC)	4.4			
Q <sub>gd</sub> (nC)	7.7			
Configuration	Single			

#### **FEATURES**

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- 175 °C operating temperature
- · Fast switching
- · Ease of paralleling
- · Simple drive requirements
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

#### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION			
Package	TO-220AB		
Lead (Pb)-free	IRF520PbF		
Lead (Pb)-free and halogen-free	IRF520PbF-BE3		

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V <sub>DS</sub>	100	V	
Gate-source voltage			$V_{GS}$	± 20	7 v	
Continuous drain current	\/ -+ 10\/	T <sub>C</sub> = 25 °C T <sub>C</sub> = 100 °C		9.2	А	
	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	6.5		
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	37	1	
Linear derating factor				0.40	W/°C	
Single pulse avalanche energy b			E <sub>AS</sub>	200	mJ	
Repetitive avalanche current <sup>a</sup>			I <sub>AR</sub>	9.2	Α	
Repetitive avalanche energy <sup>a</sup>			E <sub>AR</sub>	6.0	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	60	W	
Peak diode recovery dV/dt <sup>c</sup>			dV/dt	5.5	V/ns	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For	10 s		300	°C	
Mounting toward	6-32 or M3 screw			10	lbf ⋅ in	
Mounting torque				1.1	N⋅m	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b.  $V_{DD}$  = 25 V, starting  $T_J$  = 25 °C, L = 3.5 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 9.2 A (see fig. 12)
- c.  $I_{SD} \le 9.2$  A,  $dI/dt \le 110$  A/ $\mu$ s,  $V_{DD} \le V_{DS}$ ,  $T_J \le 175$  °C
- d. 1.6 mm from case



# Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62		
Case-to-sink, flat, greased surface	R <sub>thCS</sub>	0.50	-	°C/W	
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	2.5		

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static						•	
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0$	100	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.13	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	less	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V		1	-	25	μΑ
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>0</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	$I_D = 5.5 \text{ A}^{\text{ b}}$	1	-	0.27	Ω
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 5.5 A <sup>b</sup>		2.7	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0  MHz,  see fig. 5		1	360	-	pF
Output capacitance	C <sub>oss</sub>			ı	150	-	
Reverse transfer capacitance	$C_{rss}$			1	34	-	
Total gate charge	$Q_g$	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 9.2 A, V <sub>DS</sub> = 80 V, see fig. 6 and 13 <sup>b</sup>	1	-	16	nC
Gate-source charge	Q <sub>gs</sub>			-	-	4.4	
Gate-drain charge	$Q_{gd}$			-	-	7.7	
Turn-on delay time	t <sub>d(on)</sub>	$V_{DD}$ = 50 V, $I_{D}$ = 9.2 A, $R_{g}$ = 18 Ω, $R_{D}$ = 5.2 Ω, see fig. 10 b		-	8.8	-	ns
Rise time	t <sub>r</sub>			-	30	-	
Turn-off delay time	t <sub>d(off)</sub>			-	19	-	
Fall time	t <sub>f</sub>			-	20	-	
Gate input resistance	$R_g$	f = 1 MHz, open drain		1.0	-	5.0	Ω
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	- nH
Internal source inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristic	cs					•	
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.2	- A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	37	
Body diode voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = 9.2$ A, $V_{GS} = 0$ V b		1	-	1.8	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 9.2 A, dl/dt = 100 A/µs b		-	110	260	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	0.53	1.3	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-		-on is do	minated b	y L <sub>S</sub> and	L <sub>D</sub> )

## Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq$  300  $\mu$ s; duty cycle  $\leq$  2 %



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

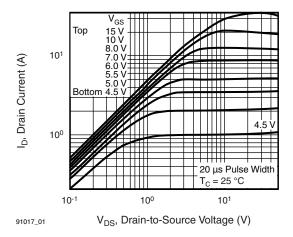


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

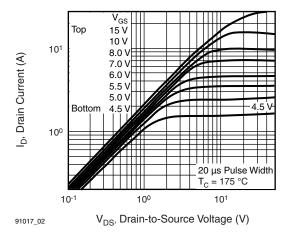


Fig. 2 - Typical Output Characteristics,  $T_C = 175$  °C

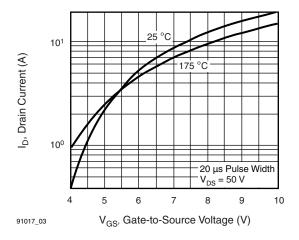


Fig. 3 - Typical Transfer Characteristics

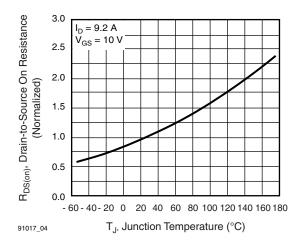


Fig. 4 - Normalized On-Resistance vs. Temperature

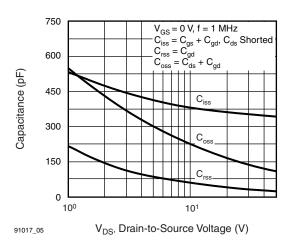


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

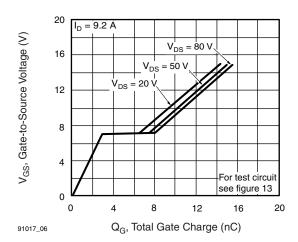


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



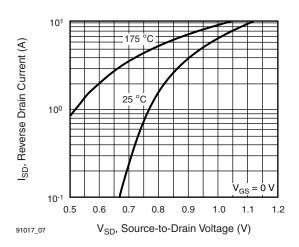


Fig. 7 - Typical Source-Drain Diode Forward Voltage

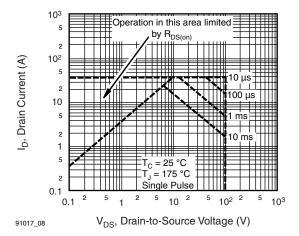


Fig. 8 - Maximum Safe Operating Area

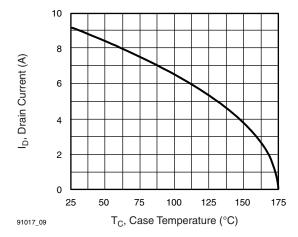


Fig. 9 - Maximum Drain Current vs. Case Temperature

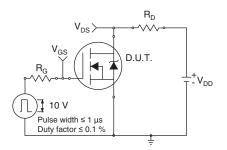


Fig. 10a - Switching Time Test Circuit

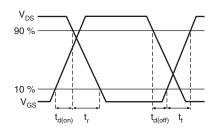


Fig. 10b - Switching Time Waveforms



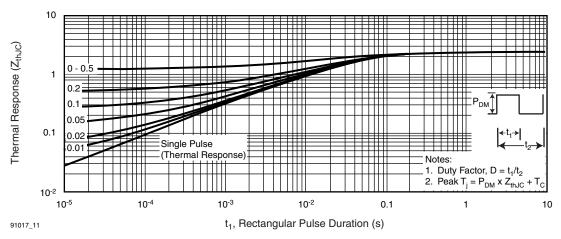


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

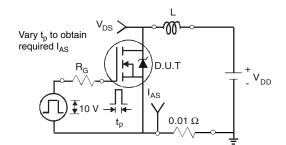


Fig. 12a - Unclamped Inductive Test Circuit

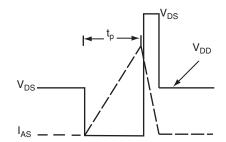


Fig. 12b - Unclamped Inductive Waveforms

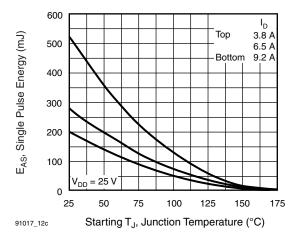


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



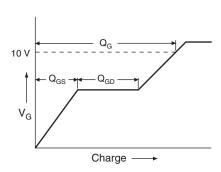


Fig. 13a - Basic Gate Charge Waveform

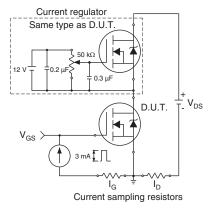
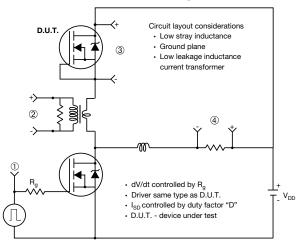


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



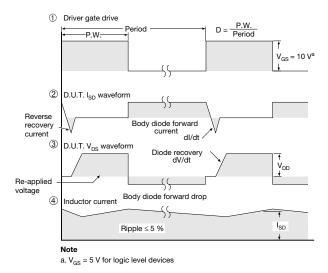


Fig. 14 - For N-Channel

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